

# Direct Digital Synthesizer With ROM-Less Architecture at 13-GHz Clock Frequency in InP DHBT Technology

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**Abstract**—A direct digital synthesizer (DDS) implemented in InP double heterojunction bipolar transistor (DHBT) technology is reported. The DDS has a ROM-less architecture and instead uses digital logic for phase conversion. The DDS operates up to a 13 GHz clock rate and is capable of synthesizing output frequencies up to 6.5 GHz. Measured spurious free dynamic range (SFDR) ranged from 34 dBc at low frequency control words (FCWs) to 26.67 dBc at high FCWs. The test circuit is implemented with 1646 transistors and consumes 5.42 W of power.

**Index Terms**—Accumulator, digital to analog converter (DAC), direct digital synthesizer (DDS), heterojunction bipolar transistor (HBT), high-speed integrated circuits (ICs), Indium Phosphide (InP).

## I. INTRODUCTION

RECENT advances in InP double heterojunction bipolar transistor (DHBT) technology allow for the implementation of complex digital and mixed-signal circuits operating at high clock rates. In this letter, we demonstrate a direct digital synthesizer (DDS) in an InP DHBT technology with  $f_t$  and  $f_{max}$  both over 300 GHz [1]. This technology integrates DHBTs with four levels of metal, precision resistors, and metal-insulator-metal (MIM) capacitors, making it well-suited for mixed-signal applications.

The development of the DDS demonstrates the ability to take advantage of the characteristics and intrinsic speed of the technology to yield complex mixed-signal circuits. Measured results show DDS operation up to a clock frequency ( $f_{clk}$ ) of 13 GHz, with 5.42 W of power consumption and a full-Nyquist spurious free dynamic range (SFDR) of 26.67 dBc. Table I shows a comparison to recently reported InP DDS results.

## II. CIRCUIT DESIGN

This design uses a traditional DDS architecture [2] with a phase accumulator, phase converter, and digital to analog converter (DAC) as shown in Fig. 1. The accumulator is 8-b wide, so the resulting fundamental output frequency of the DDS ( $f_0$ ) is 1/256 of the input clock frequency, with 128 steps of frequency

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TABLE I  
COMPARISON OF RECENTLY REPORTED InP DDS PERFORMANCE [3], [4]

Reference	$f_{clk}$ (GHz)	Power (W)	full-Nyquist SFDR (dBc)
[3]	9.2	15	30
[4]	10	8	35
[4]	12	8	30
This work	13	5.42	26.67

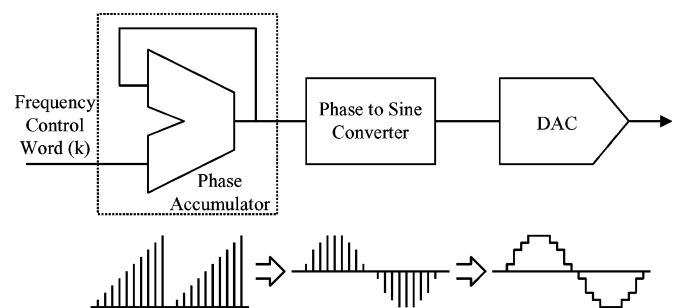


Fig. 1. Block diagram of a direct digital synthesizer with the outputs for each stage illustrated.

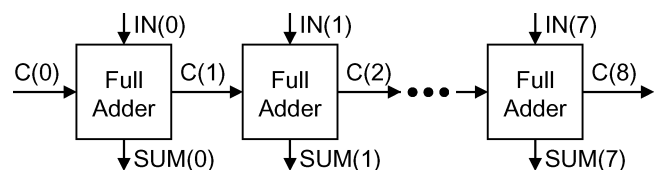


Fig. 2. Block diagram of the 8-b ripple carry accumulator. The sum outputs are registered and internally feed back for accumulation. The inputs to the full adders set the accumulation increment.

control. The 8-b accumulator output is truncated to 6-b for use in the phase conversion logic. This design uses a ROM-less approach, with logic gates performing the phase conversion operation. The DAC consists of a 4-b binary fine DAC and a 3-b coarse DAC.

### A. Phase Accumulator

Unlike previously reported high speed accumulators [5], [6], where pipelining is utilized to compute the accumulation over multiple clock cycles, the accumulator in this design computes the entire 8-b accumulation operation in a single clock cycle. As shown in Fig. 2, the accumulator is based on an 8-b ripple carry adder, with a string of full adders that all operate on the same

TABLE II  
COMPARISON OF THE POWER AND SPEED IN  
8-b ACCUMULATOR ARCHITECTURES

Reference	$f_{clk}$ (GHz)	Power (W)
[5]	41	7.86
[6]	40	6.39
This work	13	2.13

clock phase. The outputs of the full adders have built-in registers, and the sum bits feed back internally to perform accumulation. The inputs (IN) to the full adders set the accumulation increment, which is the frequency control word (FCW) of the DDS.

Since the 8-b accumulation is computed in a single clock cycle, the speed is limited by the long carry propagation path through all of the full adders. In simulation, the maximum operating frequency of the accumulator was found to be 13 GHz. In this DDS design, the accumulator is the limiting factor for speed, so the maximum operating frequency of the DDS is constrained to 13 GHz. While this single clock cycle accumulator is slower than previously reported accumulators [5], [6], it is advantageous because it contains fewer pipeline registers. This greatly reduces the power consumption, while also simplifying clock distribution of the circuit.

Extending the 4-b, 41-GHz accumulator [5] to 8-b, would lead to an estimated power consumption of 7.86 W, with two 4-b accumulator blocks at 2.86 W each and a 4-b register block at 2.12 W. Likewise, an extension of the reduced power accumulator [6] to 8-b is estimated to result in a power consumption of 6.39 W with 2.38 W from each of the 4-b accumulators and 1.63 W from the 2-b register. By comparison, the 8-b accumulator in this design uses only 2.13 W with a maximum simulated operating frequency of 13 GHz. Compared to the other designs, this adder operates at about one third of the speed and one third of the power. A speed and power comparison with previous work is shown in Table II.

### B. Phase Converter

Since both the accumulator and DAC have relatively narrow bit widths, the phase conversion can be implemented using only logic gates, eliminating the need for a ROM design. As is generally the case in DDS circuits, the phase conversion logic relies on quadrant symmetry to reduce the number of gates needed for sine conversion. The output of the accumulator is truncated so that the six most significant bits (MSBs), denoted as  $S_7$  to  $S_2$ , are used for the phase conversion. The second MSB ( $S_6$ ) is used to invert the data entering the phase conversion logic and to provide a half-wave sine output from the quarter-wave data. The MSB ( $S_7$ ) is used to invert the output data that drives the fine DAC bits, so that a full-wave sine output is generated.

The logic used in the phase converter is shown in Table III. The logic in the phase converter is designed to complete the conversion in a single clock cycle. The logic is also simplified to reduce the total number of gates and decrease power consumption. For this phase conversion scheme, the worst case simulated SFDR over the full-Nyquist range of FCWs was

TABLE III  
LOGIC USED IN THE PHASE CONVERTER TO DRIVE THE DAC

Inverted Inputs
$A = S_5 \oplus S_6$
$B = S_4 \oplus S_6$
$C = S_3 \oplus S_6$
$D = S_2 \oplus S_6$
Coarse DAC
$DAC_6 = \overline{S_7}$
$DAC_5 = (A + B \cdot C) \cdot S_7 + \overline{S_7}$
$DAC_4 = (A + B \cdot C) \cdot \overline{S_7}$
Binary Fine DAC
$DAC_3 = ((B \oplus C) + A) \oplus S_7$
$DAC_2 = (\overline{A} \cdot C + \overline{B}) \oplus S_7$
$DAC_1 = ((\overline{A} \cdot \overline{B} + \overline{C}) + (\overline{A} \cdot D + B \cdot D)) \oplus S_7$
$DAC_0 = ((\overline{A} \cdot \overline{B} + \overline{D}) + (\overline{A} \cdot \overline{C} + A \cdot B)) \oplus S_7$

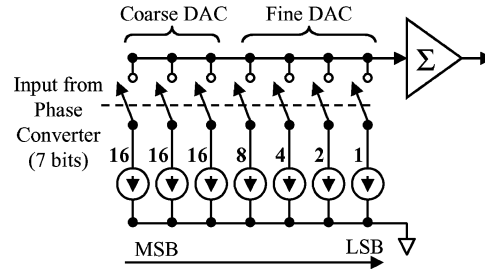


Fig. 3. Digital to analog converter with coarse and fine sections.

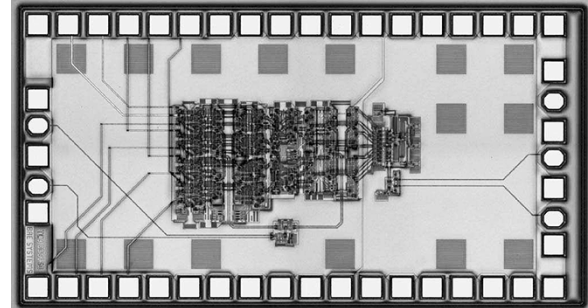


Fig. 4. Microphotograph of the DDS test chip. The chip has dimensions of 2700  $\mu\text{m}$  by 1450  $\mu\text{m}$  and contains 1646 transistors.

28.4 dBc. The simulation of SFDR versus FCW only factored in the impact of truncation and the simplifications to the phase conversion scheme, and did not include any nonlinearities from the DAC.

### C. DAC

The DAC has three coarse bits and four fine bits, as shown in Fig. 3. The coarse bits each drive 16 units of current, and the fine bits drive 8, 4, 2, and 1 units of current. The DAC generates a differential output voltage by summing the currents from the coarse and fine bits and has 64 discrete output levels.

## III. MEASUREMENT RESULTS

The DDS test chip shown in Fig. 4 has 1646 transistors in an area of 2700  $\mu\text{m}$  by 1450  $\mu\text{m}$ . The circuit was tested on wafer using a probe station and high frequency probes. The

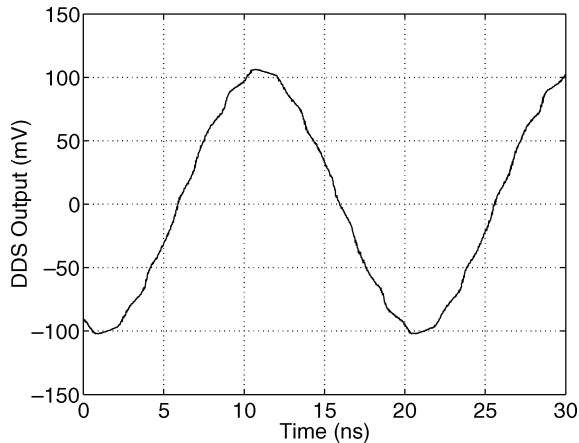


Fig. 5. Sampling oscilloscope output of the DDS with a clock frequency of 13 GHz and a frequency control word of 1. The output frequency is 50.781 25 MHz.

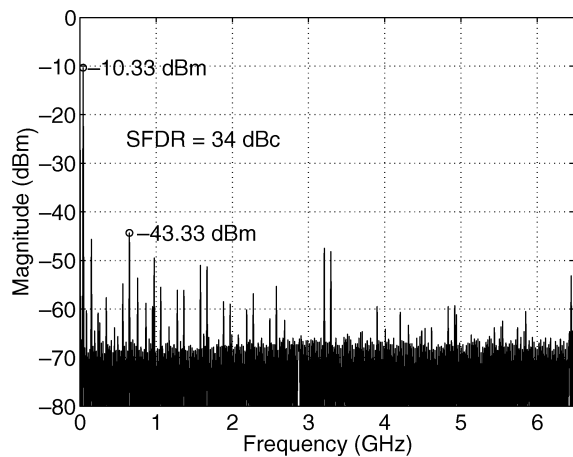


Fig. 6. Spectrum analyzer output of the DDS at 13 GHz with a frequency control word of 1. The SFDR is 34 dBc.

measured maximum clock frequency of 13 GHz correlated with simulation results. The DDS was able to synthesize outputs up to 6.5 GHz in 128 steps of 50.781 25 MHz per step. The entire DDS test chip power consumption was measured at 5.42 W.

With an FCW of 1 and a 13-GHz clock, the DDS had an output frequency of 50.781 25 MHz as shown in Fig. 5. At this frequency, the SFDR was measured to be 34 dBc, as shown in spectrum analyzer output of Fig. 6. At the maximum FCW of 128 and a 13-GHz clock the DDS operates as a divide by two circuit with a 6.5-GHz output, with an SFDR of 50 dBc. Using automated test software, the SFDR of the DDS was measured over the whole range of FCWs with a 13-GHz clock input. The sweep of SFDR versus FCW is shown in Fig. 7. The measured SFDR was better than 30 dBc over most of the FCWs. The worst case SFDR was 26.67 dBc at an output frequency of 6.389 775 GHz, which is an FCW of 126. The measured worst case SFDR was 1.73-dBc lower than in the simulations that did not take nonlinearities from the DAC into account.

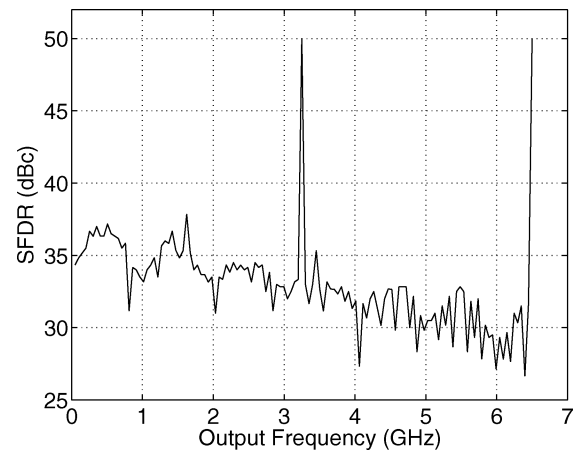


Fig. 7. Plot of the DDS SFDR as a function of the frequency control word at a 13-GHz clock rate. The SFDR peaks at multiples of  $f_{clk}/4$  were predicted by simulation of this phase conversion scheme.

#### IV. CONCLUSION

A sine-output DDS circuit with 1646 transistors was designed and fabricated using InP DHBT technology [1]. The DDS uses a ripple-carry accumulator without intermediate pipeline stages in order to reduce power consumption. The DDS is also ROM-less, instead using digital logic for phase conversion. This method is well-suited for a DDS with a relatively narrow bit width.

The DDS test chip operated up to a maximum clock frequency of 13 GHz, with a maximum synthesized output of 6.5 GHz. SFDR was measured over all FCWs and generally ranged from 34 dBc at low FCWs to 26.67 dBc at high FCWs. The measured power consumption for the test chip was 5.42 W.

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