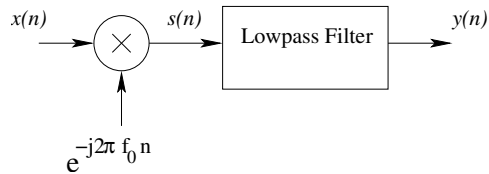
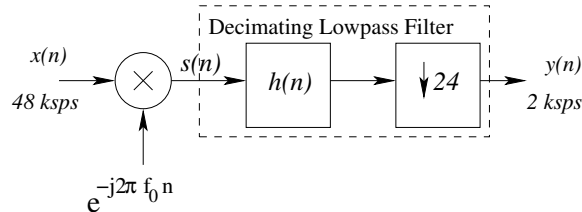


ECE-486 Homework 10, Spring 2009

1. The complex demodulator illustrated below operates at a fixed sample rate of $F_s = 48$ ksp/s. The value of f_0 and the lowpass filter bandwidth were selected to examine the band of frequencies between 12 and 13 kHz.



This problem involves the integration of a “downsampler” into the design as shown below. The sample rate at the output of the system is to be reduced to 2 ksp/s.



- Assume that $f_0 = 12.5/48$. Identify the discrete-time frequencies for the signal $s(n)$ which are associated with the input frequencies ranging from 12 kHz to 13 kHz. These frequencies will form the passband of the decimation filter $h(n)$.
 - Identify all discrete-time frequencies for the signal $s(n)$ which must be removed by the decimation filter in order to avoid aliasing onto the 12 kHz to 13 kHz band. These frequencies will form the stop-band for the decimation filter.
 - Design a minimum-order linear-phase lowpass filter which meets your passband and stopband requirements. Assume that passband ripple must remain below ± 0.2 dB, and all aliased frequencies must be attenuated by at least 80 dB. Describe how you designed your filter, and give the number of filter coefficients. Provide a plot of the magnitude response for your design.
 - Assuming that a (non-decimating) IIR filter is used, find the minimum filter order required to achieve the same specifications as those used for part 1c. Compare the computational costs (in multiplications per second) of the FIR and IIR implementations.
 - Now assume that that FIR filter of part 1c is to be implemented with the decimator in a polyphase structure. That is, 24 separate FIR filters with impulse responses $p_0(n), p_1(n), \dots, p_{23}(n)$ are to act in parallel. Draw a sketch of the Polyphase structure. Describe how the impulse response $p_0(n)$ is determined. On a single plot, show the magnitude of the (discrete-time) transfer functions of the first four polyphase filters, $P_0(f), P_1(f), P_2(f),$ and $P_3(f)$.
2. A discrete-time signal was acquired using a sampling frequency of $F_s = 100$ ksp/s, and contains a signal of interest in the band of frequencies from DC to 900 Hz. Design a decimator to reduce the sample rate by a factor of $D = 50$ to $F_{s2} = 2$ ksp/s. Implement the decimation in a single stage, allowing ± 0.1 dB of gain within the DC-900 Hz band. Any other signals which will alias to the DC-900 Hz band should be attenuated by at least 80 dB.

Calculate the number of multiplications per second required by your decimator. (My answer: about 3.2 Million... or 1.6 Million if the linear-phase symmetry of the filter coefficients is exploited.)

3. Now assume that the decimator of problem 2 is to be implemented in two stages, The first stage is to reduce the sample rate by a factor of $D_1 = 10$ to 10 ksp/s, and the second stage should decimate this output by a factor of $D_2 = 5$ to obtain the output sequence at the 2 ksp/s rate. In your design, allow ± 0.05 dB of gain within each stage over the DC-900 Hz band.

Calculate the number of multiplications per second required by your 2-stage decimator. (My answer: about 750,000... or roughly half of that if the linear-phase symmetry of the filter coefficients is exploited.)