

# Continuous Gain Calibration of Parallel Delta Sigma A/D Converters

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**Abstract** – A method to correct for gain errors in each channel of a parallel delta-sigma ( $\Pi\Delta\Sigma$ ) converters in real-time is presented. The calibration technique requires an additional channel that is linearly dependant on  $\Pi\Delta\Sigma$  channels used. By introducing the redundancy in a system, the adaptive LMS algorithm can be used to correct for gain errors within the channels. Using a 16-channel  $\Pi\Delta\Sigma$  converter with 4th order delta-sigma modulators and oversampling rate of 6, the simulation results show a 90 dB reduction in unwanted tones caused by 1% gain mismatch.

**Keywords** – parallel delta sigma converters, gain correction.

## I. INTRODUCTION

Many systems in communications and imaging require high-speed, high-resolution and wide bandwidth Analog-to-Digital Converters (ADCs). These are often implemented using pipeline multistage ADC architectures. As CMOS technologies are scaled to smaller geometries, component matching becomes increasingly difficult, which in turn limits resolution of pipeline architecture converters to approximately 10-12 bits. To increase linearity of Nyquist-rate converters different calibration techniques have been proposed and exploited [1–3]. Alternative converter architectures offer high resolution but have limited bandwidth. These include oversampling delta-sigma ( $\Delta\Sigma$ ) ADCs. Delta-sigma ADCs offer resolutions greater than 18-bits, require mostly digital circuitry and, compared to the Nyquist rate converters, they don't rely on high precision analog components [4]. The drawback of  $\Delta\Sigma$  ADCs is the need for high oversampling rate in order to get high linearity. These converters are often used in applications with low bandwidth requirements, such as digital audio. To keep the high linearity that  $\Delta\Sigma$  ADCs offer, and increase the bandwidth of the converter,  $\Delta\Sigma$  modulators can be placed in parallel [5–9]. The parallel  $\Delta\Sigma$  ( $\Pi\Delta\Sigma$ ) architectures provide one method of trading circuit complexity for increased resolution or bandwidth.

Even with  $\Pi\Delta\Sigma$  ADC architecture, the required high-speed and high-resolution cannot be obtained due to channel mismatches that degrade the overall performance of the converter [6, 10, 11]. An offline calibration technique for  $\Pi\Delta\Sigma$  converters has been reported in [12]. Under this technique, each individual path of the  $\Pi\Delta\Sigma$  modulator is taken offline to quantize a set of known calibration voltages. These values are used to

determine a set of calibration channel weights to be used in recombining the channels. The 'weights' are then implemented in each path using a digital  $\Delta\Sigma$  modulator.

In this paper, a continuous calibration technique is presented that removes gain mismatches between the channels without interrupting the operation of the  $\Pi\Delta\Sigma$  converter. The calibration technique requires an extra channel that is linearly dependent on  $\Pi\Delta\Sigma$  channels used. This redundancy in a system allows for gain errors within the channels to be successfully corrected. Calibration is demonstrated using a 16-channel  $\Pi\Delta\Sigma$  ADC in which each channel contains a 4<sup>th</sup> order modulator. The resulting  $\Pi\Delta\Sigma$  structure operates using a clock which is 6 times faster than that of a Nyquist rate converter, but achieves a resolution comparable to a conventional  $\Delta\Sigma$  modulator with an OSR of 46.

## II. OVERVIEW OF PARALLEL $\Delta\Sigma$ ARCHITECTURE WITH OVERSAMPLING

A parallel  $\Delta\Sigma$  ADC architecture was reported in [6], as a method of implementing Nyquist rate converters. Later the concept of  $\Delta\Sigma$  channels operating in parallel without time-interleaving was extended to oversampling converters [9]. For a conventional  $\Delta\Sigma$  ADC implemented using an  $L^{\text{th}}$  order delta-sigma modulator, each time the oversampling ratio is doubled, the effective number of bits is increased by  $L + 1/2$  [4]. Similar analysis can be applied to oversampled parallel  $\Delta\Sigma$  ADCs. If oversampling is employed on a parallel  $\Delta\Sigma$  converter, for an M-channel system with an oversampling ratio of D, same performance can be achieved as a conventional  $\Delta\Sigma$  converter with an oversampling ratio of  $M \times D$ . However, there is a  $\frac{1}{2}\log_2(M)$  penalty that is associated with parallel structures [9].

Figure 1 shows the oversampling  $\Pi\Delta\Sigma$  architecture. The M parallel channels have an input sequence  $x[n]$  applied simultaneously. Each channel is modulated by a distinct  $\pm 1$  sequence  $s_r[n]$ . An identical, but delayed and downsampled, copy of this signal  $p_r[n]$  is later used to (digitally) demodulate the channel. The remainder of the channel consist of a conventional  $L^{\text{th}}$  order  $\Delta\Sigma$  modulators with a decimating lowpass filter  $H(z)$ . However, the bandwidth associated with  $H(z)$  is significantly narrower than that of the conventional converter. Aside from

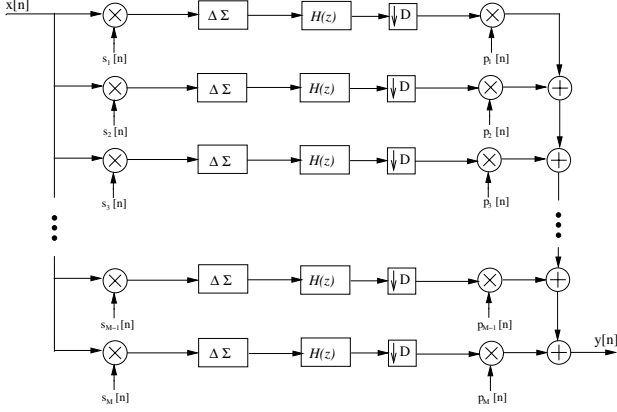


Fig. 1. Parallel  $\Delta\Sigma$  A/D converter architecture.

the selected modulation sequence, all  $\Pi\Delta\Sigma$  channels are identical. The (de)modulation sequences  $s_r[n]$  and  $p_r[n]$  are found using an  $M \times M$  Hadamard matrix  $\mathbf{H}$  and are referred to as Hadamard modulation sequences. The Hadamard matrix is defined by

$$H_r = \begin{bmatrix} H_{r-1} & H_{r-1} \\ H_{r-1} & -H_{r-1} \end{bmatrix}, \quad H_0 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \quad (1)$$

Each row of Hadamard matrix corresponds to one period of the  $r^{th}$  channel's demodulation sequence,  $p_r[n]$ . Finding modulation sequence  $s_r[n]$  for oversampled  $\Pi\Delta\Sigma$  converters involves repeating every row element in the Hadamard matrix  $D$  times, where  $D$  is the oversampling rate [9]. Each channel will be multiplied by different sequence of alternating  $\pm 1$  values. The first channel is always multiplied by a sequence of ones, which doesn't alter the input sequence  $x[n]$  and therefore first channel looks like a conventional  $\Delta\Sigma$  converter with reduced bandwidth.

### III. PROPOSED CALIBRATION ALGORITHM

The architecture described in Section II can give high-speed and high-resolution results only if all of the  $M$ -channels are identical and Hadamard modulation sequences are in-sync. Channel mismatches are usually caused by variations in the manufacturing process.

Besides the noidealities that come with conventional  $\Delta\Sigma$  modulator,  $\Pi\Delta\Sigma$  modulators are sensitive to channel gain and offset mismatches and Hadamard modulation level errors, [6, 12]. The calibration technique discussed here can correct for gain errors introduced in a channel. Figure 2 shows a model used to analyze gain and offset errors in the  $r^{th}$  channel. To simplify the analysis, we assume that the oversampling ratio  $D$  is one and therefore  $D$ -fold downsampler can be ignored. Also, to simplify the analysis, the delta-sigma modulator is replaced by its signal transfer function (a constant delay) [6]. The

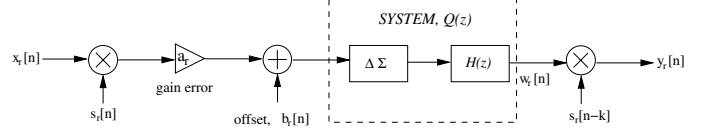


Fig. 2. Model for gain and offset errors in the  $r^{th}$  channel.

Hadamard modulation sequences for  $s_r[n]$  and  $p_r[n]$  become  $s_r[n]$  and  $s_r[n-k]$ , respectively; where  $k$  is the delay introduced by the system  $Q(z)$ . System  $Q(z)$  includes sigma-delta modulator and low-pass filter  $H(z)$ . Now a general expression for the output of the  $r^{th}$ -channel before demodulation,  $w_r[n]$ , including channel gain and offset errors is given by

$$w_r[n] = \sum_{k=0}^{\infty} q[k] a_r x[n-k] s_r[n-k] + b_r \quad (2)$$

Calibration may be realized by implementing an extra channel in the system that contains information about other channels. This is accomplished by modulating the input into a 'calibration' channel with a sequence of  $\pm 1$  that is a linear combination of the sequence used for other channels in the system. This provides information about each channel in the system and doesn't contain errors associated with those channels. With this redundant information we solve for errors in each of the original channels. Equation (3) shows an expression for modulation sequence of the 'calibration' channel. The coefficients  $\alpha_1, \alpha_2 \dots \alpha_M$  are selected so that the sequence  $s_c[n]$  contains only  $\pm 1$  terms. This allows for calibration channel to be identical in implementation as other channels used in the system. Also, calibration channel does not require demodulator.

$$\begin{aligned} s_c[n] &= \alpha_1 s_1[n] + \alpha_2 s_2[n] + \alpha_3 s_3[n] + \dots \\ &\quad + \alpha_{M-1} s_{M-1} + \alpha_M s_M[n] \\ &= \sum_{r=1}^M \alpha_r s_r[n]. \end{aligned} \quad (3)$$

The coefficients  $\alpha_r$  must be non-zero, and should preferably have equal magnitude, so that each  $\Pi\Delta\Sigma$  channel is given equal importance. A computer search for a 16-channel architecture yielded valid solutions with each  $\alpha_r = \pm 0.25$ , producing a sequence  $s_c[n]$  which only takes values  $\pm 1$ . Knowing modulation sequence for 'calibration' channel, we can now form an expression for the output of  $w_c$ , with gain and offset errors included. For the 'calibration' channel we have,

$$w_c[n] = \underbrace{\sum_{r=1}^M \sum_{k=0}^{\infty} q[k] \alpha_r a_c x[n-k] s_r[n-k]} + b_c \quad (4)$$

The expression over the brace can be written in terms of the  $\Pi\Delta\Sigma$  channel outputs  $w_r[n]$  described by (2), and therefore

(4) becomes

$$\begin{aligned}
 w_c[n] &= \sum_{r=1}^M \frac{\alpha_r a_c}{a_r} (w_r[n] - b_r) + b_c \\
 &= \sum_{r=1}^M \frac{\alpha_r a_c}{a_r} w_r[n] - \sum_{r=1}^M \frac{\alpha_r a_c}{a_r} b_r + b_c. \quad (5)
 \end{aligned}$$

The first term of (5) contains information about gain errors of each channel ( $a_r$ ), and the second term contains the sum of offsets contained in each of the channels, including ‘calibration’ channel. Equation (5) can be rewritten

$$w_c[n] = \beta_0 + \sum_{r=1}^M \beta_r w_r[n] \quad (6)$$

where  $\beta_r = \alpha_r a_c / a_r$  for  $r = 1, 2, \dots, M$  and  $\beta_0 = b_c - \sum_{r=1}^M \beta_r b_r$ .

Any least-squares procedure can be used to find coefficients  $\hat{\beta}_r$  which best predict the known calibration channel output  $w_c[n]$  from the given  $M - \Pi\Delta\Sigma$  channel outputs. Dividing these coefficients by  $\alpha_r$  provides an estimate  $\hat{\beta}_r / \alpha_r \approx a_c / a_r$  which is proportional to the reciprocal of the unknown gain for each channel. Scaling the  $\Pi\Delta\Sigma$  converter output channels by these values effectively removes the gain mismatches.

In solving for  $\hat{\beta}_r$ , a matrix formulation may be used. Given  $N$  samples of the  $\Pi\Delta\Sigma$  channel outputs, (6) can be rewritten

$$\mathbf{W} \vec{\beta} = \vec{w}_c \quad (7)$$

where  $\vec{w}_c$  is the  $N \times 1$  vector of ‘calibration’ channel outputs,  $\vec{\beta} = [\beta_0 \beta_1 \dots \beta_M]^T$ , and  $\mathbf{W}$  is an  $N \times (M + 1)$  matrix with first column given by 1s, and  $(r + 1)^{th}$  column given by the  $r^{th}$  channel output. A least-squares solution of (7) then provides  $\hat{\beta}$ . Alternatively (and more realistically) an adaptive LMS algorithm may be used to find  $\hat{\beta}$ .

Figure 3 shows a parallel  $\Delta\Sigma$  architecture modified to include continuous gain calibration. Before demodulation, the outputs of all channels are routed to adaptive filter algorithm for finding least squares solution [13]. The result is then scaled by the known  $1/\alpha_r$  values to obtain gain correction terms for each channel,  $c_r = \beta_r / \alpha_r$ .

#### IV. SIMULATION RESULTS AND CONCLUSIONS

The calibration scheme was implemented and simulated. A 16-channel  $\Pi\Delta\Sigma$  converter was modelled in which each channel contains a 4<sup>th</sup> order modulator with oversampling rate (OSR) of 6. Multi tone test signals were applied at the input to demonstrate wide bandwidth capabilities of  $\Pi\Delta\Sigma$  converter.

To have a ‘calibration’ channel as a linear combination of other channels, values of  $\alpha_r$  were set to  $\pm 0.25$  as identified by computer search. Gain error mismatches of  $\pm 1\%$  were simulated. Gain correction terms for each channel were calculated

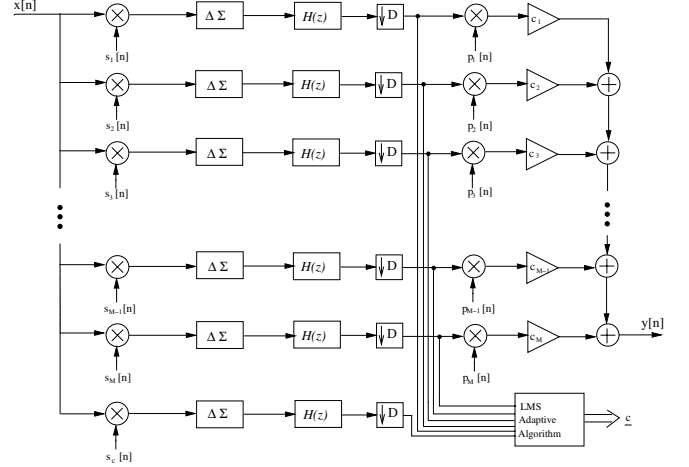
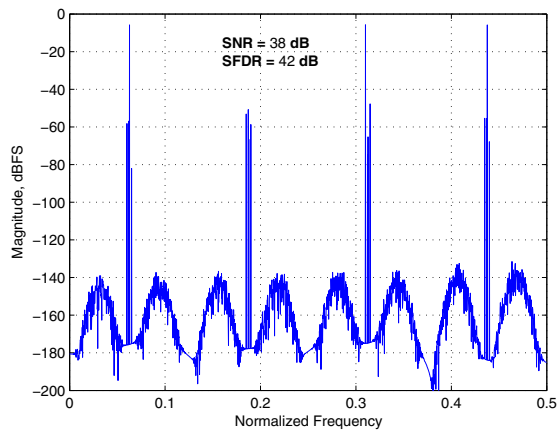


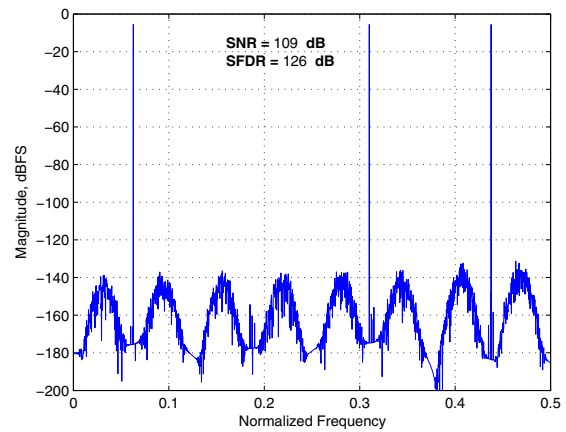
Fig. 3. Parallel  $\Delta\Sigma$  converter architecture modified to include gain calibration.

using an LMS algorithm based on 4096 samples of a random input signal. Figure 4 shows simulation results when system was not calibrated. Introduced gain errors cause an SNR performance of 38 dB which corresponds to a 6-bit converter. Figure 5 shows simulation results for calibrated system. All gain errors present within each channel were successfully cancelled by the calibration algorithm. After calibration, the SNR of the converter improves to 109 dB, which corresponds to an 18-bit device.

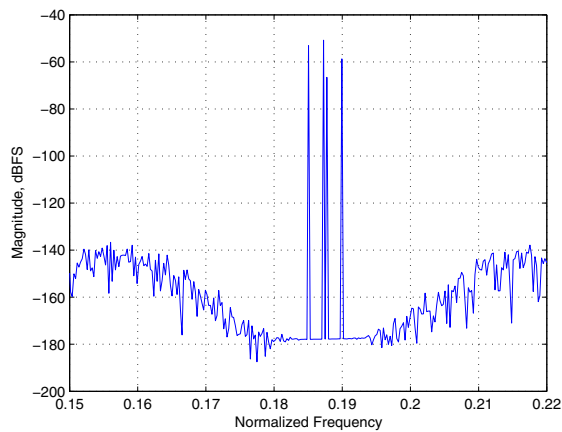
A continuous calibration technique to eliminate gain error mismatches in  $\Pi\Delta\Sigma$  converters has been demonstrated. Simulation results show 90 dB of improvement in SFDR and 70 dB of improvement in SNR for a 16-channel  $\Pi\Delta\Sigma$  converter with oversampling rate of 6. These are promising results for implementing continuous calibration for gain channel mismatches. Further work is required to find techniques to remove offset mismatches in real-time.



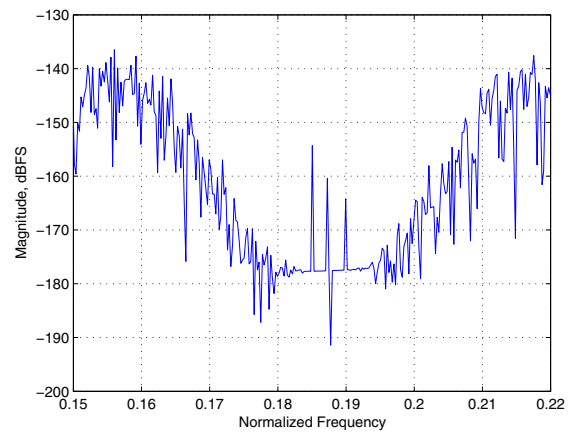
(a)



(a)



(b)



(b)

Fig. 4. Simulation results for: (a) Uncalibrated 16-channel  $\Pi\Delta\Sigma$  converter with 1% gain mismatch error and  $OSR = 6$  and (b) zoomed portion of the spectrum showing gain error tones. Frequencies are normalized by the decimated sample rate.

Fig. 5. Simulation results for: (a) Calibrated 16-channel  $\Pi\Delta\Sigma$  converter with 1% gain mismatch error and  $OSR = 6$  and (b) zoomed portion of the spectrum showing gain error tones. Frequencies are normalized by the decimated sample rate.

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