

Continuous Digital Calibration of Pipeline A/D Converters

Alma Delić-Ibukić, Donald M. Hummels

Department of Electrical and Computer Engineering, University of Maine
5708 Barrows Hall 113, Orono, ME 04469, USA

Abstract – A continuous digital calibration technique for pipeline Analog-to-Digital Converters (ADCs) is presented. The scheme utilizes an existing digital calibration algorithm and extends it to work in real-time. This is accomplished by introducing two additional stages at the end of the pipeline which are used only during calibration process. Calibration scheme is transparent to the overall system and is demonstrated using a 14-bit ADC, with 1-bit per stage architecture and 18 identical stages (including two additional stages for calibration). Dominant static errors in a pipeline are successfully corrected by the proposed calibration. Simulation results show more than 2-bits improvement in the number of effective bits and more than 20 dB improvement in the dynamic range of the converter.

Keywords – Pipeline analog-digital conversion, digital calibration.

I. INTRODUCTION

Applications such as wireless communications, image recognition and medical instrumentation require high-speed, high-resolution Analog-to-Digital Converters (ADCs). High-speed and high resolution converters are often implemented using pipeline multistage ADC architectures. The hardware complexity of the pipeline converter is proportional to the number of bits resolved. Monolithic, high-resolution pipeline ADCs are difficult to obtain due to extraordinary component matching requirements. Component matching becomes increasingly difficult as CMOS technologies are scaled to smaller geometries. Without using some form of calibration, standard CMOS process technologies limit the resolution of pipeline architecture to approximately 8-10 bits.

Different calibration techniques have been proposed to improve speed and linearity of ADCs. Most calibration techniques fall into one of three categories: calibration performed in a factory, calibration performed every time the converter is powered up (foreground calibration) [1–4], and continuous calibration [5–7]. Calibrations performed in a factory, such as capacitor trimming, are one time events. Before packaging the ADC, capacitors are trimmed to accomplish the best possible capacitor matching and therefore improve the linearity of the ADC. Because the calibration is performed only once, it cannot take into account changes in the environment that may affect performance of the converter. In contrast, “foreground calibration” allows re-calibration at power up, but requires a converter to be off-line while (re)calibration is in progress. The

ideal type of calibration is “continuous calibration” since the converter is in its normal mode of operation while being calibrated. Continuous calibration is done in the background without interrupting the ADC operation. Environmental and internal changes are continuously taken into account and corrected. Several analog continuous calibration schemes have been reported in the literature [5, 6]. Calibration techniques based on analog schemes are generally difficult to scale to new process technologies due to the increase in sub-threshold and gate leakage currents and reduced power supply voltage [8].

This paper expands on a digital calibration algorithm developed in [1] and derives a continuous digital calibration scheme targeted for pipeline ADCs [9]. This calibration technique is completely digital, transparent to the overall system and applicable to multiple bits per stage pipeline architectures. It is implemented in VHDL and requires two additional stages located at the end of the pipeline. The extra stages are only used during the calibration process. The calibration technique is demonstrated using a 14-bit ADC with 1-bit per stage pipeline architecture and interstage gains less than two. DAC and interstage gain errors due to the charge injection and capacitor mismatch are corrected successfully.

II. PROPOSED REAL-TIME CALIBRATION OF PIPELINE CONVERTERS

A conventional pipeline converter architecture is shown in Figure 1. Each stage in the pipeline serves two purposes: to provide q_i , the coarse resolution digital representation of the input voltage and to provide the next stage in the pipeline with r_i , the difference between the input voltage and analog form of q_i . This residual voltage, r_i , is passed on to the subsequent stages for quantization in an attempt to improve the digital representation of the input. All q_i 's are collected in the digital encoder block where they are combined properly to achieve a higher resolution representation of the input voltage X . Digital calibration schemes measure the error contributions of the stage in the digital domain. The measured gain and reference voltage variations are used to form the ADC output code [1, 3, 7, 10]. The accuracy of the calibration depends on how well the errors are measured in the digital domain. To digitally correct the ADC output code, modifications need to be

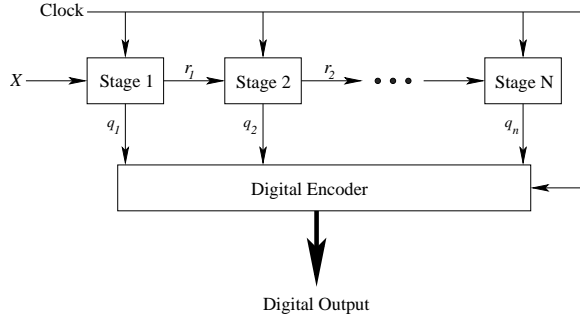


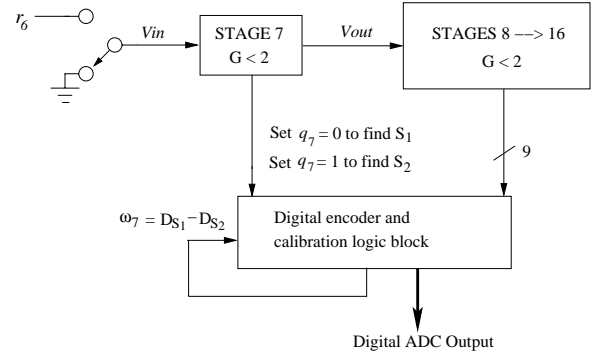
Fig. 1. Generic Pipeline ADC block diagram.

made to the digital encoder block. Section A describes an off-line digital calibration scheme developed in [1]. This technique forms the basis for the proposed continuous digital calibration scheme discussed in Section B.

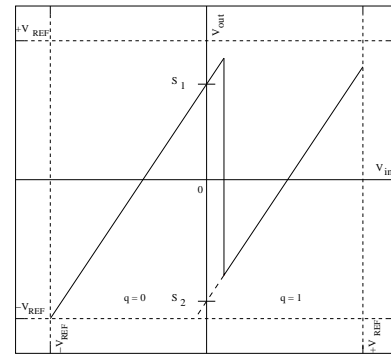
A. Off-line Calibration

Figure 2 illustrates the foreground calibration process developed in [1] for a single stage of a pipeline ADC. The illustrated case is based on the implementation of a 14-bit ADC with 16 identical stages, interstage gains less than two, and 1-bit per stage topology. Gains less than two are chosen for all 16 stages so the output of each stage does not saturate the remaining stages. Calibration begins with the least significant stages (the end of the pipeline) and progresses toward the most significant stages. For example, to calibrate stage 7, we must assume that stages 8-16 have already been calibrated, or have been fabricated to sufficient accuracy that calibration is not needed. Figure 2(a) shows the off-line digital calibration applied to the seventh stage of a 16-stage architecture. Figure 2(b) shows residual characteristics for the stage being calibrated with the threshold offset, interstage gain and DAC errors. Following calibration of the seventh stage, the process continues with the sixth stage, and so on until the first stage is reached and the calibration of the converter is complete.

Pipeline error characteristics often show discontinuities associated with the change in the output of the sub-ADC comparators. The residual error shown in Figure 2(b) consists of two segments (for $q=0$ and $q=1$) and the transition between the segments is determined by the comparator threshold. The goal of digital calibration is to make sure that for the same input voltage, the digital ADC output remains unchanged regardless of which segment is selected by the sub-ADC comparator of the stage. To assure this consistency, the converter output is examined for a stage input set to zero volts, where the stage is forced to operate on each of the segments. Setting $q_7=0$ with $V_{in}=0$, forces Stage 7 to operate on the left segment, producing output residual voltage S_1 . S_1 is quantized by the remaining pipeline stages (stages 8, 9, 10, ..., 16), producing digital output D_{S_1} . Setting $q_7=1$ ($V_{in}=0$) forces Stage 7 to operate on the



(a) Off-line digital calibration applied to the seventh stage.



(b) Residual error plot of 1-bit per stage architecture with errors.

Fig. 2. Pipeline ADC with off-line digital calibration applied to the seventh stage.

right segment, producing residual voltage S_2 and in turn digital output D_{S_2} . The equation for the digital output of the N -stage converter is given by:

$$D = q_1 (G_1 G_2 G_3 \dots G_{N-1}) + q_2 (G_2 G_3 G_4 \dots G_{N-1}) \dots + q_{N-1} G_{N-1} + q_N \quad (1)$$

Each stage output bit is given a weight indicated by the gain products given in parenthesis. Most pipeline ADCs use ‘nominal’ design gains to construct the digital output. This approach is correct only if the converter is free of any gain or sub-DAC errors. If the implemented gain is different from the design value, or if sub-DAC errors exist, there will be error in the ADC output. Making these weights programmable is the idea behind the foreground digital calibration technique discussed in [1]. Equation (1) can be re-written in terms of these programmable weights,

$$D = \sum_{i=1}^N q_i \omega_i, \quad (2)$$

where q_i is the output bit for stage i and N is the number of stages used and ω_i is the programmable term associated with the stage. Once found, the correction term ω_i is fed back to the digital encoder and calibration logic block. This value is a weight associated with the bit of the stage being calibrated and it carries the information about the interstage gain and sub-DAC errors.

B. Real-Time Digital Calibration Scheme Development

Pipeline architecture ADCs rely on a two-phase, non-overlapping clock signals with phases denoted ϕ_1 and ϕ_2 . All the odd stages in a pipeline sample during phase ϕ_1 and present the valid residue output to the next stage during ϕ_2 . All the even stages work on the opposite clock phase. This allows for all stages in the pipeline to operate concurrently.

A proposed real-time digital calibration based on the algorithm derived in [1] was realized using two extra stages located at the end of the pipeline. These two extra stages are active only during calibration. Two additional stages allow for a calibration sample to be introduced in the pipeline and still maintain the normal operation of the converter. Table I shows propagation of samples through the pipeline during the calibration process. Table I is based on a 14-bit ADC with 1-bit per stage topology, 16 identical stages plus two additional stages for calibration (total of 18 pipeline stages), and gains less than two. Numbers 1 through 18 indicate pipeline stages.

Two-phase, non-overlapping clocks are indicated by ϕ_1 and ϕ_2 . Values -1, 0, 1, 2, ..., correspond to sample number being acquired by a given stage, and $D_{-1}, D_0, D_1, D_2, \dots$, correspond to digital representation of the sample produced at the output of a given stage. For example, sample number 4 is processed by Stage 1 on a phase ϕ_1 and its digital representation as well as a residual is available on ϕ_2 . At this time, Stage 2 is ready to acquire this residual voltage. Stage 2 produced its coarse digital representation on the following ϕ_1 . This goes on until all 16 stages in a pipeline have coarse digital representation of sample number 4 available for the digital encoder and calibration logic block where the corresponding digital value for the sample is obtained.

After the inherent pipeline delay, digital outputs become available on every ϕ_1 . This is considered a normal converter operation and it must be preserved during the calibration process. When calibrating a stage using the digital calibration algorithm derived in [1], the stage being calibrated needs to be taken off line which in turn will interrupt normal operation of the converter. To avoid this, two extra stages are added at the end of the pipeline. This allows one conversion cycle to be freed for calibration purposes and at the same time maintain normal converter operation.

When calibrating, all samples at the various stages of the pipeline are shifted by two stages down in the pipeline. The two extra stages at the end of the pipeline make sure the converter maintains a full 14-bit output during the calibration cy-

cle. Table I shows the calibration of Stage 5. An artificial sample is introduced at the beginning of the pipeline denoted "T". At the same moment, sample number 3 is shifted as an input into Stage 3. This means that Stage 3 for this instant acts as a first stage of the pipeline and last stage for this sample will be Stage 18. Sample number 2, which should be at the calibration moment occupying Stage 3, is now shifted two stages down to the next free odd stage, Stage 5 and so on. The last sample that needs to be shifted at the calibration instant is located in Stage 14. Instead of going to Stage 15 on the next clock phase, it will be routed to Stage 17. The same shift is used for the coarse digital outputs for these samples. The only difference is the clock phase on which shift of the digital counterpart occurs. It can be seen from Table I that all samples still propagate through 16 stages with no time delay introduced and no lost samples.

Due to the pipeline shift, certain considerations need to be taken into account when forming the digital output code during the calibration process. With all identical stages Equation (1) becomes

$$D = q_1 G^{N-1} + q_2 G^{N-2} + q_3 G^{N-3} \dots + q_{N-2} G^2 + q_{N-1} G + q_N \quad (3)$$

From (3) it can be seen that there is a weight associated with each bit of the stage. When calibration occurs, Stage 3 becomes the first stage of the pipeline, and should be given weight G^{N-1} . Similarly the weights associated with the other stages need to shift to reflect the reorganization of the pipeline. The weights for Stages 1, 2, 3, ..., need to be available at location of Stages 3, 4, 5, ..., respectively for the correct formation of the final digital output during the calibration.

III. RESULTS AND COMPLEXITY OF THE DEVELOPED CALIBRATION TECHNIQUE

The calibration scheme was implemented using Verilog HDL and simulated using the Verilog-XL simulator. The real-time calibration technique was derived for a 14-bit ADC with 1-bit per stage architecture implemented using 18 identical stages (including two extra stages for calibration purposes). To verify that the derived real-time calibration technique works, it was necessary to model a pipeline stage in Verilog HDL and also to control gain, threshold and sub-DAC reference voltages of the stages being calibrated. To imitate the accurate behavior of the pipeline ADC, fully digital odd and even stages were created using Verilog HDL. Gain, threshold and sub-DAC reference voltages were made as controllable variables at the input of each simulated pipeline stage. Nominal gain for all 18 stages was set to 1.81. The input range (V_{FS}) for this converter was set to ± 1.12 V and the reference voltage for the converter was set to $V_{REF} = 1$ V. A sampling frequency of 51.2 MHz was used and the sinusoidal test signal was set to 150 KHz with the amplitude at -1 dBFS (994 mV). Errors were introduced in all 18 stages (including two extra stages used during calibration) of the converter and 1024 samples were used. Capacitor

TABLE I
SAMPLE PROPAGATION THROUGH THE PIPELINE FOR THE PROPOSED REAL-TIME DIGITAL CALIBRATION TECHNIQUE.

Stage	Increasing time \longrightarrow																										
	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1		
1	1	D_1	2	D_2	T	D_T	4	D_4	5	D_5	...																
2	D_0	1	D_1	2	D_2	T	D_T	4	D_4	5	D_5	...															
3	0	D_0	1	D_1	3	D_3	T	D_T	4	D_4	5	D_5	...														
4	D_{-1}	0	D_0	1	D_1	3	D_3	T	D_T	4	D_4	5	D_5	...													
5	-1	D_{-1}	0	D_0	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...												
6		-1	D_{-1}	0	D_0	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...											
7			-1	D_{-1}	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...										
8				-1	D_{-1}	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...									
9					0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...								
10						0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...							
11					-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...						
12						-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...					
13							-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...				
14								-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...			
15									-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	...		
16										-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C_5}	4	D_4	5	D_5	D_5	
17											-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3							
18												-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3						

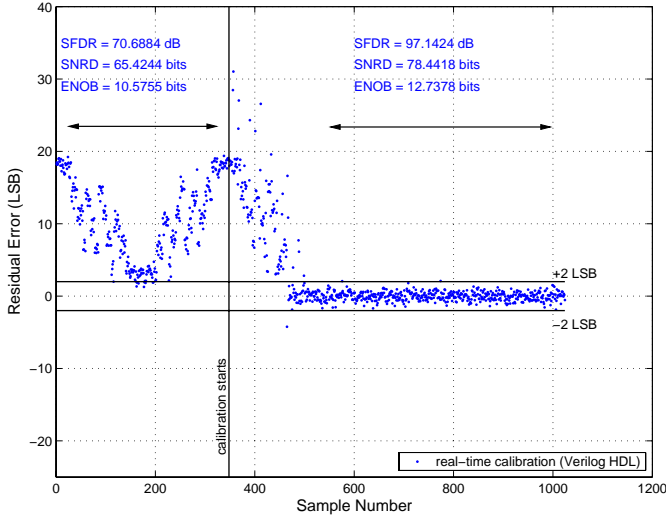


Fig. 3. Residual error characteristics for a simulated ADC with applied real-time calibration and errors introduced in all 18 stages of the converter.

matching error between 0.1-0.5% was simulated. For threshold voltage variations, a maximum error of up to 10% of V_{FS} was simulated. Figure 3 shows the residual error characteristics for a simulated 14-bit ADC calibrated in a real-time. Before activating the calibration signal, the behavior of the ADC with the error contributions in all 16 stages is presented. The ADC behaves as a 10-bit converter before calibration and as 12.7 bit converter after calibration. Once the calibration signal is activated, 154 clock cycles are needed for completion of the calibration process. At the sampling rate of 51.2 MHz this corresponds to $3\mu s$ to complete a calibration of 7 stages. The complexity of the digital logic required to implement the proposed calibration technique was evaluated using BuildGates Extreme synthesizer. Verilog modules were synthesized using

a ‘generic build’ command. This produces unoptimized digital logic necessary to implement the real-time calibration technique. Approximately 100,000 logic gates are needed to implement the derived calibration. For a minimum feature size of 135 nanometers the required area to implement the derived calibration logic is approximately $0.26 mm^2$, based on the ITRS report from year 2003 [11]. This is a fully digital logic design and therefore, the required area scales down easily with new process technologies.

IV. CONCLUSIONS

Different calibration techniques targeted to pipeline ADCs have been proposed in the literature and successfully implemented. Most of the reported calibration schemes rely on the converter being off line while calibrated or are analog in nature. Here we proposed a continuous digital calibration scheme targeted for pipeline ADCs. The scheme expands on a digital calibration algorithm developed in [1]. The proposed architecture is completely digital, transparent to the overall system and applicable to multiple bits per stage pipeline architectures. It is realized using two extra stages located at the end of the pipeline. These stages are used only during calibration process. A hardware model was designed using VHDL and it was effective in showing the success of the proposed technique. For a simulated ADC, the number of effective bits was improved by at least 2-bits and the dynamic range of the converter was improved by at least 20 dB. The required area to implement the necessary digital logic scales down easily with the new process technologies, making it an attractive solution for improving resolution of pipeline converters.

[1] A. N. Karanicolas, H.-S. Lee, and K. L. Bacrania, “A 15-b 1-Msample/s digitally self-calibrated pipeline ADC,” *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 1207–1215, Dec. 1993.

- [2] H.-S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrated 15 bit CMOS A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 6, pp. 813–819, Dec. 1984.
- [3] H.-S. Lee, "A 12- 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 509–515, Apr. 1994.
- [4] I. E. Opris, L. D. Lewicki, and B. C. Wong, "A single-ended 12-bit 20 Msample/s self-calibrating pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1898–1903, Dec. 1998.
- [5] J. M. Ingino and B. A. Wooley, "A continuously calibrated 12-b, 10-MS/s, 3.3v A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 12, pp. 1920–1931, Dec. 1998.
- [6] J. Ming and S. H. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1489–1497, Oct. 2001.
- [7] T.-H. Shu, B.-S. Song, and K. Bacrania, "A 13-b 10-Msample/s ADC digitally calibrated with oversampling delta-sigma converter," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 443–452, Apr. 1995.
- [8] A. Abo, "Design for reliability of low-voltage switched-capacitor circuits," Ph.D. dissertation, University of California, Berkeley, California, May 1999.
- [9] A. Delić-Ibukić, "Continuous digital calibration of pipeline A/D converters," Master's thesis, University of Maine, Orono, 2004.
- [10] U.-K. Moon and B.-S. Song, "Background digital calibration techniques for pipelined ADC's," *IEEE Transactions on Circuits and Systems-II*, vol. 44, pp. 102–109, Feb. 1997.
- [11] International Technology Roadmap for Semiconductors. [Online]. Available: <http://public.itrs.net>