

DIGITAL ARCHITECTURE FOR BACKGROUND CALIBRATION OF PIPELINE ADCs

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Abstract

Continuous digital calibration technique suitable for implementation in a fully monolithic pipeline analog-to-digital converter (ADC) is presented here. The technique utilizes the existing digital calibration algorithm and extends it to work in real-time. This is accomplished by introducing two additional stages at the end of the pipeline which allow for a conversation cycle to be freed for calibration purposes. Two additional pipeline stages are active only during calibration process. Digital architecture discussed here is transparent to the overall system and is demonstrated using a 14-bit ADC, with 1-bit per stage topology and 18 identical stages (including two additional calibration stages). Proposed scheme successfully correct the dominant static errors present in a pipeline. Simulation results show more than 2-bits improvement in the number of effective bits and more than 20 dB improvement in the dynamic range of the converter.

1 Introduction

Applications such as wireless communication and image recognition require high-speed, high-resolution Analog-to-Digital Converters (ADCs). These are often implemented using pipeline multistage ADC architectures. High-resolution pipeline ADCs are difficult obtain due to extraordinary component matching requirements. Component matching becomes increasingly difficult as CMOS technologies are scaled to smaller geometries. In current process technologies, capacitor matching of $\pm 0.1\%$ is achievable [1]. This process limitation restricts the achievable resolution of pipeline ADCs to roughly 10 bits. For higher resolution some form of calibration needs to be employed. Different calibration techniques have been proposed to improve speed and linearity of ADCs. Analog calibration schemes use analog signal path and extra analog circuitry to apply corrections to the stage being calibrated [2, 3]. With scaled technologies, analog switch capacitor components are getting more difficult to design. This is due to the increase in sub-threshold and gate leakage currents and reduced power supply voltage [4]. Digital calibration schemes measure the error contributions of the stage in digital domain [5–7]. Only extra digital circuitry is required. Digital schemes are more suitable for scaled technologies.

In this paper, we propose a continuous digital calibration

architecture targeted for pipeline ADCs [8]. The developed architecture is based on the calibration algorithm first reported in [5]. It is completely digital, transparent to the overall system and applicable to multiple bits per stage pipeline architectures. It is implemented in VHDL and requires two additional stages located at the end of the pipeline. The extra stages are only used during the calibration process. The calibration technique is demonstrated using a 14-bit ADC with 1-bit per stage topology and interstage gains less than two. Dominant static errors in a pipeline are successfully corrected.

2 One-bit Per Stage Pipeline A/D Converter

High speed, high resolution, low power ADCs are frequently based on a pipeline architecture. Using 1-bit per stage topology, a basic operation of the pipeline converter is described in Section 2.1. Section 2.2 describes the common error sources in a pipeline stage.

2.1 Architecture Overview

A pipeline converter architecture for 1-bit per stage topology is shown in Figure 1. Each stage in the pipeline provides the digital encoder block with the coarse resolution digital representation of the input voltage, q_i , and provides the next stage in the pipeline with r_i , the difference between the input voltage and analog form of q_i . This residual voltage, r_i , is passed on to the subsequent stages for quantization in an attempt to further improve the digital representation of the input. All q_i 's are collected in the digital encoder block where they are combined properly to achieve a higher resolution representation of the input voltage X .

A pipeline stage consists of a sample and hold (S/H) block, 1-bit analog-to-digital converter (sub-ADC), 1-bit digital-to-analog converter (sub-DAC), analog subtractor and a gain block. The quantization interval for a single 1-bit stage is given by V_{REF} . The sub-ADC block for this particular topology requires one comparator with a zero volt threshold. There are two valid digital outputs of the sub-ADC block, 0 or 1. The corresponding sub-DAC outputs for these two digital values are $-V_{REF}/2$ and $+V_{REF}/2$. The sub-DAC outputs are subtracted from the input and multiplied by the appropriate gain G . Ideally the gain should scale the residual error, r_i , to $\pm V_{REF}$, the input range of the subsequent stage.

The input voltage X can be represented in terms of the error voltage, e , and sub-DAC outputs. Equation 1 shows the

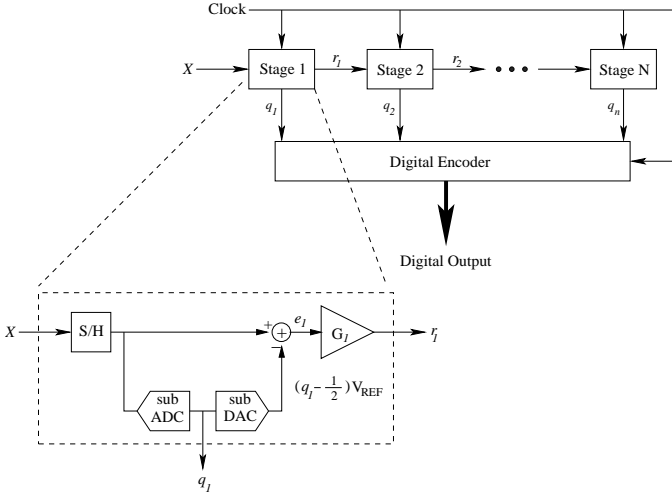


Figure 1: Block diagram of a pipeline ADC with 1-bit per stage topology.

representation of X in terms of the first stage error voltage, e_1 , and sub-ADC output, q_1 .

$$X = e_1 + \left(q_1 - \frac{1}{2} \right) V_{REF} \quad (1)$$

The first stage residual voltage, r_1 , can be written in terms of the corresponding values from the next stage in the pipeline.

$$r_1 = G_1 e_1 = e_2 + \left(q_2 - \frac{1}{2} \right) V_{REF} \quad (2)$$

Solving (2) for e_1 and making a substitution in (1) gives the input voltage, X , in terms of the quantized outputs of the first two pipeline stages.

$$X = \frac{e_2}{G_1} + \left(q_1 - \frac{1}{2} \right) V_{REF} + \left(q_2 - \frac{1}{2} \right) \frac{V_{REF}}{G_1} \quad (3)$$

The error voltage e_2 is, in turn, amplified and quantized by Stage 3, refining the representation of X . This process continues throughout the remaining stages of the pipeline. For the N -stage converter the input voltage X is represented in terms of the quantized outputs of the N stages and the error voltage e_N . Equation (4) shows this relationship.

$$\begin{aligned} X = & \frac{e_N}{G_1 G_2 G_3 \dots G_{N-1}} + \left(q_1 - \frac{1}{2} \right) V_{REF} \\ & \dots + \left(q_{N-1} - \frac{1}{2} \right) \frac{V_{REF}}{G_1 G_2 G_3 \dots G_{N-2}} \\ & + \left(q_N - \frac{1}{2} \right) \frac{V_{REF}}{G_1 G_2 G_3 \dots G_{N-1}} \end{aligned} \quad (4)$$

Equation (4) contains all required terms to form the digital output code for this N -stage converter. The digital output is given by:

$$\begin{aligned} D = & q_1 (G_1 G_2 G_3 \dots G_{N-1}) + q_2 (G_2 G_3 G_4 \dots G_{N-1}) \\ & \dots + q_{N-1} G_{N-1} + q_N \end{aligned} \quad (5)$$

From (5) it can be seen that the digital output is correct as long as the analog gains match the coefficients used in forming the digital output. Often, the gains are selected as power of two, making the hardware implementation of a digital encoder easy.

2.2 Sources of Error in Pipeline A/D Converters

Dominant static errors in a pipeline stage are sub-ADC, sub-DAC and interstage gain errors. Sub-ADC error can be fixed by modifying a pipeline stage and this is described in Section 2.2.1. Sub-DAC and interstage gain errors cannot be solved by implementing stage modifications alone. Rather, new techniques need to be derived to address these errors. Sub-DAC and gain errors are discussed in Sections 2.2.2 and 2.2.3.

2.2.1 Sub-ADC Error

Variability in threshold voltages introduce a comparator offset error. This error causes the residual of one stage to exceed the input range of the next stage. There are two ways to relax the comparator offset requirements: increase the quantization resolution of the stage and keep the interstage gain as a power of two, or keep the same number of bits per stage but reduce the interstage gain. Increasing the quantization interval of the stage, allows for the digital encoder block to remain the same because the interstage gain does not change. On the other hand, reducing the interstage gain adds complexity to the digital encoder block design.

When implementing the digital calibration, values used to form the ADC output code need to be modified. This requires alteration of the digital encoder block. If modification of the digital encoder is needed, then reducing the gain of the stage is the better choice of dealing with the comparator offset errors. The interstage gain reduction generally requires additional stages so that the resolution of the converter is not compromised. Equation (5) can be used to determine the relationship between the implemented value of G and the number of required stages. For example, to obtain a converter with a 14-bit resolution using identical stages, we set $D = 2^{14} - 1$ for all $q_i = 1$. Using $N = 16$ stages gives a value of $G = 1.81$, small enough to ensure that residual voltages will not saturate subsequent stages. If the interstage gain is less than two, the full scale voltage (V_{FS}) of the pipeline is no longer $\pm V_{REF}$. The full scale voltage for a converter with an arbitrary gain can be derived by solving for the input voltage V_{FS} which produces residual voltage V_{FS} at each stage of the pipeline. The following relationship between the interstage gain, G , and full scale voltage, V_{FS} , is derived:

$$\begin{aligned} G(V_{FS} - V_{DAC}) &= V_{FS}, \text{ where } V_{DAC} = \frac{V_{REF}}{2}. \\ V_{FS} &= \frac{G}{G-1} \left(\frac{V_{REF}}{2} \right) \end{aligned} \quad (6)$$

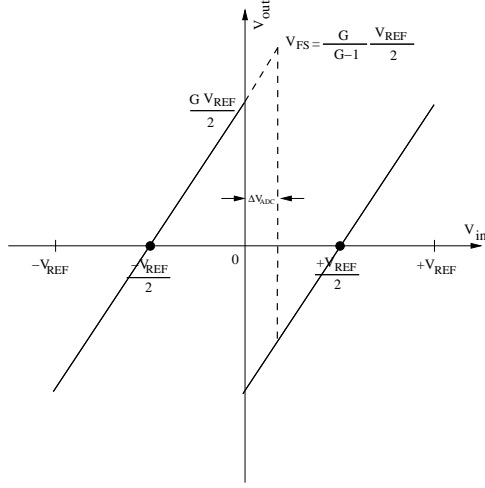


Figure 2: Residual error characteristics and allowed threshold voltage variations.

This corresponds to a quantization interval $Q = 2V_{FS}/2^n$, where n is the number of bits.

Reducing an interstage gain allows for variations in threshold voltages of the sub-ADC comparators. Figure 2 shows the residual error characteristics for the 1-bit per stage architecture and allowed threshold voltage change (ΔV_{ADC}) before the full scale range of the next stage is reached. For the 14-bit example introduced above, the gain of 1.81 is used and V_{REF} is set to 1V. The full scale range of the converter is $V_{FS} = 1.12$ V. This accommodates ± 0.12 V variations in the threshold voltage of the sub-ADC comparator.

2.2.2 Sub-DAC error

The role of the sub-DAC block is to provide an estimate of the input signal voltage to the next stage. For a 1-bit per stage architecture the desired sub-DAC output is $(q - \frac{1}{2})V_{REF}$, where q is the digital decision level obtained by sub-ADC and V_{REF} is the sub-DAC reference voltage. Unlike comparator offset errors, errors in the sub-DAC output change the voltage passed to subsequent stages, and ultimately distort the ADC output. If Δ_{DAC1} , Δ_{DAC2} and Δ_{DAC3} represent sub-DAC errors in the first three stages of the N -stage converter discussed in Section 2.1, then (4) can be re-written as

$$\begin{aligned}
 X &= \frac{e_3}{G_1 G_2} + \left(q_1 - \frac{1}{2}\right) V_{REF} + \left(q_2 - \frac{1}{2}\right) \frac{V_{REF}}{G_1} \\
 &+ \left(q_3 - \frac{1}{2}\right) \frac{V_{REF}}{G_1 G_2} + \Delta_{DAC1} + \frac{\Delta_{DAC2}}{G_1} \\
 &+ \frac{\Delta_{DAC3}}{G_1 G_2} \quad (7)
 \end{aligned}$$

From (7) it can be seen that the sub-DAC error associated with a stage scales down by the total gain factor of all previous stages.

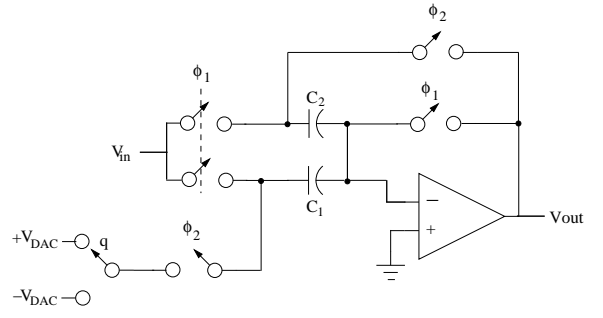


Figure 3: Switched capacitor implementation of the MDAC for 1-bit per stage architecture.

Stages near the pipeline front end are especially critical, and tend to dominate these error contributions.

2.2.3 Interstage Gain Error

The gain error changes the slope of the residual curve. Many modern pipeline converters are implemented using switched capacitor circuits [4]. This technology is suitable for high-speed, low power and monolithic CMOS implementations of pipeline ADCs. For CMOS implementations, the S/H block, sub-DAC and gain block are implemented together is what is known as a multiplying digital-to-analog converter (MDAC). Figure 3 shows switched capacitor implementation of the MDAC for 1-bit per stage architecture. Non-overlapping clocks, ϕ_1 and ϕ_2 , control the switches of the MDAC. During ϕ_1 , the input voltage is sampled onto two capacitors, C_1 and C_2 . During ϕ_2 , C_2 is connected to the amplifier through the feedback loop and C_1 is sampling one of the sub-DAC outputs, q or \bar{q} . The two capacitors in the MDAC block determine the value of gain. If there is a mismatch in one of the capacitor values, $C_1 + \Delta C_1$ instead of C_1 , the gain would be altered in the following manner,

$$V_{out} = \left(1 + \frac{C_1}{C_2} + \frac{\Delta C_1}{C_2}\right) V_{in} - \left(\frac{C_1}{C_2} + \frac{\Delta C_1}{C_2}\right) V_{DAC}. \quad (8)$$

Equation (5) shows dependency of the ADC output on gains. When designing the digital encoder block, gains are known in advance and their digital representations are implemented in hardware to be used during normal converter operation. When there is a gain error in a pipeline converter, the ADC output is greatly affected because the digital encoder assumes the nominal gain. For accurate representation of any gain value, excellent capacitor matching is required which is not achievable with current process technologies.

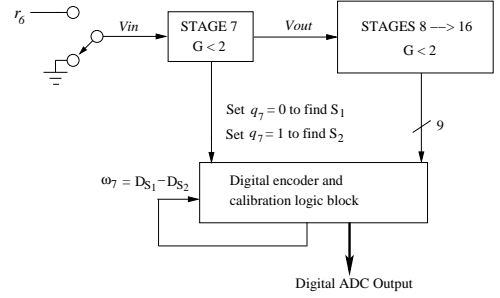
3 Proposed Digital Architecture for Background Calibration of Pipeline ADCs

Digital calibration schemes measure the error contributions of the stage in the digital domain. The measured gain and reference voltage variations are used to form the ADC output code [5–7]. The accuracy of the calibration depends on how well the errors are measured in the digital domain. To digitally correct the ADC output code, modifications need to be made to the digital encoder block. Section 3.1 describes an off-line digital calibration scheme developed in [5]. This technique forms the basis for the proposed continuous digital calibration scheme discussed in Section 3.2.

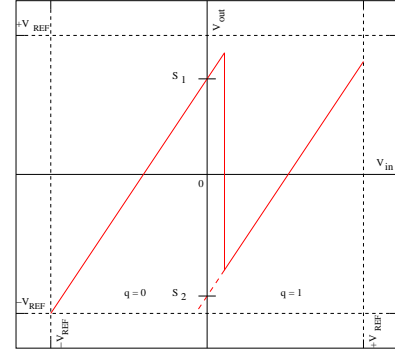
3.1 Off-line Calibration Algorithm

Figure 4 illustrates the off-line calibration process developed in [5] for a single stage of a pipeline ADC. The illustrated case is based on the implementation of a 14-bit ADC with 16 identical stages, interstage gains less than two, and 1-bit per stage topology. Gains less than two are chosen for all 16 stages so the output of each stage does not saturate the remaining stages. Calibration begins with the least significant stages (the end of the pipeline) and progresses toward the most significant stages. For example, to calibrate stage 7, we must assume that stages 8–16 have already been calibrated, or have been fabricated to sufficient accuracy that calibration is not needed. Figure 4(a) shows the off-line digital calibration applied to the seventh stage of a 16-stage architecture. Figure 4(b) shows residual characteristics for the stage being calibrated with the threshold offset (sub-ADC errors), interstage gain and DAC errors. Following calibration of the seventh stage, the process continues with the sixth stage, and so on until the first stage is reached and the calibration of the converter is complete.

Pipeline error characteristics often show discontinuities associated with the change in the output of the sub-ADC comparators. The residual error shown in Figure 4(b) consists of two segments (for $q=0$ and $q=1$) and the transition between the segments is determined by the comparator threshold. The goal of digital calibration is to make sure that for the same input voltage, the digital ADC output remains unchanged regardless of which segment is selected by the sub-ADC comparator of the stage. To assure this consistency, the converter output is examined with the stage input set to zero volts, where the stage is forced to operate on each of the segments. Setting $q_7=0$ with $V_{in}=0$, forces Stage 7 to operate on the left segment, producing output residual voltage S_1 . S_1 is quantized by the remaining pipeline stages (stages 8, 9, 10, ..., 16), producing digital output D_{S_1} . Setting $q_7=1$ ($V_{in}=0$) forces Stage 7 to operate on the right segment, producing residual voltage S_2 and in turn digital output D_{S_2} . The digital output of the N -stage converter is given by Equation (5). Each stage output bit is given a weight indicated by the gain products given in parenthesis. Most pipeline ADCs use ‘nominal’ design gains to construct the digital output. This



(a) Off-line digital calibration applied to the seventh stage.



(b) Residual error plot of 1-bit per stage architecture with errors.

Figure 4: Pipeline ADC with off-line digital calibration applied to the seventh stage.

approach is correct only if the converter is free of any gain or sub-DAC errors. If the implemented gain is different from the design value, or if sub-DAC errors exist, there will be error in the ADC output. Making these weights programmable is the idea behind the foreground digital calibration technique discussed in [5]. Equation (5) can be modified to include these programmable weights,

$$D = \sum_{i=1}^N q_i \omega_i, \quad (9)$$

where q_i is the output bit for stage i and N is the number of stages used and ω_i is the programmable term associated with the stage. Once found, the correction term ω_i is fed back to the digital encoder and calibration logic block. This value is a weight associated with the bit of the stage being calibrated and it carries the information about the interstage gain and sub-DAC errors.

3.2 Development of a Digital Architecture for Continuous Calibration

Pipeline architecture ADCs rely on a two-phase, non-overlapping clock signals with clock phases denoted ϕ_1 and ϕ_2 . All the odd stages in a pipeline sample during phase ϕ_1 and present the valid residue output to the next stage during ϕ_2 . All the even stages work on the opposite clock phase. This

Stage	Increasing time \longrightarrow																									
	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_2
1	1	D_1	2	D_2	T	D_T	4	D_4	5	D_5	...															
2	D_0	1	D_1	2	D_2	T	D_T	4	D_4	5	D_5	...														
3	0	D_0	1	D_1	3	D_3	T	D_T	4	D_4	5	D_5	...													
4	D_{-1}	0	D_0	1	D_1	3	D_3	T	D_T	4	D_4	5	D_5	...												
5	-1	D_{-1}	0	D_0	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...											
6		-1	D_{-1}	0	D_0	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...										
7			-1	D_{-1}	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...									
8				-1	D_{-1}	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...								
9					0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...							
10					0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...							
11					-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...					
12					-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...					
13						-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...				
14						-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...				
15							-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...			
16								-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...		
17									-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...	
18										-1	D_{-1}	0	D_0	1	D_1	2	D_2	3	D_3	C_5	D_{C5}	4	D_4	5	D_5	...

Table 1: Sample propagation through the pipeline for the proposed real-time digital calibration technique.

allows for all stages in the pipeline to operate concurrently. A proposed real-time digital calibration was realized using two extra stages located at the end of the pipeline. Two additional stages allow for a calibration sample to be introduced in the pipeline and still maintain the normal operation of the converter. Table 1 shows propagation of samples through the pipeline during the calibration process. Table 1 is based on a 14-bit ADC with 1-bit per stage topology, 16 identical stages plus two additional stages for calibration (total of 18 pipeline stages), and gains less than two. Numbers 1 through 18 indicate pipeline stages. Values -1, 0, 1, 2, ..., correspond to sample number being acquired by a given stage, and D_{-1} , D_0 , D_1 , D_2 , ..., correspond to digital representation of the sample produced at the output of a given stage. For example, sample number 4 is processed by Stage 1 on a phase ϕ_1 and its digital representation as well as a residual is available on ϕ_2 . At this time, Stage 2 is ready to acquire this residual voltage. Stage 2 produced its coarse digital representation on the following ϕ_1 . This goes on until all 16 stages in a pipeline have coarse digital representation of sample number 4 available for the digital encoder and calibration logic block where the corresponding digital value for the sample is obtained. After the inherent pipeline delay, digital outputs become available on every ϕ_1 . This is considered a normal converter operation and it must be preserved during the calibration process.

When calibrating a stage using the digital calibration algorithm derived in [5], the stage being calibrated needs to be taken off line which in turn will interrupt normal operation of the converter. To avoid this, two extra stages are added at the end of the pipeline. This allows a conversion cycle to be freed for calibration and still maintain the normal converter operation. During a calibration cycle, all samples at various stages of the pipeline are shifted by two stages down in the pipeline, making sure the converter maintains a full 14-bit output. Table 1 shows the calibration of Stage 5. An artificial sample is introduced at the beginning of the pipeline denoted "T". At the same moment, sample number 3 is shifted as an input into Stage 3.

This means that Stage 3 for this instant acts as a first stage of the pipeline and last stage for this sample will be Stage 18. Sample number 2, which should be at the calibration moment occupying Stage 3, is now shifted two stages down to the next free odd stage, Stage 5 and so on. The last sample that needs to be shifted at the calibration instant is located in Stage 14. Instead of going to Stage 15 on the next clock phase, it will be routed to Stage 17. It can be seen from Table 1 that all samples still propagate through 16 stages with no time delay introduced and no lost samples.

Due to the pipeline shift, formation of the digital output code during the calibration process needs additional consideration. In (5) it can be seen that each stage is given a weight indicated by the gain products given in parenthesis. When calibration occurs, Stage 3 becomes the first stage of the pipeline, and should be given weight $(G_1G_2G_3 \dots G_{N-1})$. Similarly the weights associated with the other stages need to shift to reflect the reorganization of the pipeline. The weights for Stages 1, 2, 3, ..., need to be available at location of Stages 3, 4, 5, ..., respectively for the correct formation of the final digital output during the calibration process.

4 Results and Complexity of the Developed Technique

The calibration scheme was implemented using VHDL and simulated using the Verilog-XL simulator. The real-time calibration technique was derived for a 14-bit ADC with 1-bit per stage architecture implemented using 18 identical stages (including two extra stages for calibration purposes). To model the accurate behavior of the pipeline ADC, fully digital odd and even stages were created using VHDL. Gain, threshold and sub-DAC reference voltages were made as controllable variables at the input of each simulated pipeline stage. Nominal gain for all 18 stages was set to 1.81. The input range (V_{FS}) for this converter was set to ± 1.12 V and the reference voltage for the converter was set to $V_{REF} = 1$ V. A sampling

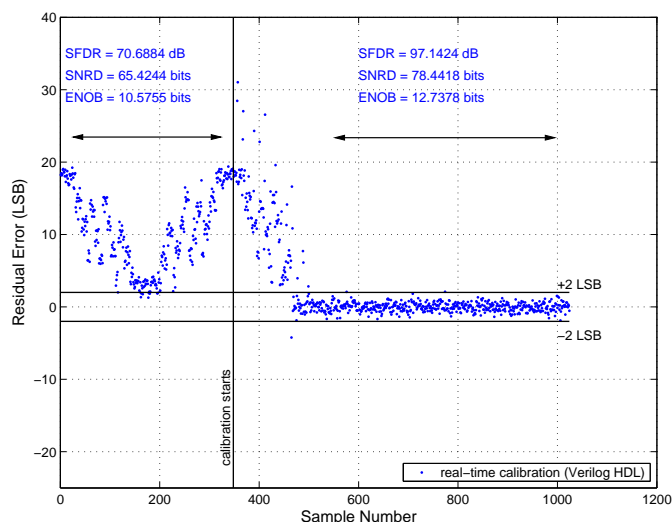


Figure 5: Residual error characteristics for a simulated ADC with applied real-time calibration and errors introduced in all 18 stages of the converter.

frequency of 51.2 MHz was used and the sinusoidal test signal was set to 150 KHz with the amplitude at -1 dBFS (994 mV). Errors were introduced in all 18 stages (including two extra stages used during calibration) of the converter and 1024 samples were used. Capacitor matching error between 0.1-0.5% was simulated. For threshold voltage variations, a maximum error of up to 10% of V_{FS} was simulated. Figure 5 shows the residual error characteristics for a simulated 14-bit ADC calibrated in a real-time. Before activating the calibration signal, the behavior of the ADC with the error contributions in all 16 stages is presented. The ADC behaves as a 10-bit converter before calibration and as 12.7 bit converter after calibration. Once the calibration signal is activated, 154 clock cycles are needed for completion of the calibration process. At the sampling rate of 51.2 MHz this corresponds to $3\mu\text{s}$ to complete a calibration of 7 stages. Based on the BuildGates Extreme synthesizer, approximately 100,000 logic gates are needed to implement the derived calibration. For a minimum feature size of 135 nanometers the required area to implement the derived calibration logic is approximately 0.26 mm^2 , based on the ITRS report from year 2003 [9]. This is a fully digital logic design and therefore, the required area scales down easily with new process technologies.

5 Conclusions

Different calibration techniques targeted to pipeline ADCs have been proposed in the literature and successfully implemented. Most of the reported calibration schemes rely on the converter being off line while calibrated or are analog in nature. Here we proposed a continuous digital calibration scheme targeted for pipeline ADCs. The scheme expands on a digital calibration algorithm developed in [5]. The proposed

architecture is completely digital, transparent to the overall system and applicable to multiple bits per stage pipeline architectures. It is realized using two extra stages located at the end of the pipeline. These stages are used only during calibration process. A hardware model was designed using VHDL and it was effective in showing the success of the proposed technique. For a simulated ADC, the number of effective bits was improved by at least 2-bits and the dynamic range of the converter was improved by at least 20 dB. The required area to implement the necessary digital logic scales down easily with the new process technologies, making it an attractive solution for improving resolution of pipeline converters.

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