

Design and Layout of a Programmable
Bandpass IQ Delta-Sigma Modulator Analog
to Digital Converter.

S. Saucier R. Bryant

December 21, 2001 - Electrical and Computer Engineering
Department, University of Maine, Orono

Contents

1	Introduction	1
1.1	Project Overview	1
1.1.1	Sigma-Delta Basics	1
1.1.2	Multi-Stage Noise Shaping (MASH)	3
1.1.3	Frequency Selection	4
1.2	Objective Of The Project	5
1.3	Project Specifications	7
1.4	Inputs and Outputs	7
1.5	Known Limitations of Current Design	8
1.6	Organization of the remainder of the report	10
2	Circuit Design	11
2.1	Overall circuit design	11
2.2	Modulator	11
2.2.1	Component function	11
2.2.2	Counter	13
2.2.3	Combinational logic	14
2.2.4	Capacitor gate control logic	15
2.2.5	Modulator capacitors	16
2.3	MASH stage	19
2.3.1	Operational transconductance amplifier (OTA)	19
2.3.2	Common mode feedback (CMF)	22
2.3.3	Integrator capacitors	23
2.3.4	CMF capacitors	23
2.3.5	Comparator	24
2.3.6	DAC Switch	28
2.4	Digital Filter	30
2.4.1	Component function	30
2.4.2	Design rational and tradeoffs	30
2.4.3	Specifications and Simulations Results	32
2.4.4	Physical layout rational	32
2.5	Clock	32
2.5.1	Component function	32
2.5.2	Design rational and Simulations Results	33

2.5.3	Schematic and physical design	33
2.5.4	Clock buffers	34
2.6	Miscellaneous components	34
2.6.1	Basic Inverter	34
2.6.2	Logic Gates	36
2.6.3	Transmission Gates	36
2.7	Input output pads	37
2.7.1	Analog buffer	37
2.7.2	Digital buffer	41
2.8	Bypass capacitors	41
2.8.1	Component function	41
2.8.2	Design and physical layout rational	41
3	Circuit Verification	43
3.1	Design Check	43
3.2	Top Level Simulation Results	47
3.3	On-chip voltage and current demand	55
3.4	Performance with temperature variations.	55
4	Circuit Testing	58
4.1	Testing circuits	58
4.1.1	Probe calibration	58
4.1.2	On chip voltage verification	58
4.1.3	Capacitor linearity	58
4.1.4	Transistor Tests	60
4.1.5	Clock signals	60
4.1.6	Quadrature SDM	60
4.1.7	Digital stage outputs	60
4.2	Tests of Device	60
4.2.1	Static Power Test	61
4.2.2	Capacitor Bank Modulator Test	62
4.2.3	Baseband Signal A/D Conversion Test	63
4.2.4	Modulated Signal A/D Conversion Test	64
4.2.5	Evaluation of Nmos transistors	71
4.3	Additional Test Proposals	76

5	Summary	80
5.1	Comparison of simulation and experimental results	80
5.2	Potential improvements	80
5.2.1	Design methodology	80
5.3	Suggestions for improvements	81
5.3.1	Operating frequency	81
5.3.2	Overall physical layout	81
5.3.3	Transmission gates	82
5.3.4	Modulator capacitors	82
5.3.5	Coping with parasitics	83
5.4	Project time commitment	84
A	Circuit Schematics	86
B	Circuit Physical Designs	95
C	Selected Process Parameters	105
	Biography of the Author	107

List of Tables

1.1	Table of Specifications	8
1.2	Table of Pinouts	9
2.1	Table of major components of the project.	12
2.2	Table of combinational logic outputs.	14
2.3	Table of combinational logic outputs. Letters refer to Figure 2.1. G_{in} refers to a gate control signal generated by the capacitor gate control logic.	16
2.4	Modulator capacitor values and subunit values.	18
2.5	Simulation of the OTA.	22
2.6	Table of output coding logic.	31
2.7	Total Gate Capacitance Attached to Each Clock Phase.	33
2.8	Dimensions of inverters responsible for non-overlap adjustments in the clock.	34
2.9	Specifications of Basic CMOS Inverter	36

4.1	Table of Probe Pads	59
4.2	Signal at first integrator input stage given the frequency select settings.	63
C.1	Selected Process Parameters Considered in Design (Source – MOSIS).	106

List of Figures

1.1	Second order sigma-delta block diagram.	2
1.2	Block diagram of proposed device.	6
1.3	Switched capacitor second order sigma-delta implementation.	7
2.1	Timing diagram of modulator. The overlap periods are exaggerated for clarity. A is latching of counter output. B is latching of the modulator logic output. C to D is the capacitor sampling interval. During the interval E to F the charge is integrated off the capacitors. Subscripts 1 and 2 refer to two consecutive cycles.	17
2.2	DC current response of the OTA. One input swept from 1 to 4V while the other is fixed at V_{cm}	21
2.3	Transient response of comparator.	26
2.4	DC response of comparator.	27
2.5	The four phases of the clock (ϕ_1 , ϕ_2 , ϕ'_1 , and ϕ'_2) each driving a $2pF$ load). The clock rate above is $4MHz$ and demonstrates the non-overlap intervals.	35
2.6	Transmission gate testing circuit.	38
2.7	Three transmission gates tested.	39
2.8	Results of transmission gate testing.	40
2.9	Comparison of one OTA voltage output and the voltage at the corresponding output pad for a $5\mu s$ simulation (no load).	42
3.1	Simulated results from MATLAB w/ 32k samples.	48
3.2	Simulated results from MATLAB w/ 1k samples.	49
3.3	Simulated results from schematic w/ 1k samples.	50
3.4	Simulated results (full range and a closer look, with average value curve) from schematic w/ 1k samples.	52

3.5	Simulated results (full range and a closer look, with average value curves from both stages) from schematic w/ 1k samples.	53
3.6	Simulated results (full spectrum and a closer look) from top level schematic w/ 500 samples, modulated by $\frac{f_s}{32}$.	54
3.7	On chip V_{dd} and supply current. Simulated with a total lead inductance of $4nH$ on the power pins and eight output bits loaded with $20pF$ each.	56
3.8	On chip V_{dd} and supply current. Same conditions as Figure 3.7 except without the on chip by-pass capacitance.	57
4.1	Baseband Test Data	65
4.2	Digital Filter errors in baseband test	66
4.3	Modulated Signal Test Data	68
4.4	Digital Filter errors in modulated test (In-Phase)	69
4.5	Digital Filter errors in modulated test (Quadrature)	70
4.6	NMOS $W/L = 3/0.6$.	73
4.7	NMOS $W/L = 3/1.8$.	74
4.8	NMOS $W/L = 3/3$.	75
4.9	NMOS $W/L = 3/0.6$.	77
4.10	NMOS $W/L = 3/1.8$.	78
4.11	NMOS $W/L = 3/3$.	79
A.1	Modulator capacitor gate control logic.	87
A.2	Comparator and buffer schematic.	88
A.3	OTA	88
A.4	Schematic of a NMOS/PMOS transmission gate. The other type of transmission gate used consisted of an NMOS transistor alone, of the same size as the NMOS above.	89
A.5	The clock	89
A.6	CMF circuit.	90
A.7	Edge triggered flip-flop with clear and set.	91
A.8	Full adder with carry	92
A.9	Coding logic for output bits	93
A.10	Shift register.	94
B.1	OTA	96
B.2	Comparator	97
B.3	Modulator capacitor gate control logic.	98
B.4	Five bit modulo-32 counter	99
B.5	NMOS/PMOS transmission Gate	100
B.6	The clock.	101

B.7	CMF circuit	102
B.8	Edge triggered flip-flop with clear and set.	103
B.9	Full adder with carry.	104
B.10	Shift register.	104

1 Introduction

1.1 Project Overview

Sigma-delta converters obtain high resolution through oversampling and noise shaping. However, due to oversampling the bandwidth is typically limited and sigma-delta converters are most often used in narrow bandwidth applications, such as radio, telephone, and other audio applications. The oversampling allows for much simpler components than some other types of Analog-to-Digital converters (ADCs). This makes them well-suited for VLSI technologies. The precision of the components can be less than the resolution of the overall converter. Inside the converter, integration and feedback are employed to shape quantization noise away from baseband. By oversampling and noise shaping, sigma-delta converters are able to obtain many bits of resolution using only a one-bit ADC (also called a quantizer).

The sigma-delta converter described in this paper has been constructed as part of thesis work that will investigate using multiple sigma-delta converters run in parallel to encompass a wider signal band while maintaining high resolution.

1.1.1 Sigma-Delta Basics

The sigma-delta ADC (Analog-to-Digital Converter) is an oversampled data converter, which means that it takes many more samples than are needed to reproduce the signal from the converter output. Critically sampled ADCs sample the input signal at the Nyquist rate, given as

$$f_{nyq} = 2f_b \tag{1.1}$$

where f_b is the maximum frequency of interest in the signal (sampling any slower than f_{nyq} leads to the aliasing of the input spectrum). The “error” of a quantizer, defined as the difference between the output and the input, has been shown to have a finite noise power based on the quantization interval that is spread throughout the band of frequencies ranging from DC to f_s , where f_s is the sampling rate of the converter. In an oversampled converter, where f_s is increased, the same amount of noise power is spread out over a

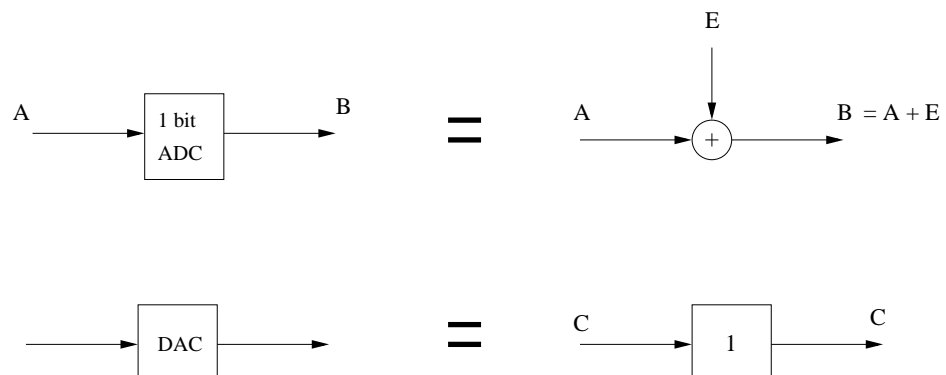
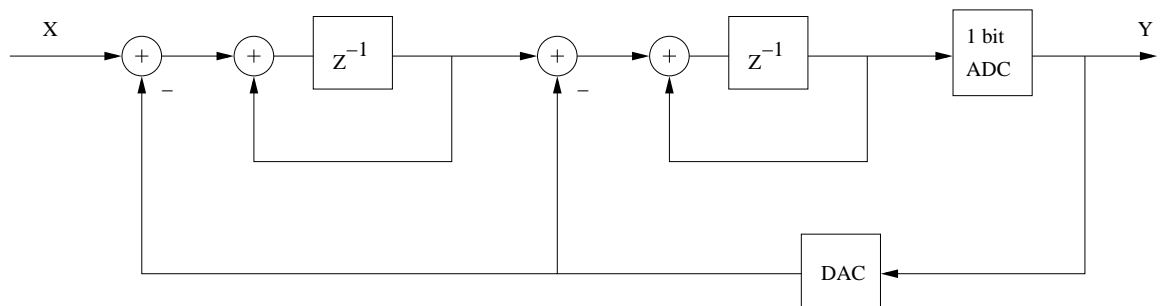


Figure 1.1: Second order sigma-delta block diagram.

larger range of frequencies, and thus diminished within the band of interest. The oversampling ratio (OSR) is given by

$$OSR = \frac{f_s}{2f_b} \quad (1.2)$$

The sigma-delta architecture takes advantage of the wide output spectrum by using integration and feedback to shape the quantization noise away from baseband. A basic block diagram of a second order sigma-delta converter appears in Figure 1.1. The one-bit quantizer, most often a comparator, drives a Digital-to-Analog Converter (DAC) that feeds the input back to the beginning of the loop, where it is subtracted from the input. In analysis of the loop the DAC is modeled as a unity gain block and the ADC is modeled as the addition of an error term to the signal. This error is defined as the difference between the output and input of the quantizer, and the transfer functions associated with the input signal and error terms, H_s and H_e , are found to be

$$\begin{aligned} H_s(z) &= z^{-2} \\ H_e(z) &= (1 - z^{-1})^2 \end{aligned} \quad (1.3)$$

The error transfer function of the system effectively pushes the quantization error away from baseband, where the desired output lies, while there is no shaping involved with the signal transfer function. Increasing the order of the system by adding more integration loops further improves the resolution, although stability becomes an issue for systems above first order [1]. Sigma-delta converters can easily handle large out of band signals as a result of this shaping of the output spectrum. As the sampling rate is increased, the error is more easily differentiated from the signal, and resolution is increased. Once the output is obtained it will normally undergo lowpass filtering to remove the shaped error from the system, and downsampling to return the quantized signal to the original sample rate.

1.1.2 Multi-Stage Noise Shaping (MASH)

The device described in this paper uses two second order loops cascaded in a MASH (Multi-stAge noise SHaping) architecture in order to achieve improved resolution. This results in a fourth order system that shapes quantizer noise once in each converter, pushing the total error even further away from

baseband and the desired output. The MASH architecture takes the previously discussed error signal generated in the first sigma-delta stage (denoted E_1) and processes it through a second stage, obtaining an extra bit for the output code. The output bits for both stages can be expressed as

$$\begin{aligned} b_1 &= H_s(z)X + H_e(z)E_1 \\ &= Xz^{-2} + E_1(1 - z^{-1})^2 \\ b_2 &= H_s(z)E_1 + H_e(z)E_2 \\ &= E_1z^{-2} + E_2(1 - z^{-1})^2 \end{aligned} \quad (1.4)$$

where X is the input signal and E_2 is the quantizer error term generated in the second stage. The proper filtering is able to remove the first stage error term E_1 , which is highly dependent on the input signal:

$$\begin{aligned} b_{out} &= H_s(z)b_1 - H_e(z)b_2 \\ &= Xz^{-4} - E_2(1 - z^{-1})^4 \end{aligned} \quad (1.5)$$

The remaining error for the system is the second stage error term E_2 , that is less correlated with the input signal than E_1 . Overall resolution is improved over that of a single second order loop.

1.1.3 Frequency Selection

The most common configuration of the sigma-delta is a lowpass implementation, although bandpass converters can be constructed by using a bandpass loop transfer function. In this project the effect of bandpass conversion is achieved by mixing (frequency translating) different bands of the input signal down to baseband and using a lowpass sigma-delta to code the signal. Two separate channels are used to process the in-phase and quadrature parts of the signal alone. The outputs of the two channels will be added together 90 degrees out of phase from one another to achieve complex modulation of each selected frequency band.

Outputs from two such devices converting adjacent bands will be filtered, translated as needed, and added back together in order to obtain high resolution conversion across a wider bandwidth. Once this has been accomplished, outputs from many similar devices can be combined to use the high resolution conversion of the sigma-delta ADC across the useable frequency band of DC to $\frac{f_s}{2}$.

1.2 Objective Of The Project

The objective of this project is to design and construct (through layout) a sigma-delta converter with an OSR of 32 that can achieve 14 bits of resolution operating at a sampling rate of 5MHz.

A block diagram of the proposed device appears in Figure 1.2. The device contains two channels of fourth order MASH architecture sigma-delta ADCs, one each for the in-phase (I) and quadrature (Q) parts of the signal. Each MASH section is composed of two cascaded second order sections, each yielding one bit of output. The resulting recombined output yields 4 functional bits of oversampled data per channel.

A MASH stage corresponds to the fully differential switched capacitor implementation of a second order sigma-delta modulator shown in Figure 1.3. A two-phase non-overlapping clock is required for operation in order to separate the sampling and integrating phases of circuit operation. Switches $S1$ and $S3$ close together on the sample phase (with switches $S2$ and $S4$ open) to sample the difference between the input and the feedback voltage from the DAC, and switches $S2$ and $S4$ close together in the integrate phase (with switches $S1$ and $S3$ open) to transfer the charge to the integrators. It should also be noted that switches $S3$ and $S4$ are clocked to open slightly before their counterparts at the end of their respective phases to reduce charge injection. The integrators are composed of operational amplifiers with capacitive feedback. A comparator is used for the one bit ADC and the DAC is a switch that sends back the reference voltages depending on the state of the comparator. The reference voltage V_{cm} is the midpoint of the supply rails for the circuit and V_{ref}^+ and V_{ref}^- are chosen based on the amplitude of the input signal in relation to the supply rails.

The mixing or modulation is achieved by sampling the input signal onto different valued capacitors before the first integrator. The charge that is sent to the integrator is effectively modulated with the frequency of the “waveform” that is made up of the sequence of different capacitance values. Factors of capacitance values are chosen from 32 evenly spaced values of a sine wave throughout one cycle. The first 8 different capacitance values from the beginning of the cycle are repeated with different polarity and in a different sequence in order to finish the cycle. Using the entire cycle of sine wave values takes 32 clock cycles, and effectively modulates the input signal with a frequency of $\frac{f_s}{32}$. Using every n th capacitor value of the waveform takes $\frac{32}{n}$ clock cycles, and effectively modulates the signal with a frequency

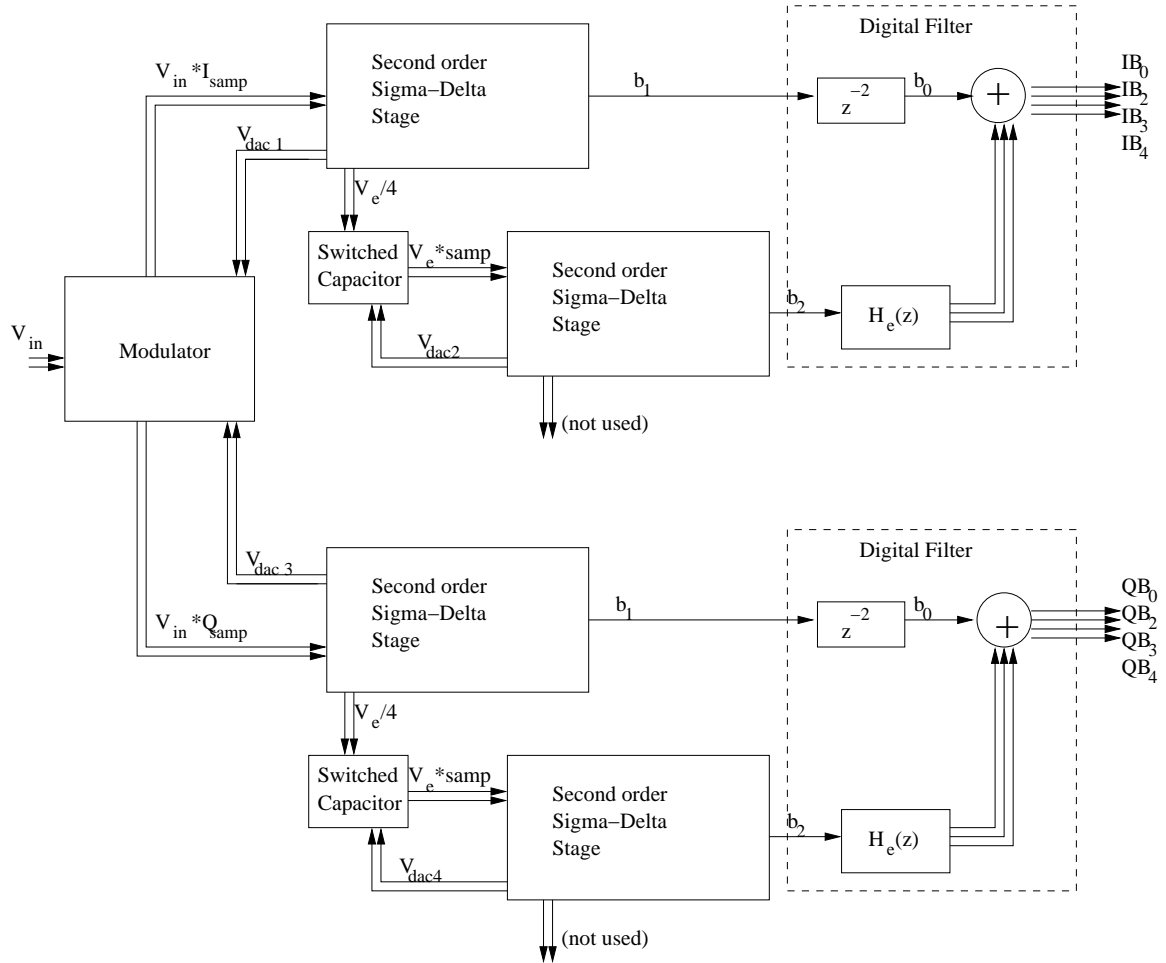


Figure 1.2: Block diagram of proposed device.

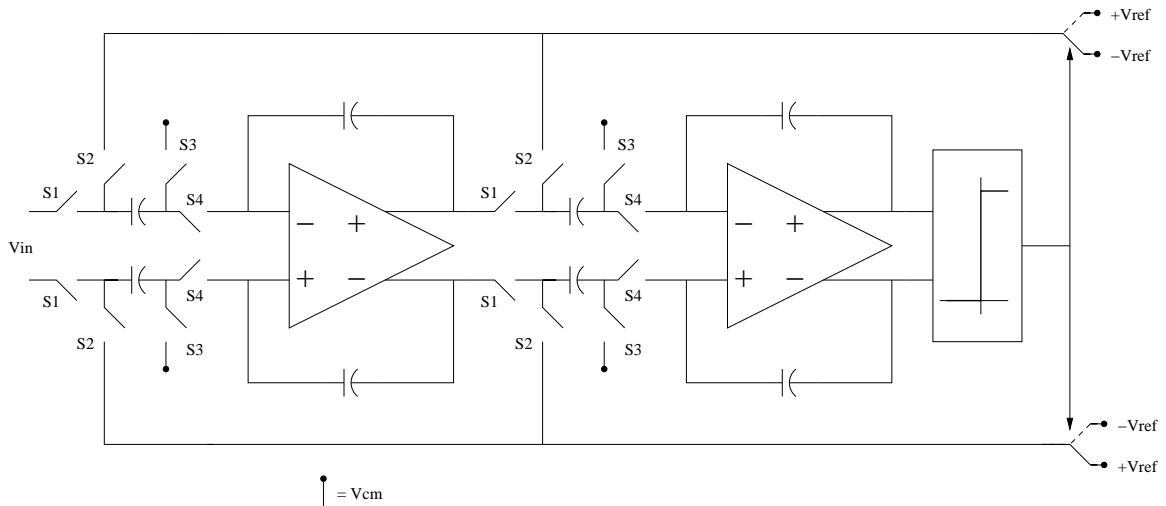


Figure 1.3: Switched capacitor second order sigma-delta implementation.

of $\frac{nf_s}{32}$. A logic network coordinates the sequence of capacitors selected from the bank of capacitors. The polarity of the capacitor can be changed by switching which side is connected to the integrator once the input signal has been sampled. The frequency of modulation is selected by the user through a 4 bit input word.

1.3 Project Specifications

Table 1.1 gives the specifications of the project. Power consumption is based on loading just the outputs required to record the digital filter output. That is, none of the testing outputs are loaded.

1.4 Inputs and Outputs

Table 1.2 gives the assignment of all pins on the package. Approximately half of the pins are present for testing purposes only. The function of these testing pins is discussed in Chapter 4.

Normal operation requires inputs of the power pins, reference voltage pins, signal input pins, frequency select pins, a reference clock, and a high

Specification	Value	Units
Maximum sample rate	5	MHz
Precision	14	bits
Supply	0 and 5	V
V_{cm}	2.5	V
V_{ref}^+	2.85	V
V_{ref}^-	2.15	V
Power consumption	70	<i>mW</i>
Signal		
DC	V_{cm}	
V_{pp}	$V_{ref}^- - V_{ref}^+$	
Digital Output	0 and 5	V
Oversample rate (OSR)	32	Filtered off chip.
Bandwidth	$\frac{f_s}{OSR}$	Hz
Center Frequency of Band	$\frac{nf_s}{OSR}$	$n = 0 : 15$

Table 1.1: Table of Specifications

signal on \overline{Q} and \overline{RST} . Outputs are taken from the eight filtered output pins.

1.5 Known Limitations of Current Design

The most significant known limitation of the design is the failure of the sampling capacitances to be of adequate precision. In order to obtain the 14 bit precision expected from the design the sampling capacitors are required to have an equal precision. Capacitor precision is low by a factor of 2 to 3 because of limitation of space on the die. The ramification of this is that harmonics of the sampling frequency will appear that are proportional to deviation of capacitor values from the designed values. This will be a predictable error and theoretically can be corrected with post-acquisition digital signal processing.

There is also an error that will occur from charge injection onto capacitors by transmission gates. Efforts were made to minimize this effect. To the first order, the differential configuration of this design eliminates charge injection. However, if the input signal modulates the charge injection at a transmission gate the differential design will be unable to compensate for this effect.

Pin	Name	Function
1	V_{dd}	Power
2	f_2	Frequency select
3	OTA^+	OTA test
4	OTA^-	OTA test
5	I_{12}^+	OTA test
6	I_{12}^-	OTA test
7	D_2	OTA test
8	V_{cm}	Reference common mode voltage
9	V_{ref}^+	Reference voltage above V_{cm}
10	V_{in}^+	Signal input
11	V_{in}^-	Signal input
12	V_{ref}^-	Reference voltage below V_{cm}
13	I_{22}^-	OTA test
14	I_{22}^+	OTA test
15	I_{21}^+	OTA test
16	I_{21}^-	OTA test
17	D_1	OTA test
18	I_{11}^-	OTA test
19	I_{11}^+	OTA test
20	Gnd	Power
21	V_{dd}	Power
22	f_1	Frequency select
23	f_0	Frequency select
24	BQ_1	Quadrature output bit, Stage 1
25	BQ_2	Quadrature output bit, Stage 2
26	q_0	Quadrature output bit, filtered
27	q_2	Quadrature output bit, filtered
28	q_3	Quadrature output bit, filtered
29	CLK	Input reference clock
30	q_4	Quadrature output bit, filtered
31	RST	Reset counter
32	BI_1	Inphase output bit, Stage 1
33	BI_2	Inphase output bit, Stage 2
34	i_0	Inphase output bit, filtered
35	i_2	Inphase output bit, filtered
36	i_3	Inphase output bit, filtered
37	i_4	Inphase output bit, filtered
38	f_3	Frequency select
39	Q	Quadrature test
40	Gnd	Power

Table 1.2: Table of Pinouts

The input signal is limited to the range of $V_{ref}^- - V_{ref}^+$ or $V_{cm} \pm 0.35V$. This limitation stems from the dynamic output range of the integrating amplifiers used. Signal amplitudes within the circuit reach as high as four times the amplitude of the input, so the input signal must be limited to avoid saturation of the amplifiers. Additional modifications to the integrating amplifiers could extend their range approximately $200mV$ giving a slightly wider input range.

Sampling frequency is specified as $5MHz$. This is conservative. Integrations within the ADC must be completed within slightly less than half a cycle. Typically this is accomplished in about $50ns$, so sampling rates approaching 8 to $10MHz$ may be possible. However other limitations such as stability of the on-chip supply voltage restrict the maximum frequency.

1.6 Organization of the remainder of the report

Chapter 2 contains a description of the schematics and layouts of the various components of the circuit. There is a discussion of the rational and tradeoffs associated with each component, circuit design, and layout. The required specifications for each component are given along with the performance of the simulated circuits.

Chapter 3 reports the verification results of the overall design. The effects of parasitics and temperature are also included.

Chapter 4 gives the circuit testing capabilities designed into the chip. The results of the measurements will be reported and the results compared to the simulated data following testing in early 2002.

Chapter 5 summarizes the project and draws conclusions.

Circuit schematics are given in Appendix A and physical layouts in B. Several fundamental process parameters were important in the design of this circuit. These selected parameters are given in a table in C.

2 Circuit Design

This chapter is organized in a hierarchical fashion. The first section discusses the highest level of the circuit design. The second section of this chapter contains a description of the major components of the design. Subsequent sections describe the specifications, design, and performance of the components and subcomponents. Design features that facilitate testing are discussed in Chapter 4. Table 2.1 contains the major components and subcomponents in the Sigma-Delta Modulator (referred to as SDM).

2.1 Overall circuit design

The overall architecture of the circuit includes two fourth-order SDMs with a single modulator. The block diagram of the circuit is illustrated in Figure 1.1 in Chapter 1. The modulator function is described extensively below.

The output of the first MASH stage is an error signal and a bit stream. The bit stream b_1 is sent to the digital filter. The error signal V_e is attenuated by a factor of 4 (in order to reduce clipping in the integrators) and presented to the second MASH stage for quantization. The bit stream output of the second MASH stage, b_2 , is amplified by 4 (in order to preserve the original amplitude of the signal) and combined with b_1 in the digital filter to give the final 4 bit result.

The layout is largely dictated by the modulator capacitors. These capacitors serve to separate the layout in two parts, a digital portion at the bottom and the analog portion at the top. Only clock signals and the bit streams b_1 and b_2 pass between the top and the bottom of the layout.

2.2 Modulator

2.2.1 Component function

The modulator block enables selection of the frequency band to use for the analog to digital conversion. The bandwidth of the converted signal is $\frac{f_s}{2OSR}$, where f_s is the sampling rate and OSR is the over sampling rate. The selectable center frequencies are $\frac{nf_s}{OSR}$ where n is an integer from 0 to $\frac{OSR}{2} - 1$.

Component	Major subcomponents
Modulator	
	Counter
	Switching logic
	Modulator logic
	Input capacitor array
MASH stage	
	Operational transconductance amplifier (OTA)
	Common mode feed-back (CMF) circuit for OTA
	Integrator and CMF capacitors
	Comparator
	DAC with Latch
	Current references
Digital Filter	
Clock	
Miscellaneous components	
	Basic Inverter
	Logic gates
	Transmission gates
Input-output pads	
	Digital output current buffer
	Analog output current buffer
By-pass capacitor	
Test circuits	(See Chapter 4)

Table 2.1: Table of major components of the project.

The modulator consists of two matched sets or eight sinusoidally weighted capacitors and associated logic. The matched pairs are for the two differential signal paths. The input signal is sequentially sampled on to each of the pairs of capacitors to modulate the input and shift the desired frequencies to baseband. Modulation is done simultaneously by $\sin(\frac{nf_s}{OSR}t)$ and $\cos(\frac{nf_s}{OSR}t)$ so that the in-phase and quadrature component of the signal is obtained.

The modulator consists of four major components:

1. A 5 bit barrel counter that can be programmed to count by increments of 0 to 15. Its output bits are $b_4b_3b_2b_1b_0$.
2. A block of combinational logic which interprets $b_4b_3b_2b_1b_0$ and latches the capacitor selected for the next clock cycle.
3. A block of logic which controls the gates to the sampling capacitors by combining the clock edge with latched output from the combinational logic.
4. The 16 capacitors.

A timing diagram of the modulator is shown in Figure 2.1. The seven clock signals are shown relative to one another, but the non-overlap periods are expanded for clarity. The letters indicate critical timing points. The subscripts refer to two consecutive cycles. Latching of outputs and opening of gates occurs on the rising edges of clock pulses. The counter output latches at A_1 and has until A_2 to increment and stabilize at its next value. The combinational logic section evaluates the counter output between A_1 and B_1 then remains latched until B_2 . The capacitor gate control logic must evaluate the combinational logic output before C_1 when the gate control signal is generated. Capacitors sample the input between C_1 and D_1 . It is essential that the input gates are completely closed before the integrate gates open at E_1 . The integration is terminated with gate closure at F_1 .

2.2.2 Counter

Counter function

The counter consists of five full adders with carries. The four bit input word $f_3f_2f_1f_0$ allows counting by $f_3f_2f_1f_0$ bits at a time. Counting is modulo 32. An additional input to the counter, \overline{CLR} , resets the counter to 00000 thus

Bit	Subscripts	Function
CSEL	07, 16, 25, 34	Selects the active set of capacitors.
POS	0 ... 7	Indicates polarity for sampling.
INP	0 ... 7	Indicates whether capacitor is in-phase or quadrature.

Table 2.2: Table of combinational logic outputs.

allowing the synchronization of two of these circuits. The output of each of the five counter bits, $b_4b_3b_2b_1b_0$, is latched on $\overline{\phi_1}$ and the output is fed-back to the input at that time. Thus the counter has a full clock cycle to increment and stabilize.

Counter Testing

The counter was tested by driving it with a $33MHz$ clock. With inputs $f_3f_2f_1f_0 = 0000, 0001, 0011, 1000,$ or 1111 to the counter the output bits $b_4b_3b_2b_1b_0$ were observed for 34 clock cycles. In all cases the expected sequences resulted from counting by 0, 1, 3, 8, or 15 was obtained. When \overline{CLR} is tied high counting proceeds normally. If \overline{CLR} is low, the output of the counter is fixed at $b_4b_3b_2b_1b_0 = 00000$.

Counter physical design

The layout of the counter offered no particular challenge, consisting of five full-adder components with latches on the output bits. The layout is shown in Figure B.4 in Appendix B.

2.2.3 Combinational logic

Combinational logic function

Five latched bits from the counter, $b_4b_3b_2b_1b_0$, are translated to 20 bits that are latched on $\overline{\phi_2'}$. Table 2.2 summarizes the interpretation of the bits. The bits CSEL designate two sets of capacitors for sampling. Because modulation is both in-phase and quadrature, the selected capacitors are always in pairs that are ninety degrees out of phase with respect to their relative sizes. POS indicates whether the input is connected to the top or bottom plate of the capacitor. INP indicates whether the output will be routed to the in-phase

or quadrature SDM. These twenty bits and their complements are latched on $\overline{\phi_2}$.

Combinational logic testing

The combinational logic was tested by driving it with the counter running at $33MHz$ clock. With inputs $f_3f_2f_1f_0 = 0000, 0001, 1000, 1001, 1011,$ or 1111 to the counter the 20 output lines were observed for 9 to 35 cycles and sequencing was correct.

Combinational logic schematic and physical design

The combinational logic is generated relatively simply given the counter output. These 20 boolean expressions are not given in this report. The expressions could be simplified, but the expressions are implemented in the unsimplified form, often causing the signal to propagate through four gates prior to the latch. Although there is adequate time for the signal to settle before the output is latched, in retrospect it would have been beneficial to simplify the boolean expression. This would have the obvious benefits of saving space and power, but the simplification would have reduced the wiring complexity of this circuit saved significant time. Time, it turns out, was the most valuable commodity in this project.

The outputs of this component are formed by two or three subcomponents for each pair of capacitors. The components are in close proximity to the capacitor gate control logic to assure that the signal has settled in the next stage in anticipation of the clock signal that triggers gate opening and closing.

2.2.4 Capacitor gate control logic

Capacitor gate control logic function

During each cycle of the clock, this section of the modulator is required to synchronize the sampling of the signal by four capacitors and open the appropriate capacitor gates to ensure proper routing, polarity, and modulation. A total of eight gates are connected to each capacitors. The control lines to each differential pair are the same. Two of the gates open for sampling during ϕ_1 and two others are open for integration at ϕ_2 .

Interval	Specified	Simulated
CSEL rise time	$< 1.5nsec$	$1.1nsec$
CSEL - ϕ_1 ($C_1 - B_1$) interval	$> 1.5nsec$	$5.3nsec$
G_{in} - ϕ_2 ($E_1 - D_1$) interval	$> 1nsec$	$1.2nsec$

Table 2.3: Table of combinational logic outputs. Letters refer to Figure 2.1. G_{in} refers to a gate control signal generated by the capacitor gate control logic.

Capacitor gate control logic schematic and physical design

The schematic and physical design are in Figures A.1 and B.3 respectively.

Capacitor gate control logic specification and simulation

This part of the modulator has the most critical timing requirement. The clock signal which triggers gate opening occurs about $6ns$ following latching of the combinational logic block output. Table 2.3 gives critical timing at the capacitor gates. These were measured with parasitic capacitances included. The total clock line load was 2pF, and the load on the inverters driving the capacitor gates is 150fF, which is the load on the longest gate line.

2.2.5 Modulator capacitors

Component function and specification

The modulator capacitors are required have values spread over approximately a ten-fold range and to have high precision. The relative value of the eight capacitors need to be sinusoidally related, taking on values proportional to $\sin(\frac{n\pi}{8} + \frac{\pi}{16})$ where n is an integer ranging from 0 to 7. To obtain 14 bit precision at the output of the SDM these capacitors must have a similar precision. A relative mismatch of these capacitors should result in energy in multiples of the modulator frequency and could be compensated for off chip, but regardless this should be kept at a minimum. The required capacitor values are given in Table 2.4

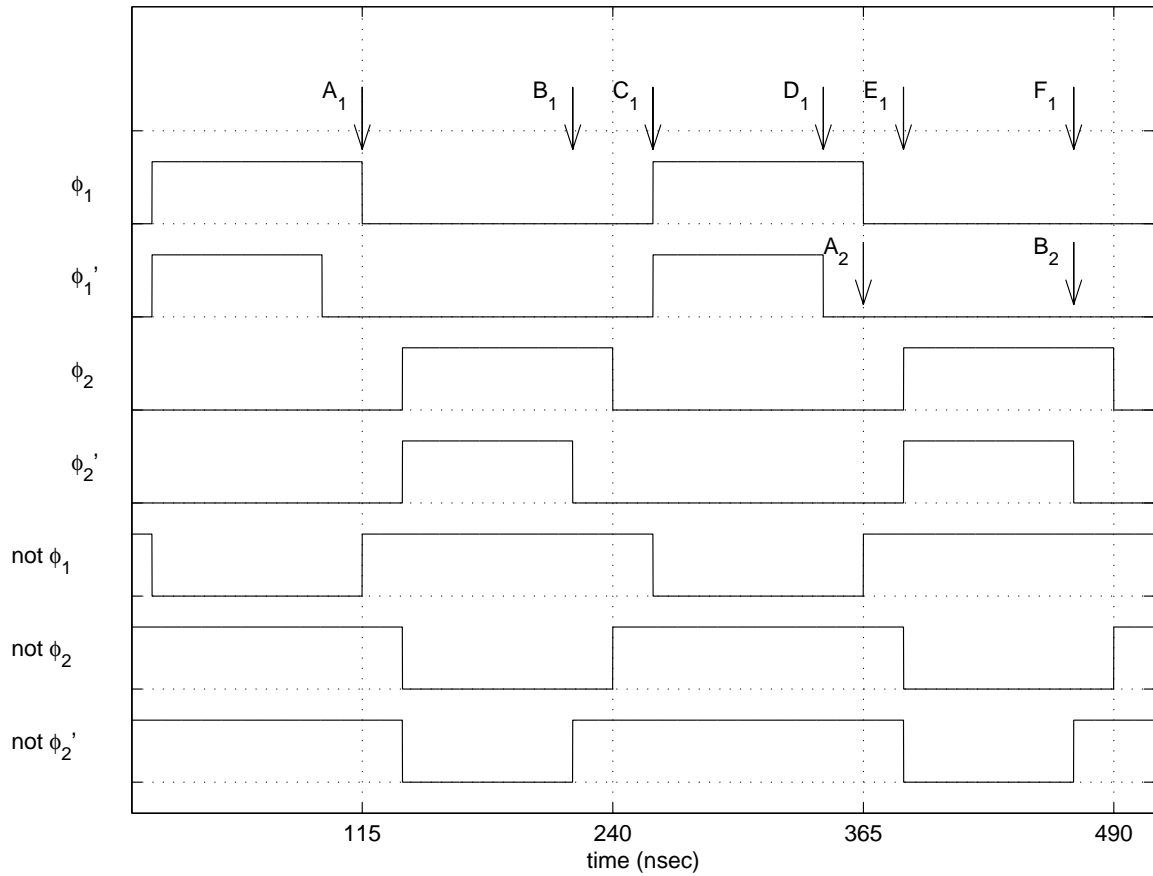


Figure 2.1: Timing diagram of modulator. The overlap periods are exaggerated for clarity. A is latching of counter output. B is latching of the modulator logic output. C to D is the capacitor sampling interval. During the interval E to F the charge is integrated off the capacitors. Subscripts 1 and 2 refer to two consecutive cycles.

Capacitor Number	Value (fF)	Subunit Size (fF)	Number of Subunits
0	19.60	19.55	1
1	58.06	19.36	3
2	94.28	18.85	5
3	126.88	21.14	6
4	154.60	19.32	8
5	176.38	19.59	9
6	191.39	19.13	10
7	199.04	19.90	10

Table 2.4: Modulator capacitor values and subunit values.

Design rational and tradeoffs

Three competing factors were considered in design of the capacitors; physical size, precision, and the demand placed on the OTA. In order to minimize the demand on the OTA and maintain adequate precision the low capacitance between metal layers was used. Although Metal 1 / Metal 3 capacitors would meet the precision and OTA requirements, the required die area would be too large. Metal 2 / Metal 3 capacitors were designed, but estimated precision of the resulting capacitors will fall short by a factor of two to three.

The relative sizes of the capacitors prohibited the use of a "unit" capacitor. Each individual capacitor is constructed of identical subunits. The subunit used for each capacitor is approximately $20fF$ in size, and plates are as close to square as possible. The bottom plate overlaps the top plate by 35λ . Metal 3 leads leading to the top plate contributed a significant amount of the total capacitance due to area and fringe effect. Consideration of this capacitance caused significant deviations from the goal of a square layout, but with the use of small strips (width of $\lambda/2$) of Metal 3 added adjacent to the top plate, the calculated capacitance from simulations exceeded the required precision. The Matlab code (capbits.m) was used to calculate the required plate sizes and trim lengths. $50aF$ parasitic capacitance was estimated at the switch end of each capacitor. Table 2.4 above includes the size and number of unit capacitors comprising each modulator capacitor.

Physical layout rational

The capacitors dictated the overall layout of the design. They are central on the die and separate the analog from the digital circuitry. A large Metal 1 ground plane was placed under each of these capacitors.

2.3 MASH stage

A MASH stage consists of two integrators comprised of an OTA and associated sampling and integrator capacitors and transmission gates. Additionally there is a common-mode feedback (referred to as CMF) circuit that corrects V_{cm} at each integrator output. Finally a comparator and a DAC with a latch feed back the reference voltage to each of the integrators. A block diagram of a Mash stage is illustrated in Figure 1.3.

The first integrator in a stage has a gain of $1/2$ and the second integrator has a gain of 2 . At the sampling capacitor for the second integrator both the input signal and the fed-back DAC output are applied to opposite plates on the same capacitor. On the first integrator a separate capacitor must be used for each signal. The feed-back for the first stage needs its own capacitor to avoid modulation and the feed-back on the second stage needs its own capacitor to avoid the attenuation factor of 4 that the error signal from MASH 1 experiences.

2.3.1 Operational transconductance amplifier (OTA)

Component function

The OTA acts as an integrator. The basic function of the OTA is to transfer charge from the input sampling capacitor to the integrator capacitor during ϕ_2 and accurately replicate the OTA output voltage on the sampling capacitor of the following stage during ϕ_1 .

The OTA is fully differential, so precise matching between sides is essential, but matching of the OTAs between stages is not essential provided that each stage accomplishes the require transfer of charge in the allotted time. A schematic of the OTA is shown in Figure A.3 in Appendix A.

Design rational and tradeoffs

The OTA design was modified from Degrauwe *et. al.* [2]. The design incorporates a low quiescent bias current, but uses positive feedback to recruit more tail current for the differential input pair. A pair of cascode transistors at the outputs increases the output resistance. The stability of an operational transconductance amplifier is determined by the capacitive load. The load on the OTA is dominated by the large capacitor in the CMF circuit. For this reason the CMF capacitor was selected to be $1pF$. The phase margin of the OTA with a total load of $1pF$ is 95 deg. The quiescent current drawn by the OTA is $240\mu A$ and the maximum current is $700\mu A$ when providing the maximum current to the load.

Simulation of the OTA

The performance of the OTA is summarized given in Table 2.5.

The OTA is sufficient to meet the current demands required. The maximum load that will be present at the OTA output will be the sum of the $1pF$ capacitor of the CMF, an integrator and load capacitor each of up to $400fF$ resulting in a total of $< 2pF$. A maximum output swing on each side of the OTA of $V_{cm} \pm 1.3V$ means that a total $q = 2pF \cdot 1.3V = 2.6pC$ of charge must be transferred in one-half of a clock cycle. Given a $5MHz$ clock frequency this requires an average current of $I = q/100ns = 26\mu A$. Figure 2.2 shows that the maximum current from the OTA is $150\mu A$ and occurs with one input $1.2V$ below V_{cm} of $2.5V$. This figure was obtained with one input fixed at V_{cm} and the other swept from 1 to $4V$. This is adequate to meet the charge transfer requirement above. The transconductance when both inputs are close to V_{cm} is $155\mu mA/V$.

Physical layout rational

The layout of the OTA exploits the bilateral symmetry of the design to match the two differential paths. Like transistors on each path are placed adjacent to one another and the signal paths are of similar lengths.

The physical layout is shown in Figure B.1 in Appendix B.

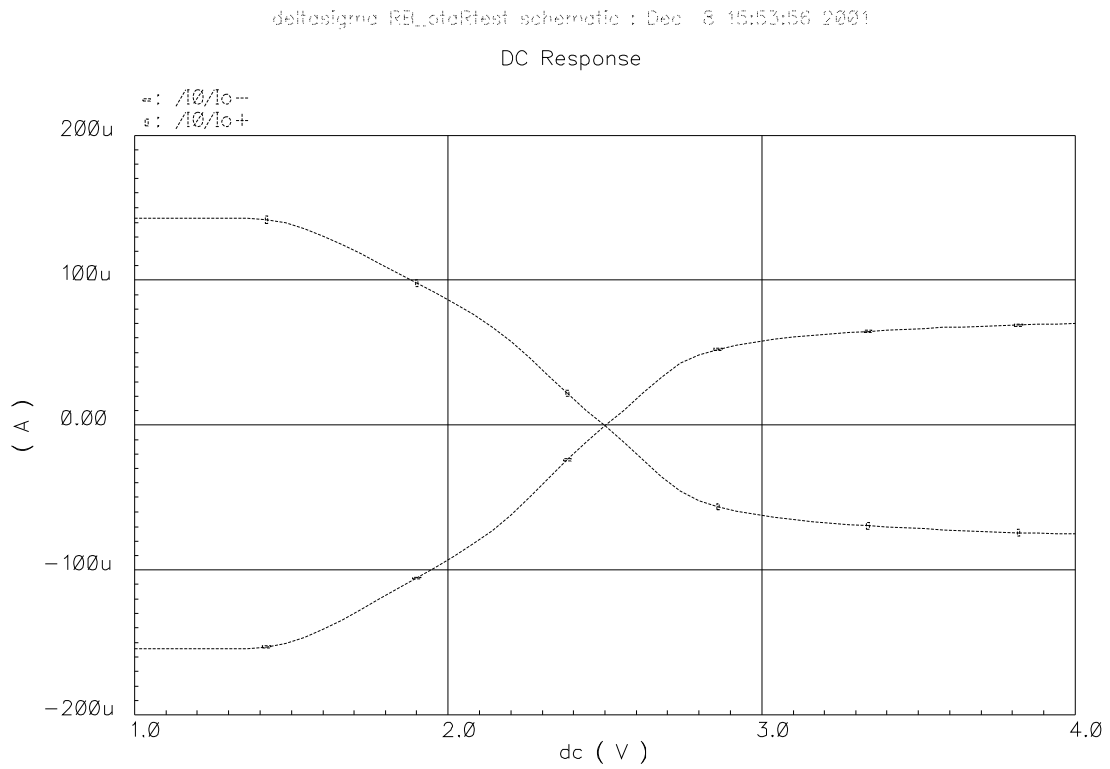


Figure 2.2: DC current response of the OTA. One input swept from 1 to 4V while the other is fixed at V_{cm} .

Parameter	Simulation Result
Quiescent OTA current	$240\mu A$
Quiescent output current	$2\mu A$
Maximum OTA current	$700\mu A$
Phase margin	95 deg
Transconductance at zero input	$155\mu A/V$
Maximum output current magnitude	$150\mu A$
Unity gain frequency	$28MHz$
Dynamic output range	???????

Table 2.5: Simulation of the OTA.

2.3.2 Common mode feedback (CMF)

Component function

The common mode feedback circuit maintains V_{cm} at the two differential outputs of the OTAs. One circuit is attached to each OTA.

Design rational and tradeoffs

The design is modified from Castello and Gray [3]. The capacitor sizes in the CMF circuit were selected to stabilize the OTA. The CMF circuit is not symmetrical with respect to positive and negative deviations from V_{cm} . The bias for the PMOS transistor is fixed, limiting the rate at which negative common mode variations can be corrected. For this reason a small positive quiescent output current was designed in the OTA. This quiescent current causes common mode variations to be positive. Since the voltage on the capacitor of the CMF circuit controls the gate voltage of the NMOS, positive drifts in V_{cm} produce larger corrective currents and are easily corrected.

A schematic of the CMF circuit is shown in Figure A.6 in Appendix A.

Simulations Results

The common mode voltage at the OTA inputs was observed during simulations of the entire circuit and did not differ from V_{cm} by more than $100mV$.

Physical layout rational

Matching of the two sides of the CMF is important to ensure the differential outputs were not adjusted unequally. Thus the CMF circuit component were fabricated close to one another. The physical layout is shown in Figure B.7 in Appendix B.

2.3.3 Integrator capacitors

Component function

The integrator capacitors are critical to the performance of the SDM stages. The key specifications are precise matching in conjunction with a size that allows the OTA to fully transfer any charge within half a clock cycle.

Design rational and specifications

The unit size of the Integrator capacitor is $200fF$. Multiples of this unit are combined in series and parallel to generate capacitors of $50fF$ and $400fF$ for the gain of the various OTA stages.

Physical layout rational

Capacitors from each of the differential signal paths were placed adjacent to one another to improve matching. All capacitors were placed in N-wells to isolate them from substrate noise.

2.3.4 CMF capacitors

Component function

Two capacitor sizes are needed for the CMF circuit. The smaller of the two samples V_{cm} and transfers the sample to the larger capacitor each clock cycle.

Design rational and tradeoffs

Precise matching from the small to the large capacitor is not critical, but matching with respect to the two differential signals is important. The large capacitor of $1pF$ contributes a majority of the load for the OTA. This value

stabilize the OTA as well as V_{cm} at the OTA output. The smaller capacitor is a 10^{th} the size of the the larger.

Physical layout rational

Capacitors from each of the differential signal paths were placed adjacent to one another to improve matching. All capacitors were place in N-wells to isolate them from substrate noise.

2.3.5 Comparator

Component function

The sigma-delta architecture only needs a one-bit ADC to quantize the signal, and thus a comparator is used to compare the loop output to a threshold level. The fully differential configuration of each MASH stage dictates that the two output voltages of the last integrator in the stage are instead compared to each other to see which is greater, rather than to ground (as in a single-sided configuration). A simple two-input comparator with a binary output (driving the output to the rails) gives the proper one-bit output for the converter, which then drives the DAC to generate the proper feedback voltages for the loop. For the comparator, the most important requirements are switching time and accuracy. The comparator needs to make an accurate decision based on the integrator output voltages before the integrate phase of the cycle is over, in order to allow the DAC enough time to switch in the proper feedback voltages to be used in the following sample phase.

Design rational and tradeoffs

The three major components of the comparator are a basic differential pair, a decision circuit, and an output buffer (the building blocks for the comparator follow those described in [4]). The comparator differential pair with decision circuit and comparator buffer schematic is shown in Figure A.2. The differential pair accounts for the voltage sensitivity of the circuit. The input voltages are translated into currents that are in turn evaluated by the decision circuit. The transconductance of the source-coupled pair sets the gain of the stage. By increasing the transconductance, the comparator output will switch for smaller voltages. The PMOS current mirror above the differential pair mirrors the two currents with some amplification to the decision circuit,

which generates the state for the comparator output. The decision circuit is composed of a cross-coupled NMOS pair which evaluates the currents and gives the comparator output. Higher current through one branch causes the gate voltage of the NMOS in that branch to rise while the gate voltage of the NMOS in the opposite branch falls. The gate-drain connected NMOS at the sources of the cross-coupled pair acts as a resistor as it shifts the lowest end of the output voltage swing up from ground. This allows the buffer to see an input voltage swing that varies around V_{cm} .

The largest output voltages generated by the decision circuit are only on the order of 2 or $3V_{TH}$, so the output buffer needs to translate those voltages to binary levels that can drive other inverters. The self biasing buffer [4] drives the output to both supply rails even when the input voltage range is small. This buffer has a differential input that is driven by the differential output of the decision circuit. The outputs of the decision circuit always oppose each other (one is high, the other is low, or vice versa) making it necessary to look at only one output of the decision circuit to determine the state of the comparator. One input is used to shift the bias levels for the buffer, and the other input drives the buffer to generate the single-ended output. In order to maintain proper phase of the signal through the comparator, the positive differential input drives the single-ended output while the negative differential input biases the circuit.

Specifications and Simulations Results

The two biggest areas of concern for the comparator are switching time and sensitivity. The comparator is designed without hysteresis to prevent quantization error. The integrate phase lasts for the second half of the clock period. This gives the comparator roughly $100ns$ to code the output when the system is clocked at its maximum sample rate of $5MHz$. This is the fastest the comparator needs to operate, regardless of the sample rate. The transient response of the comparator is shown in Figure 2.3. Here the propagation delay through the comparator is seen to be roughly $16ns$. By comparison, an op-amp used as a comparator will typically have a propagation delay on the order of hundreds of ns, much too large for this application. In the transient analysis the current used by the comparator is $20\mu A$ in the differential pair, $140\mu A$ in the decision circuit, and $110\mu A$ in the biasing of the output buffer. The large output inverter of the buffer draws currents on the order of $2mA$ when switching states and uses very little current otherwise.

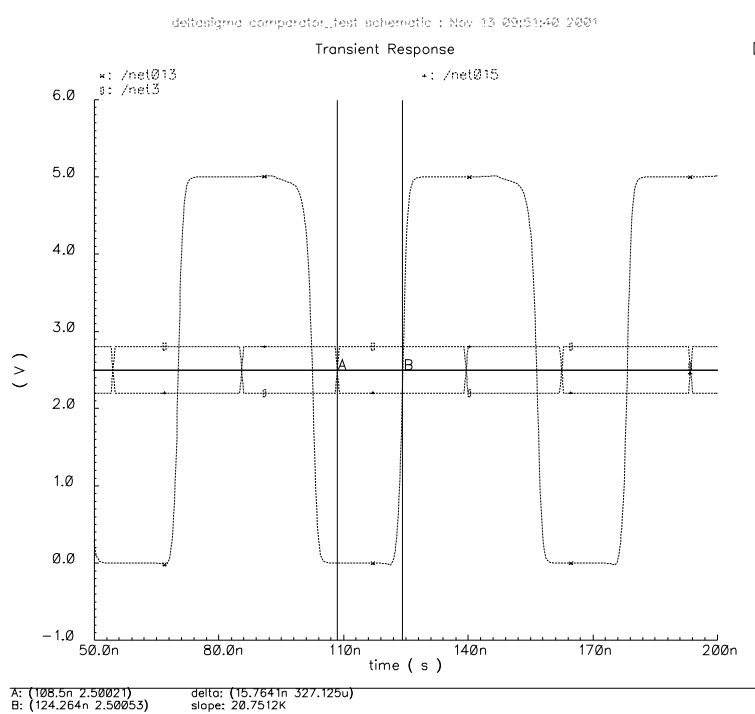


Figure 2.3: Transient response of comparator.

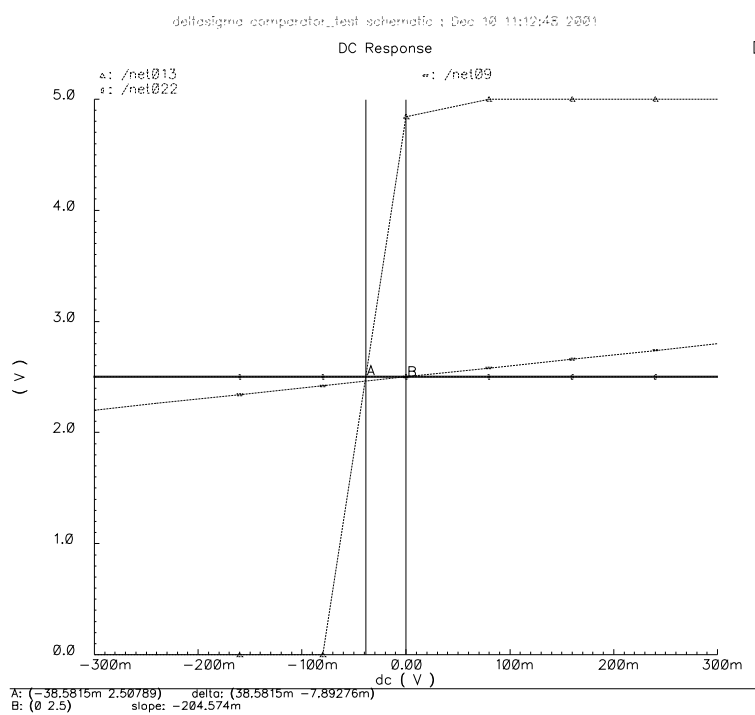


Figure 2.4: DC response of comparator.

The use of the negative feedback in the sigma-delta loop causes the integrator to constantly subtract charge, which forces the integrator outputs towards each other. It is important that the comparator can determine the polarity of the difference between these two outputs when that difference is very small, as is often the case. A DC voltage sweep of the comparator inputs, with one input fixed at V_{cm} and the other input swept from $(V_{cm} - 1V)$ to $(V_{cm} + 1V)$, is shown in Figure 2.4. The point at which the comparator output reaches 2.5V is considered to be the "decision" point for the comparator, and this point actually comes before the voltage across the inputs is zero. This offset voltage is useful in determining the sensitivity of the comparator, and from the figure this comparator has an offset voltage of just under 40mV. This means that the comparator will switch states when the inputs get within 40mV of each other.

Physical layout rational

In the layout of the comparator matching of components is a concern due to the symmetry of the design. Most pairs of transistors are laid out in the common-centroid manner as described in [4], while those that aren't appear in an interdigitated fashion in order to reduce the effects that any large scale wafer variations may have on matching. The large inverter in the output buffer is connected to both the substrate and the N-well with thick metal in compliance with the electro migration rules for the process. The physical layout of the capacitor is shown in Figure B.2

2.3.6 DAC Switch

Component function

After the signal has been quantized by the ADC, the output voltages are fed back to be summed with the input signal. The output bit for the stage is converted back into an analog voltage using a DAC (Digital to Analog Converter), and then fed back to the input. In this configuration the DAC needs to send back the proper reference voltages (either V_{ref}^+ or V_{ref}^-) to the positive input based on the state of the comparator, and the opposite reference back to the negative input. The reference voltages V_{ref}^+ and V_{ref}^- are supplied to chip externally, so the DAC needs only to close a switch in each feedback path.

Design rational and tradeoffs

Single transistors are used for opening feedback paths for the reference voltages. PMOS transistors are used to switch V_{ref}^+ (which is always higher than V_{cm}) and NMOS transistors are used to switch V_{ref}^- (which is always lower than V_{cm}). The transistors are sized the same as those used in transmission gates throughout the top level circuit.

Timing is an issue between the comparator and the DAC. The comparator values must be latched and sent to the DAC so that the feedback reference voltages don't change during the integrate phase of the clock. The comparator can only switch states during the integrate phase, and sending the comparator output to the switches immediately causes the output bits to oscillate until the integrate phase is over. This clocked latch does not need to have *SET* and *CLR* capabilities, since its operation is always the same. The design differs from the previously discussed latch in that only inverters and transmission gates are needed to construct it. For purposes of distinguishing this latch from that previously mentioned (which is called "latch"), it is referred to as "latch_nsc".

Specifications and Simulations Results

The DAC switch is tested along with the components that it will interact with in the sigma-delta loop. A comparator drives its input while the outputs are sent to clocked transmission gates. The DAC switch is clocked at 10MHz, and transfers the reference voltages as expected.

Physical layout rational

The layout for this circuit looks much like that of the latch with *SET* and *CLR* capabilities, although it the actual latch is only half the size. The only other components in the DAC are the 4 transistors, 2 NMOS and 2 PMOS apiece for each of the reference voltages V_{ref}^+ and V_{ref}^- .

2.4 Digital Filter

2.4.1 Component function

The bits that come out of the two stages of the MASH architecture, b_1 and b_2 are recombined through a digital filter in order to remove the error introduced by the quantizer in the first stage. Error from the second stage quantizer is still present, although it is more randomized with respect to the input signal than that of the first stage. The filtering applied to the output bits is effectively the same as that of the second order loop. Bit b_1 is delayed by 2 samples, while bit b_2 is filtered by the same transfer function that the quantizer error of each stage sees. The recombined output gives (from Equation 1.5)

$$\begin{aligned} b_{out} &= b_1 z^{-2} - 4b_2(1 - z^{-1})^2 \\ &= b_1 z^{-2} - b_2(4 - 8z^{-1} + 4z^{-2}) \end{aligned} \quad (2.1)$$

The factor of four in front of the filtered error bit comes from scaling the signal through the system in order to avoid clipping (first stage error term E_1 is scaled by four going into the second stage, and must be scaled coming out).

2.4.2 Design rational and tradeoffs

Given the fact that designing the circuitry to carry out analog multiplication and addition proves difficult, it was decided that the digital filter would be done with combinational logic blocks. The only values that b_1 and b_2 assume are 1 and 0, and thus the proper recombined values for b_{out} can be mapped for every possible sequence of output bits by assigning the following variables:

$$\begin{aligned} A &= b_1 z^{-2} \\ B &= b_2 \\ C &= b_2 z^{-1} \\ D &= b_2 z^{-2} \\ b_{out} &= A - 4(B - 2C + D) \end{aligned} \quad (2.2)$$

The values of b_{out} are shifted so that the minimum value is zero, and it is represented in a five bit number $B_4 B_3 B_2 B_1 B_0$. The logic table for the correct

A	B	C	D	b_{out}	$b_{out}+8$	$B_4B_3B_2B_1B_0$
0	0	0	0	0	8	01000
0	0	0	1	4	12	01100
0	0	1	0	-8	0	00000
0	0	1	1	-4	4	00100
0	1	0	0	4	12	01100
0	1	0	1	8	16	10000
0	1	1	0	-4	4	00100
0	1	1	1	0	8	01000
1	0	0	0	1	9	01001
1	0	0	1	5	13	01101
1	0	1	0	-7	1	00001
1	0	1	1	-3	5	00101
1	1	0	0	5	13	01101
1	1	0	1	9	17	10001
1	1	1	0	-3	5	00101
1	1	1	1	1	9	01001

Table 2.6: Table of output coding logic.

conversion from b_1 and b_2 to $B_4B_3B_2B_1B_0$ can be found in Table 2.6.

The entire filter is constructed out of shift registers and multi-input NAND and NOR logic gates, all circuits of minimal complexity. The shift registers that delay the samples one and two places are constructed out of pass transistors that are closed on opposite clock phases. The delayed digital values are walked through the shift register, and inverters after every pass transistor hold and help restore the value. The required logic function appears through examining the inputs and their corresponding outputs, and is carried out by a network of NAND and NOR gates, all sized to give approximately the same delay as a minimum sized inverter.

2.4.3 Specifications and Simulations Results

The shift registers and logic produce the correct output values for all possible combinations of sequences of bits b_1 and b_2 . After the shift registers set the delayed values on the rising edge of the clock, the signals propagate through at most 3 inverters before reaching the output buffers that drive off-chip loads. This accounts for a minimal delay through the filter that is much shorter than the clock phase.

2.4.4 Physical layout rational

While designed in separately, the logic for all coded bits is laid out in one cell. This allows for easy wiring of inputs where some signals are sent to many gates. In looking at table 2.6 it can be seen that output bit B_0 is always equal to A , or b_1z^{-2} , which simplifies the logic. Output bit B_1 is always low, and thus no consideration was given to the logic or pin out of B_1 .

2.5 Clock

2.5.1 Component function

The clock is required to provide two (ϕ_1 and ϕ_2) non-overlapping phases each of equal length. The non-overlap interval of $3ns$ assures that gates switching on opposite clock phases are never simultaneously open. Each phase also contains a separate signal (ϕ'_1 and ϕ'_2) that turns on at the same time as the unprimed phases, but turns off $3ns$ before the unprimed clock phase. This

Clock signal	ϕ_1	ϕ_2	ϕ'_1	ϕ'_2	$\overline{\phi_1}$	$\overline{\phi_2}$	$\overline{\phi'_2}$
Capacitance (fF)	780	590	396	396	346	346	864

Table 2.7: Total Gate Capacitance Attached to Each Clock Phase.

allows control of the order of switching of the top and bottom plates of the switched capacitors. The complement of three of the four phases (except $\overline{\phi'_1}$) is also supplied by the clock. The four non-complemented phases are shown in Figure 2.5 when driving a $2pF$ load.

2.5.2 Design rational and Simulations Results

A central clock was designed without peripheral buffering. This early decision, in conjunction with the choice of the basic inverter size and large number of gate loads, placed a high current demand on the centrally located clock. Table 2.7 gives the total gate capacitance attached to each clock phase. This resulted in the need for a large buffer attached to each clock phase (see Section clock buffers below.) $\overline{\phi'_2}$ has the largest load of $864fF$, but this phase drives the logic circuits and is not critical. Subsequently parasitic capacitances were extracted from the layout and indicated that up to $1pF$ of additional capacitance was present on the clock lines. The most critical signals with high loads are ϕ_1 and ϕ_2 that drive the switched capacitors. In simulation the clock had a $860ps$ rise and fall time when driving a $2pF$ capacitor indicating adequate power to drive the calculated load.

The clock design was modified from Abo [5]. The inverters and NAND gates used in the clock design are mostly of basic size. The required delays to assure no overlap and the early fall of the primed signal are produced by the two sets of inverters indicated in the schematic of the clock in Figure A.5 in Appendix A. The channel length of these two sets of inverters are simply lengthened until the required delay is produced. The transistor sizes and resultant delays are given in Table 2.8.

2.5.3 Schematic and physical design

The schematic of the clock is found Figure A.4 in Appendix A. The physical layout is shown in Figure B.5 in Appendix B.

Inverter function	Time (<i>nsec</i>)	NMOS W/L ($\mu m/\mu m$)	PMOS W/L ($\mu m/\mu m$)
Non-overlap period	3	1.5/3.75	3/3.75
Early primed fall	3	1.5/5.4	3/5.4

Table 2.8: Dimensions of inverters responsible for non-overlap adjustments in the clock.

2.5.4 Clock buffers

The clock is centrally located on the chip and a current buffer is attached to each clock phase. A buffer consists of two inverters in series. The channel length of each inverter is $0.6\mu m$ and NMOS/PMOS ($\mu m/\mu m$) channel widths are 16.8/12 and 66.4/48.

The maximum current spike during clock switching when driving the $2pF$ capacitor was measured as $18mA$. This raised concern with respect to electro migration on the metal clock lines and contacts. Clock lines are $4\mu m$ wide for ϕ_1, ϕ_2 , and $\overline{\phi_2}$. A wide power bus is also supplying the clock.

2.6 Miscellaneous components

2.6.1 Basic Inverter

Design rational and performance

An early decision was made concerning the size of the basic converter. Based on the recommendation for MOSIS that all critical gates have a width of at least $3\mu m$, the NMOS of the inverter was selected to have an gate of size $W/L = 3\mu m/0.6\mu m$. This is referred to as the "basic" sized inverter. The PMOS was sized, given the NMOS constraint, to provide the minimum average inverter propagation delay. Given a high field mobility ratio of about 2/1 the PMOS $W/L = 3\sqrt{2} = 4.2\mu m/0.6\mu m$. The resulting propagation delays and noise margins are given in Table 2.9. Although these inverter gate sizes resulted in asymmetric noise margins, the effect is small as seen in the table.

The choice of the gates size resulted in a total inverter gate area of $4.32\mu m^2$ and given the process C_{ox} (Appendix C) a minimal inverter gate capacitance of $10.8fF$.

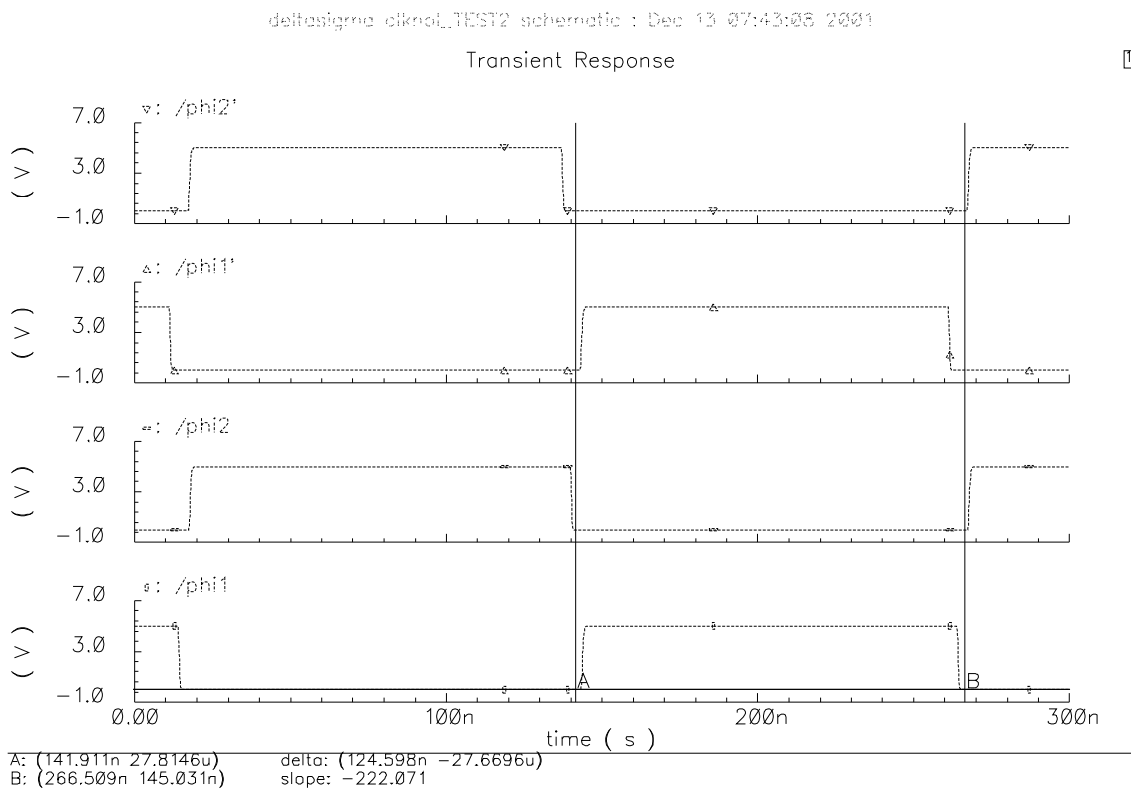


Figure 2.5: The four phases of the clock (ϕ_1 , ϕ_2 , ϕ'_1 , and ϕ'_2) each driving a $2pF$ load). The clock rate above is $4MHz$ and demonstrates the non-overlap intervals.

Parameter	Specification	Simulation Result
t_{ph-l}		83psec
t_{pl-h}		95psec
t_p		89psec
NM_{low}	$> 1.5V$	1.76V
NM_{high}	$> 1.5V$	2.55V

Table 2.9: Specifications of Basic CMOS Inverter

Physical layout rational

The inverter was designed physically to give the minimal area subject to the size of the NMOS and PMOS gates. Initially the inverter, as well as many other components, was designed with abundant body contacts and Metal 1 or Metal 2 input and output contacts. This almost invariably lead to inefficient designs as sub-components were aggregated to form larger circuits. As a result, several physical versions of the basic components are used; later versions were designed to postpone the decision of where to access basic components and place body contacts.

2.6.2 Logic Gates

Logic gates were constructed to be minimal size subject to the minimum width constraint mentioned in the inverter section above. All logic gates had channel lengths of $0.6\mu m$, but were widened to give current carrying capacity equivalent to the basic size inverter.

2.6.3 Transmission Gates

Several transmission gate configurations are used in this circuit. Design considerations included the dynamic range of the signal being gated and the amount of charge injection that resulted when the gate was used in conjunction with the switched capacitor circuits.

Design considerations

Two types of transmission gates are used: a simple NMOS transistor and a transmission gate consisting of an NMOS in parallel with a PMOS. The

NMOS only gate is suitable for the circuit input signal since the maximum magnitude of V_{in} is less than $3V$, well less than $V_{dd} - V_{TH}$, the voltage where the NMOS only gate resistance becomes very high. The full transmission gate is used at OTA outputs where voltages may approach $V_{dd} - V_{TH}$.

The NMOS only transmission gate has a significant space advantage over the parallel gate due to the absence of the inverter and the large PMOS.

A potential source of error is the charge injection from the transmission gates onto the capacitors. To a first order this is canceled by the differential configuration of the design. But, to the extent that the input voltage to a gate modulates this injection, an error may occur. The transmission gate configurations used, were chosen not because they had minimum charge injection, but because the charge injection was least affected by the input voltage.

The following simulation experiments illustrate this effect of charge injection. Figure 2.6 shows the testing circuit used. For each experiment one of the three transmission gates shown in Figure 2.7 was used. A DC voltage from -0.5 to $0.5V$ either side of V_{cm} was applied to the transmission gate and the clock was cycled. The resultant charge injected was read from the simulation output. The results are plotted in Figure 2.8. While the dummy gate in conjunction with the NMOS has the least absolute charge injection, it is dependent on the input voltage. The NMOS alone has a greater amount of charge injection, but a differential configuration would fully eliminate the effects of charge injection. The full NMOS/PMOS transmission gate performs less well than the other two configurations with respect to both absolute charge injection and input modulation. Unfortunately this latter gate must be used at the intermediate SDM stages because of the large signal swing.

2.7 Input output pads

An approved set of probe pads was provided by MOSIS. Two modifications of the the pad_io design were made to allow for buffering digital and analog signals. The parameters below were verified with simulation.

2.7.1 Analog buffer

The analog buffer schematic and layout is shown in Appendix A and B. This buffer is linear to within $40mV$ over the output range of the OTAs

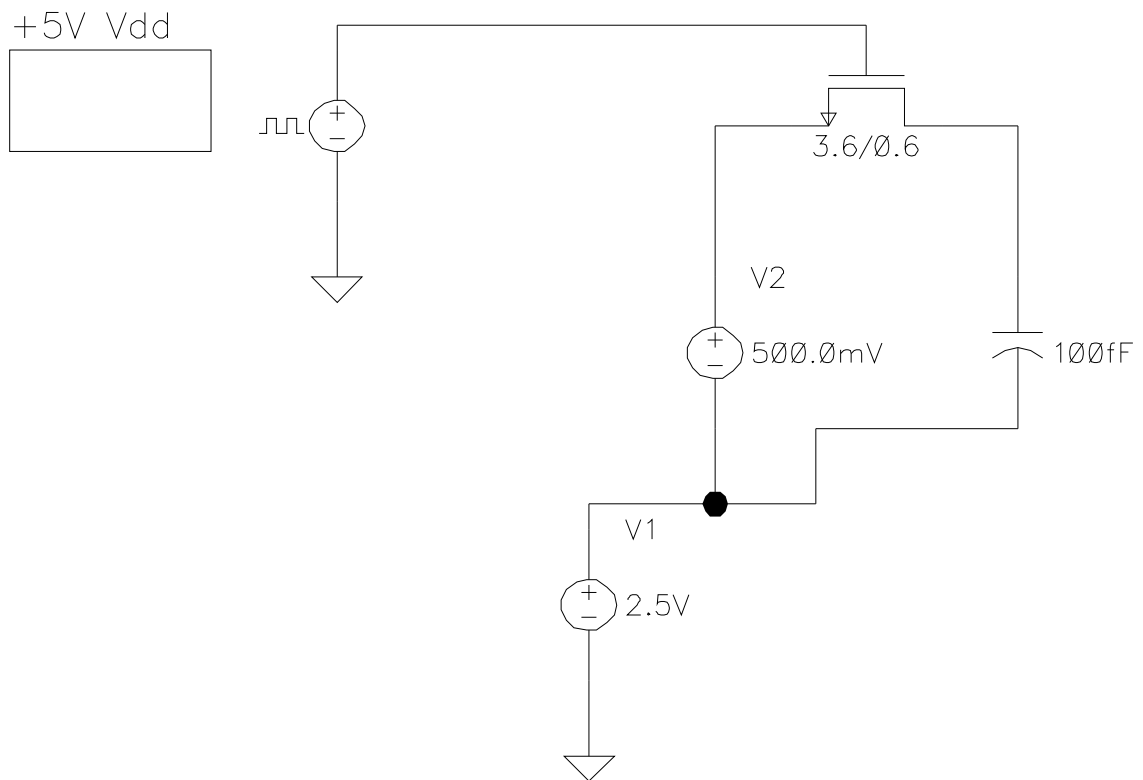


Figure 2.6: Transmission gate testing circuit.

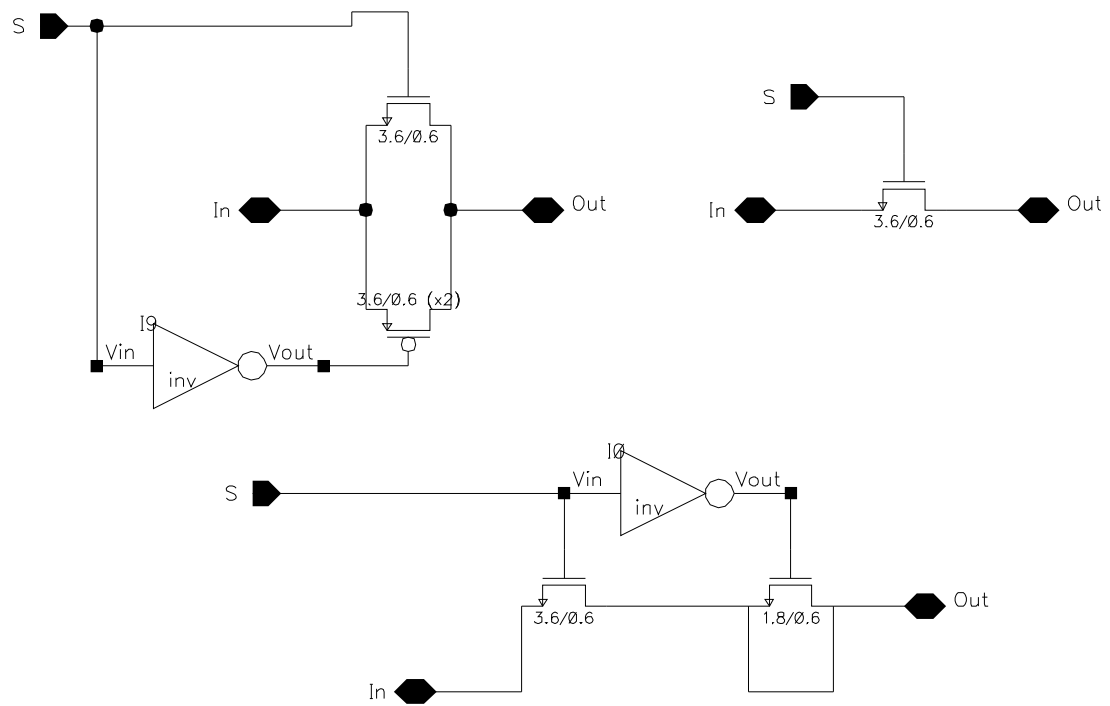


Figure 2.7: Three transmission gates tested.

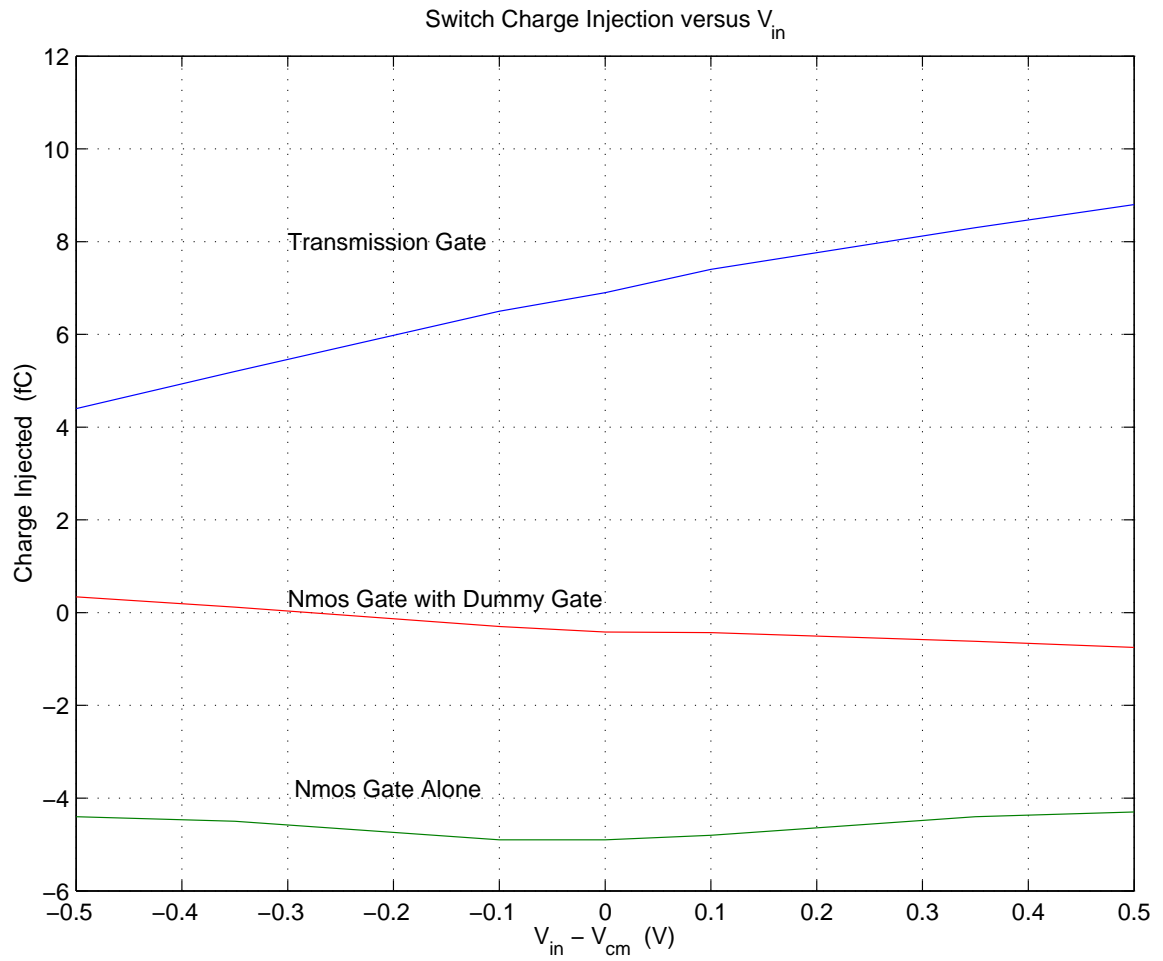


Figure 2.8: Results of transmission gate testing.

and is capable of driving a $20pF$ load. Figure 2.9 shows the output from an OTA and the corresponding waveform at the output pad. The maximum difference between the waveforms is $30mV$.

2.7.2 Digital buffer

The circuit consists of four serially chained inverters with channel lengths of $0.6\mu m$ and NMOS/PMOS ($\mu m/\mu m$) channel widths of 4.2/3.0, 12/6, 36/18, and 108/54. The digital buffer layout is shown in Appendix B. This buffer is capable of driving a $20pF$ load with a rise and a fall time of less than $6ns$.

2.8 Bypass capacitors

2.8.1 Component function

By-pass capacitors between V_{dd} and gnd serve to stabilize the on-chip supply voltages. It is desirable to maximize this capacitance.

2.8.2 Design and physical layout rational

The modulator capacitors occupied a large are of the die, but poly layers below Metal 1 were available under the modulator capacitors. Poly 2 is connected directly to Metal 1 ground plane and this leads to good conduction to the periphery of the top plate. There is not good access to the central part of the Poly 1 layer, but the roughly triangular shape and the circumferential access causes the bottom plate resistance to be limited. Regardless, the by-pass capacitance still functions well since the inclusion of bottom plate resistance only reduces the effective size of the capacitor. The bottom plate is connected to V_{dd} .

In addition, at the end of the project, any significant areas of vacant silicon were filled with by-pass capacitance.

The total by-pass capacitance is $260pF$.

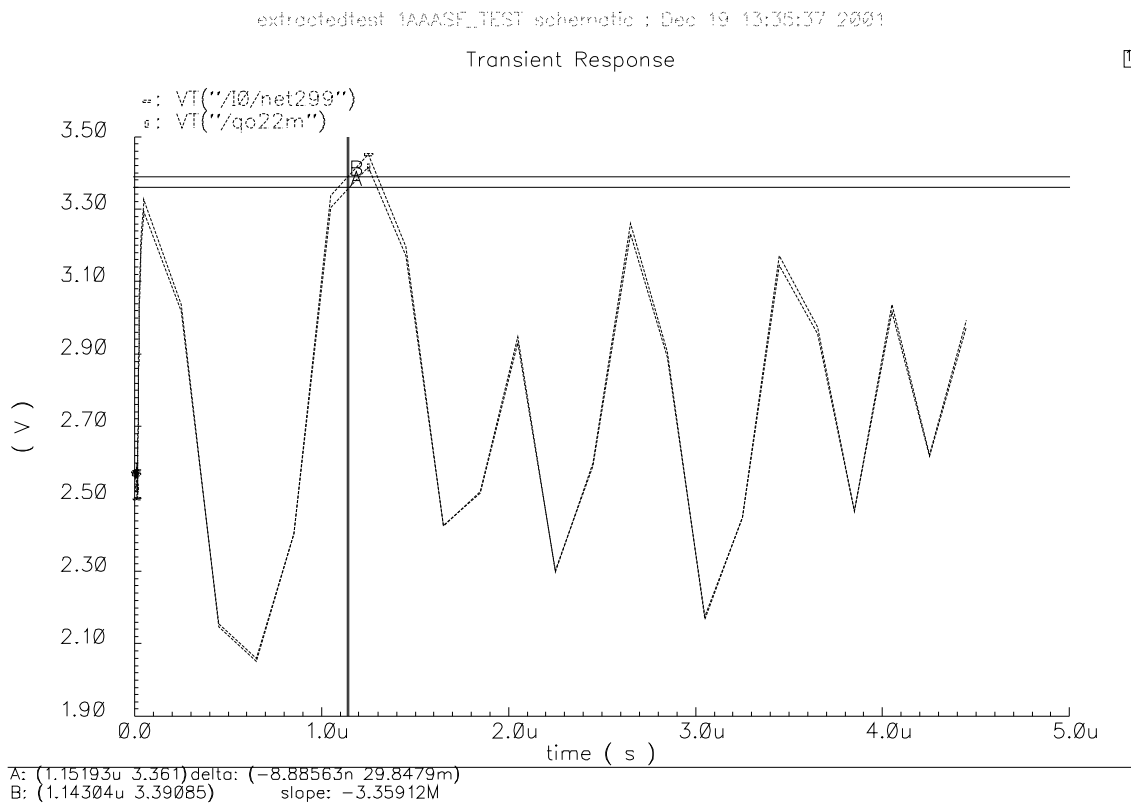


Figure 2.9: Comparison of one OTA voltage output and the voltage at the corresponding output pad for a $5\mu\text{s}$ simulation (no load).

3 Circuit Verification

Overall circuit verification was done in several ways. These tests included design checks built into Cadence and specifically designed simulations of circuit schematics. These tests are discussed below.

3.1 Design Check

Before being sent to the foundry, the schematic and layout of the top level circuit were checked for errors. Design Rule Check (DRC), extraction, and Layout versus Schematic (LVS) showed no errors.

The following is the output from running LVS on the top level schematic.

```
@(#)CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $
```

```
Like matching is enabled.
```

```
Net swapping is enabled.
```

```
Using terminal names as correspondence points.
```

```
Net-list summary for /cadence/LVS/layout/netlist
count
1838 nets
60 terminals
141 cap
3138 pmos
2804 nmos
```

```
Net-list summary for /cadence/LVS/schematic/netlist
count
1762 nets
60 terminals
70 cap
1784 pmos
1966 nmos
```

Terminal correspondence points

- 1 BI1
- 2 BI2
- 3 BQ1
- 4 BQ2
- 5 CLK
- 6 D1
- 7 D2
- 8 INVtest
- 9 Ntest1
- 10 Ntest2
- 11 Ntest3
- 12 Ntests
- 13 OPin
- 14 OPout
- 15 Phi1
- 16 Phi1prime
- 17 Phi2
- 18 Phi2primebar
- 19 Ptest1
- 20 Ptest2
- 21 Ptest3
- 22 Ptests
- 23 Qbar
- 24 R50in
- 25 RSTbar
- 26 SH
- 27 Ttest
- 28 VCM
- 29 VINminus
- 30 VINplus
- 31 VRminus
- 32 VRplus
- 33 capcal1b
- 34 capcal1t
- 35 capcal2b
- 36 capcal2t

```
37 f0
38 f1
39 f2
40 f3
41 gnd!
42 i0
43 i2
44 i3
45 i4
46 inotaminus
47 inotaplus
48 ota11minus
49 ota11plus
50 ota12minus
51 ota12plus
52 ota21minus
53 ota21plus
54 ota22minus
55 ota22plus
56 q0
57 q2
58 q3
59 q4
60 vdd!
```

The net-lists match.

```
        layout schematic
instances
un-matched 0 0
rewired 0 0
size errors 0 0
pruned 0 0
active 6083 3820
total 6083 3820

        nets
un-matched 0 0
```

```
merged 0 0
pruned 0 0
active 1838 1762
total 1838 1762
```

```
terminals
un-matched 0 0
matched but
different type 0 0
total 60 60
```

Probe files from /cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

3.2 Top Level Simulation Results

Due to the averaging nature of the sigma-delta ADC, many samples are needed in order to achieve the full resolution of the converter. This proved to be a limiting factor in the simulation of the fully assembled schematic. While the converter running at a sample rate of f_s creates a new valid output every $\frac{1}{f_s}$ seconds, calculations are needed for many other time points in order to obtain valid outputs. A test on the top level design can take up to 18 hours to obtain 1000 samples of output data. As a result of the large calculation time needed for such a small data set, very few tests were run at the top level. Most often the performance of the circuit was evaluated by simulating one-half of the chip, using either the in-phase or quadrature channel alone. Fortunately this did allow for the verification of the basic design functions, such as frequency modulation and the effects of sigma delta conversion on the spectrum. True measures of the overall resolution of the converter have been hard to obtain while evaluating such small output data sets. Some tests are currently running and many others remain to be performed regarding the effects of different input signals, different reference voltages, temperature and parasitics.

Code was written for the MATLAB software package to simulate the circuit mathematically in order to gain some insight on expected performance. The narrow bandwidth of the output spectrum near DC is shown in Figure 3.1 for a simulation using 32 kilo samples. The improvement in using two stages is clearly evident, as the shaping in the second order and fourth order systems is quite different. MATLAB simulation with a smaller number of samples, as the 1 kilo sample used in the schematic simulations, generated the output spectrum of Figure 3.2. There is very little improvement in resolution from a second order to a fourth order system. The same results are seen in the output spectrum of a schematic simulation with 1 kilo sample of

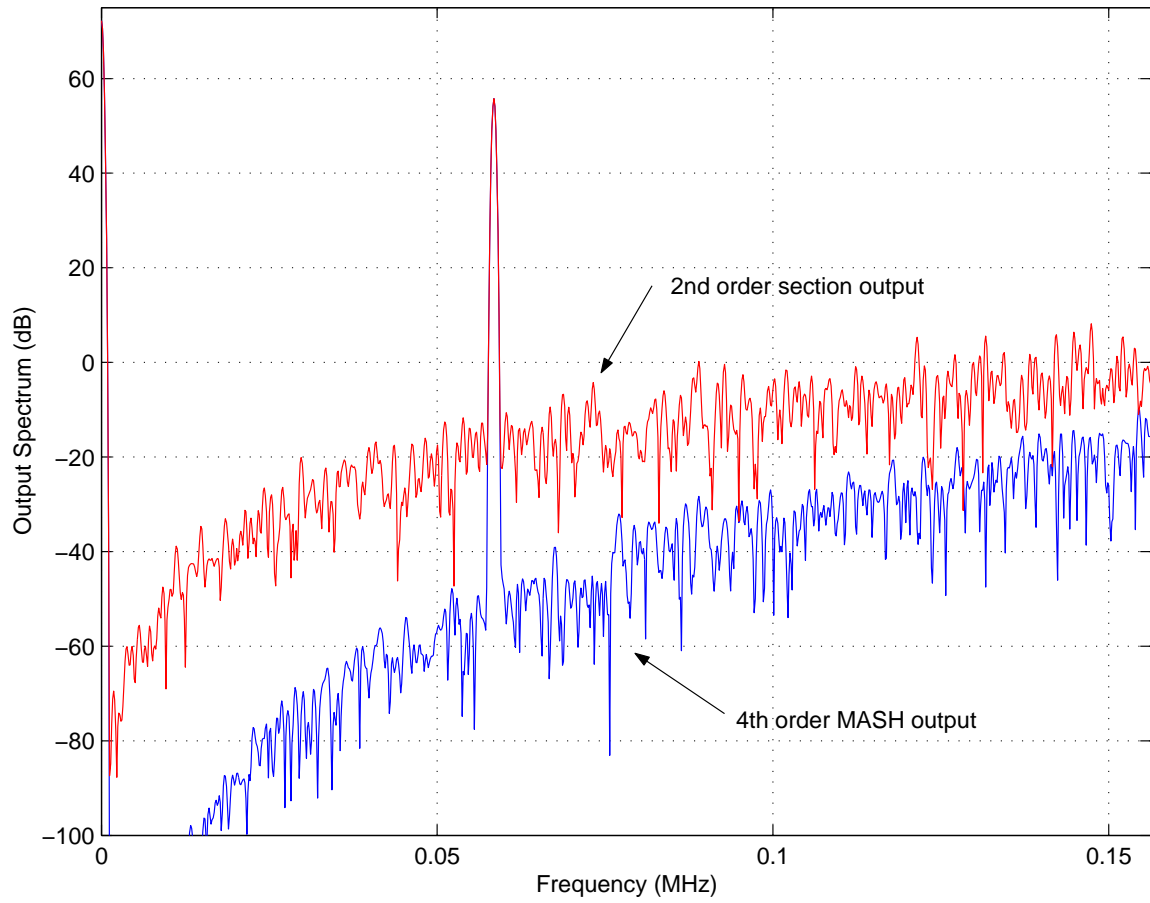


Figure 3.1: Simulated results from MATLAB w/ 32k samples.

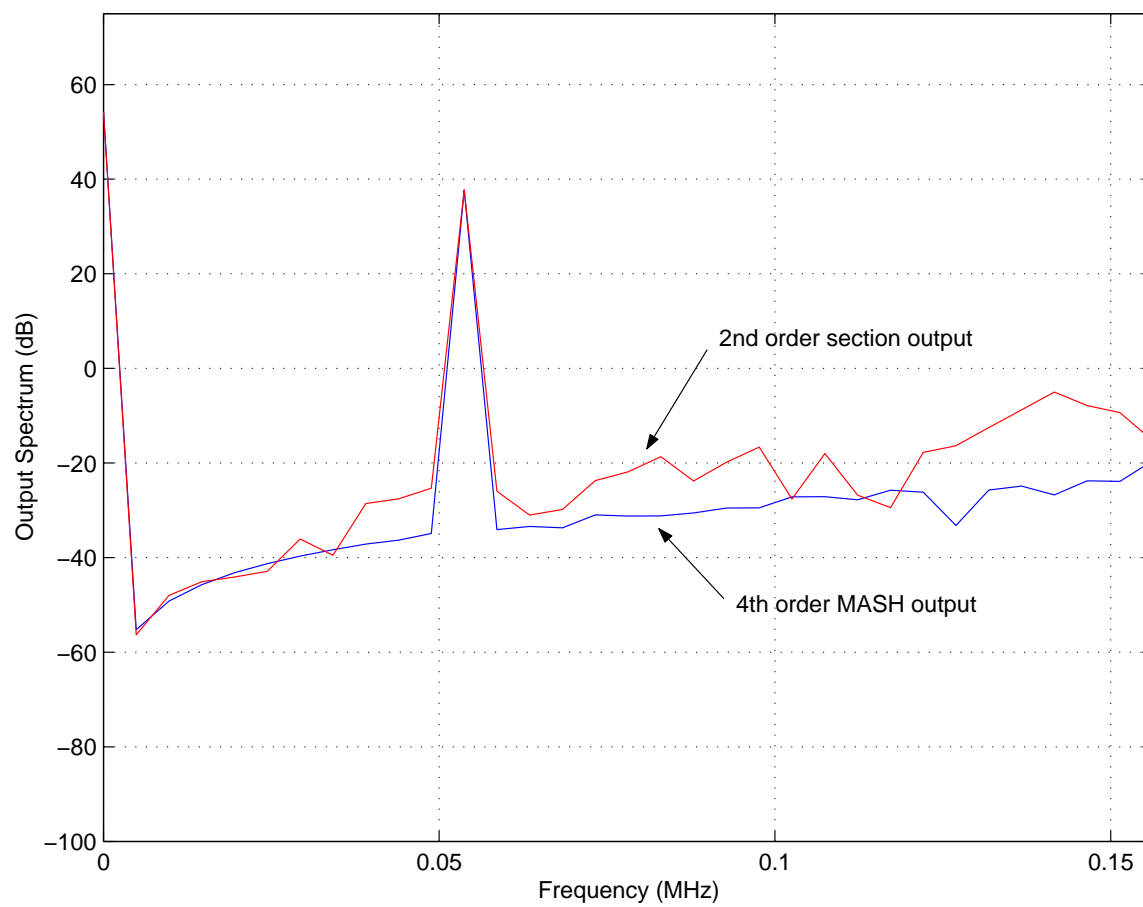


Figure 3.2: Simulated results from MATLAB w/ 1k samples.

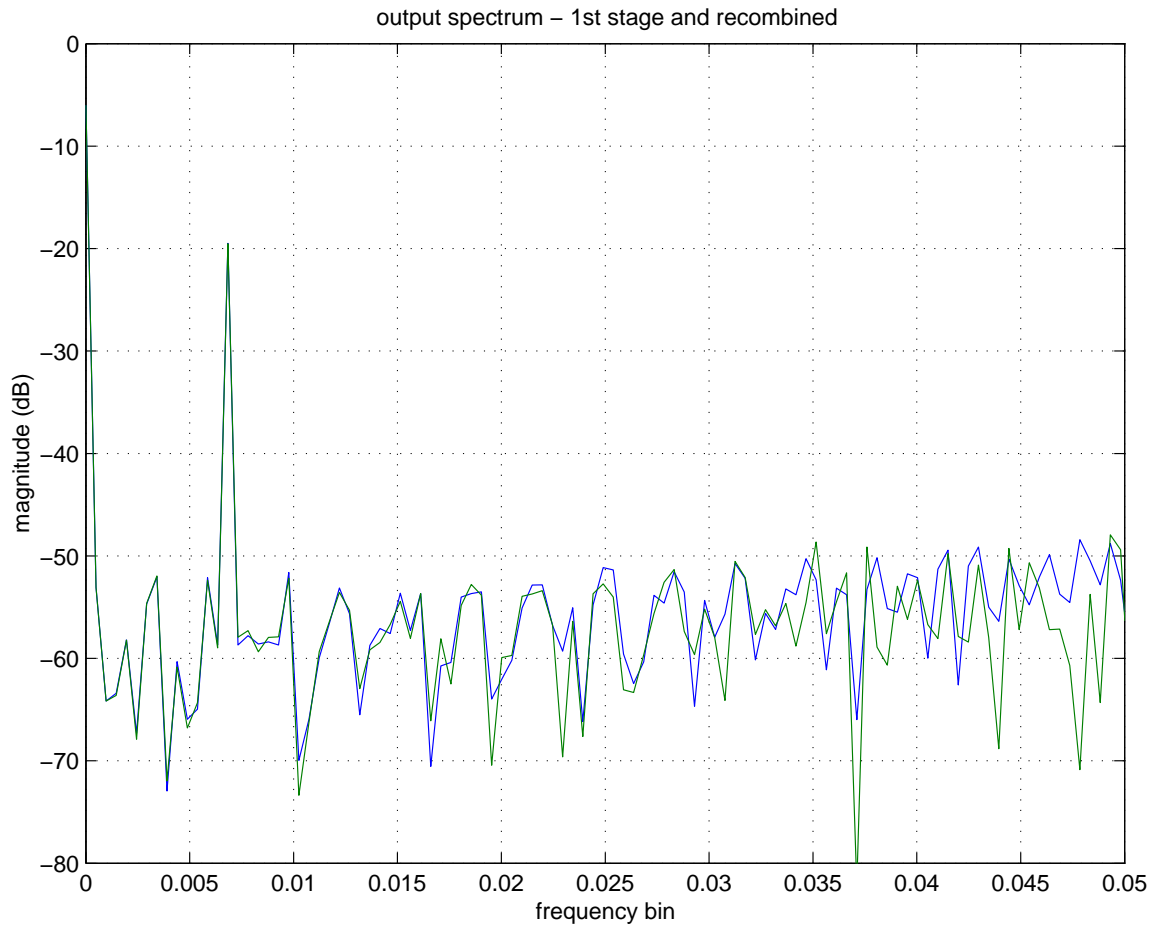


Figure 3.3: Simulated results from schematic w/ 1k samples.

output data, shown in Figure 3.3. In both of the output spectra, the recombined output of the two stages closely follows the output of the first stage. This comparison lends some validity to the idea that the circuit will operate as designed. The difference in scale between the resolution of the MATLAB and schematic simulations for 1 kilo sample of data can be attributed to the fact that the MATLAB simulation is ideal. There are no considerations for things such as parasitic capacitances in the MATLAB simulation, whereas the schematic simulation gives a much more realistic view of the performance of the circuit.

The error between the stages also appeared to show the predicted effects despite the small data set. The error from the first stage quantizer is plotted versus input state in Figure 3.4. The curve that appears through the data is the average value of the error for the given input state. Ideally this curve would be flat across the input range, indicating that the error is truly independent of the input signal. Second stage quantizer error is plotted in Figure 3.5, along with the average value curves for both the first and second stages for comparison. The second stage error does appear to be somewhat more random with respect to the input, with an average value curve that is marginally flatter than that of the first stage. Again, more samples would help to validate these claims.

A schematic simulation of the top level circuit obtained 500 data points to show complex modulated output samples produced by the converter. The output spectrum of the converter is shown in Figure 3.6. The input is a two-tone signal, near bins 4 and 6, which is modulated by $\frac{f_s}{32}$, and the converter is operated at a sample rate of 5MHz. The noise shaping of the fourth order system is seen in the high noise floor near the middle of the spectrum. The complex modulation can also be seen in the presence of four tones near DC and the absence of any tones near f_s . The complex modulation shifts the entire spectrum to the right by $\frac{512}{32}$ or 16 bins, translating the the two input tones and their images (which are near f_s) to be centered around $\frac{f_s}{32}$ instead of DC. While the input signal has been modulated out of the bandwidth of highest resolution, this test serves to show that the circuit can generate complex modulated outputs, and that the modulator appears to work as designed.

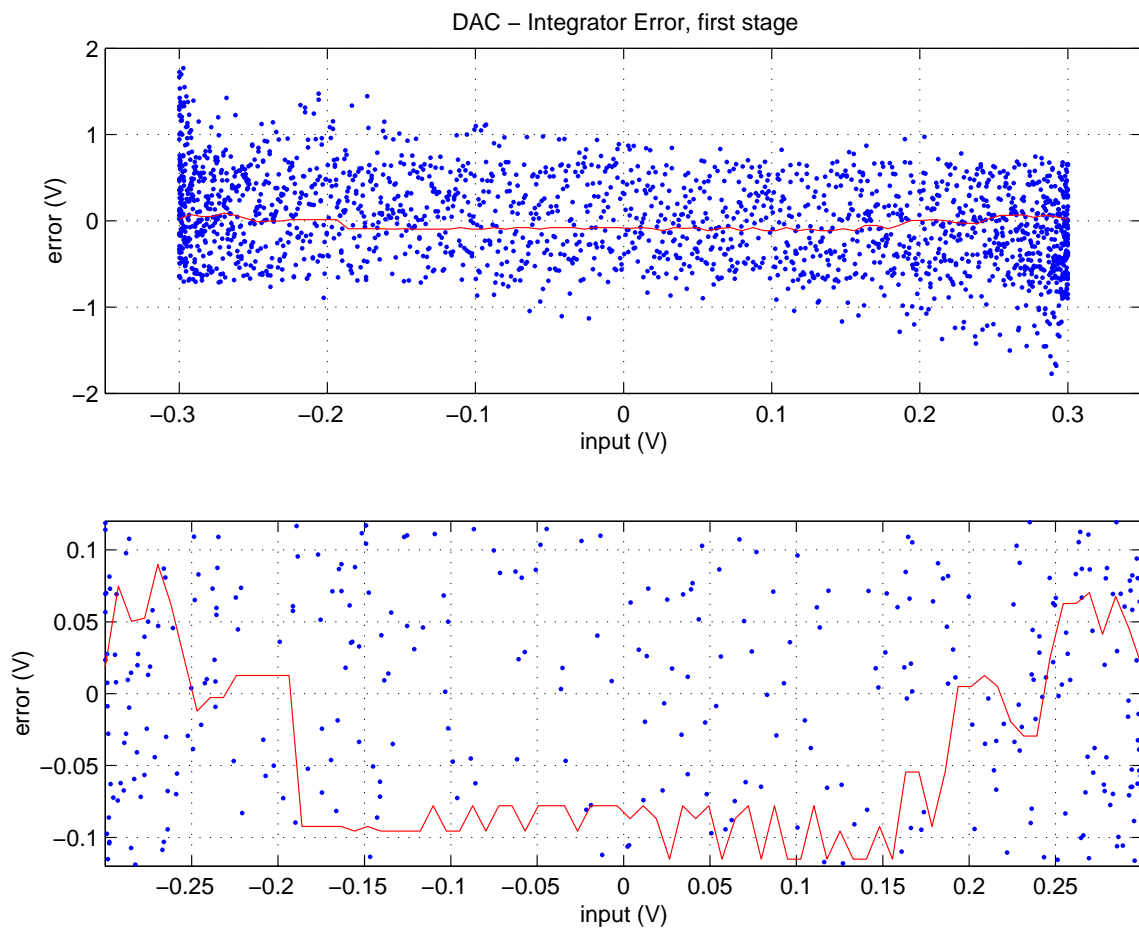


Figure 3.4: Simulated results (full range and a closer look, with average value curve) from schematic w/ 1k samples.

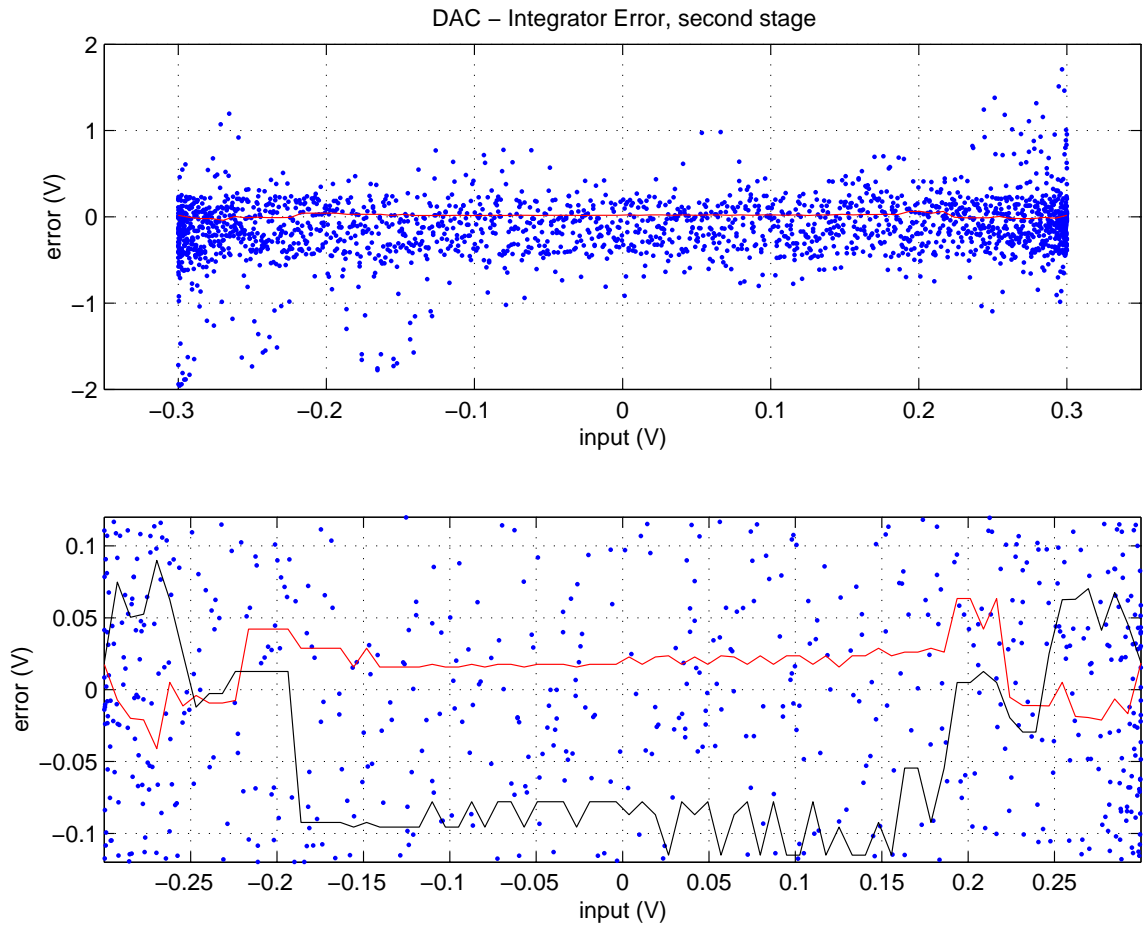


Figure 3.5: Simulated results (full range and a closer look, with average value curves from both stages) from schematic w/ 1k samples.

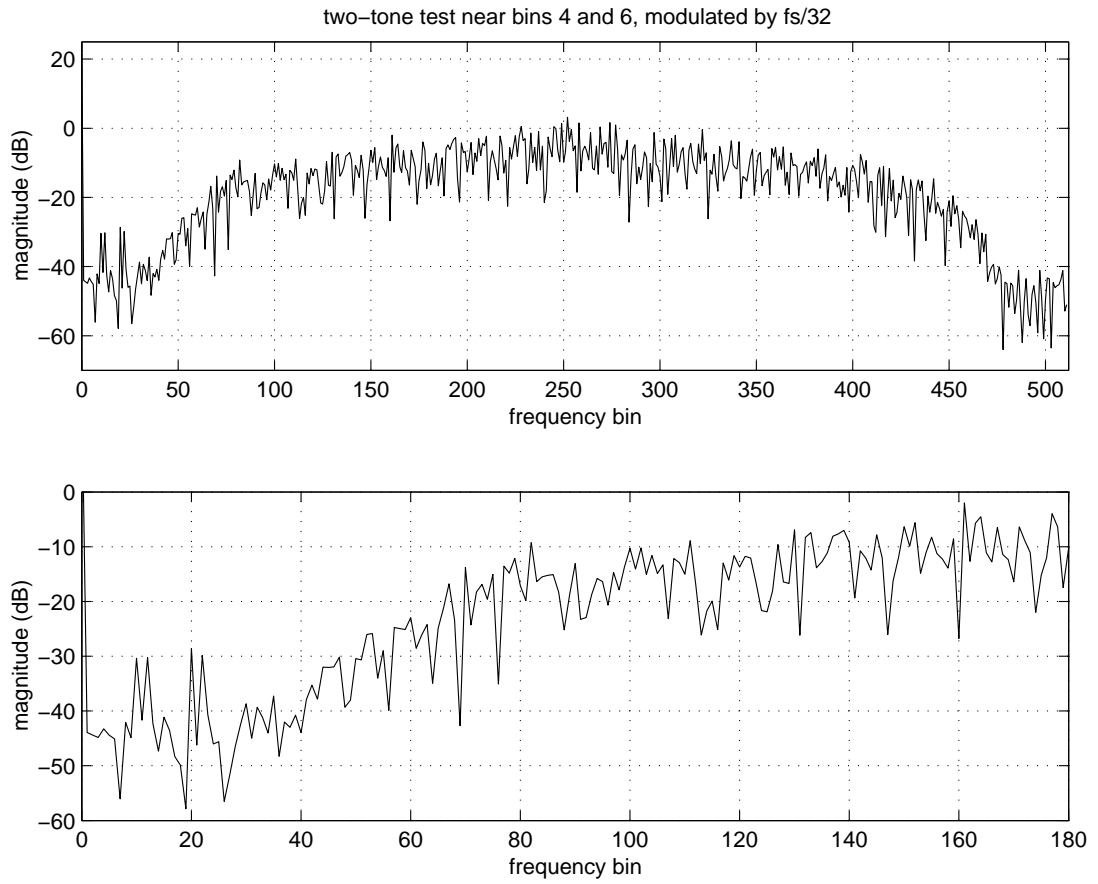


Figure 3.6: Simulated results (full spectrum and a closer look) from top level schematic w/ 500 samples, modulated by $\frac{f_s}{32}$.

3.3 On-chip voltage and current demand

The effectiveness of the by-pass capacitor was assessed by adding the package pin inductance, capacitance, and resistance to the supply pins and observing the supply voltage and current. Major parasitic capacitances are also included in this simulation. Figure 3.7 shows the variations in current and supply voltage on the chip for a full clock period when running at $5MHz$. The on chip voltage is $5V \pm 100mV$ with the deviations in V_{dd} occurring at the switching of the clock. Average current is $14mA$ with peaks as high as $40mA$. The frequency of the ripple in the voltage is approximately what is expected from the power pin inductance and by-pass capacitor.

The by-pass capacitance was reduced from $260pF$ to $1pF$ and the simulation was repeated (Figure 3.8.) In the absence of the by-pass capacitor the voltage varied $\pm 400mV$. The frequency of the ripple also was higher, and died out more quickly when the by-pass capacitor was absent.

Clearly the by-pass capacitor buffered on-chip supply voltage, reducing voltage the variations by a factor of four. The by-pass capacitor also slowed the decay of the ripple. The net effect was that at the end of a clock phase the on-chip ripple in the supply voltage was about $2mV_{pp}$ when the by-pass capacitor is present compared to $1mV_{pp}$ when the bypass capacitor is absent. It is interesting to note that at the beginning of an clock cycle it is probably not important that the OTA is supplied with an absolutely stable voltage. Where as the end of the cycle when the differential input voltage of the OTA has returned to zero, a stable supply would be desirable. Ironically the by-pass capacitor causes a less stable level at this time. Fortunately both situations lead to only a few millivolts, hopefully less than the noise floor.

3.4 Performance with temperature variations.

The chip will be packaged using a DIP40 package. At room temperature in still air the package temperature rises at $25 \text{ deg } C/W$. Given the power consumption of this design the anticipated temperature rise is less than $2 \text{ deg } C$.

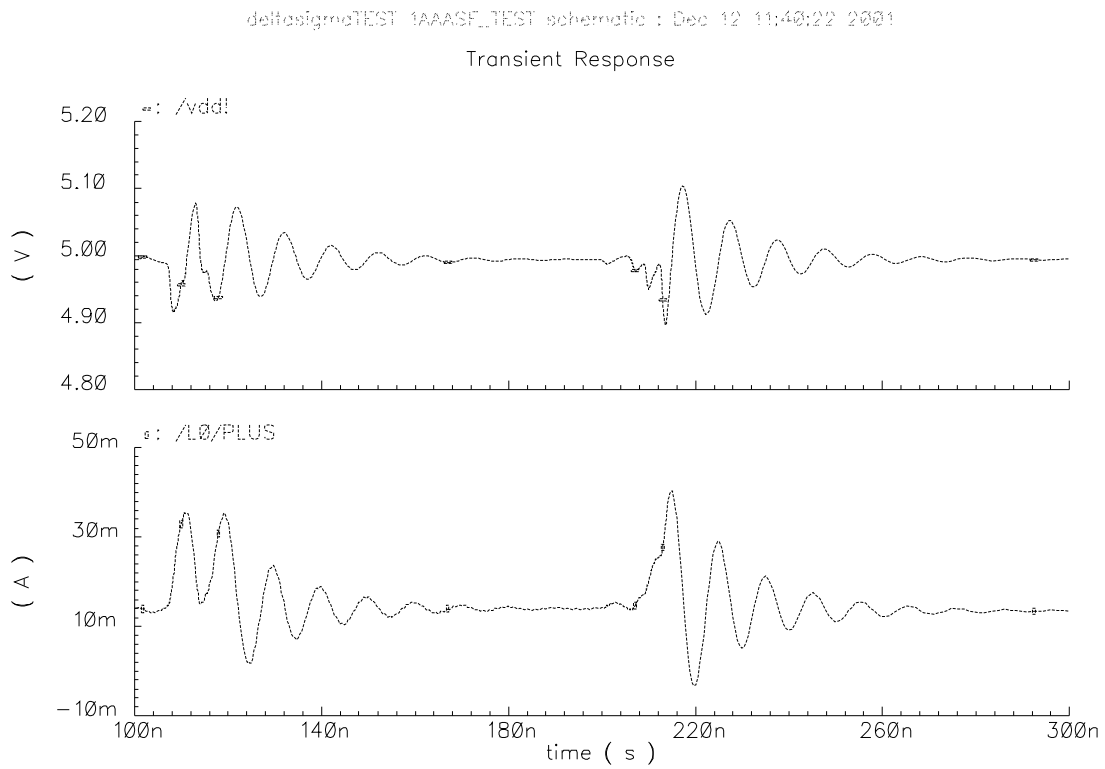


Figure 3.7: On chip V_{dd} and supply current. Simulated with a total lead inductance of $4nH$ on the power pins and eight output bits loaded with $20pF$ each.

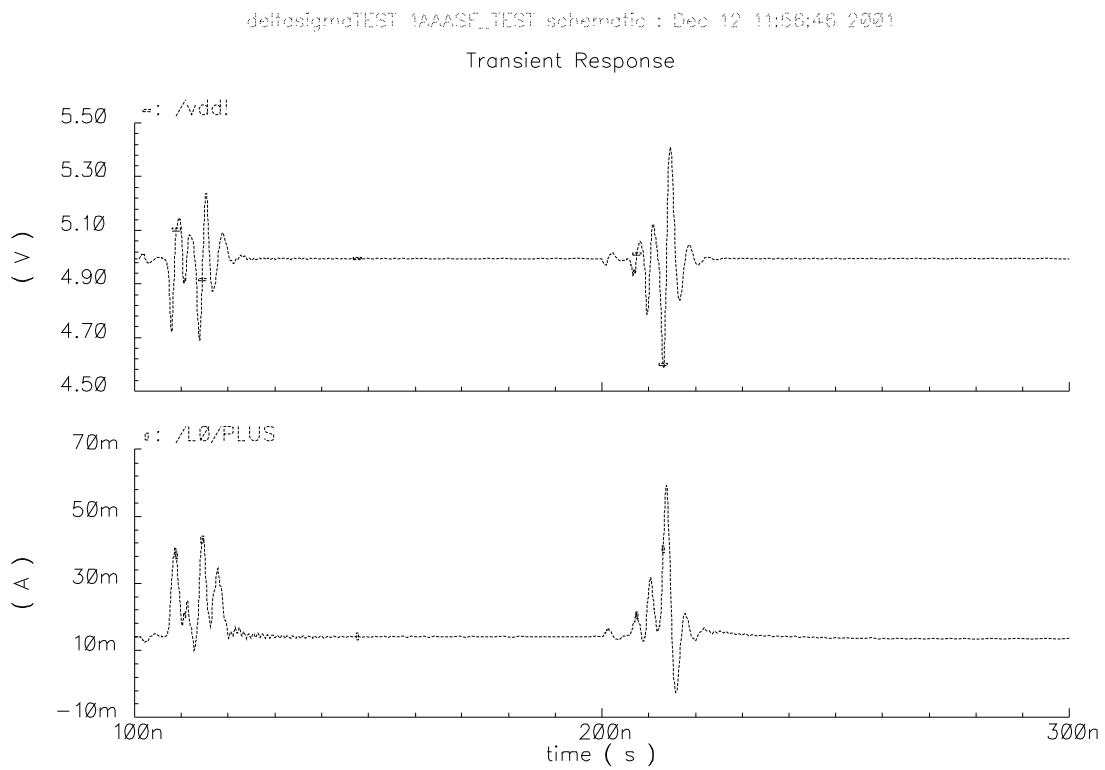


Figure 3.8: On chip V_{dd} and supply current. Same conditions as Figure 3.7 except without the on chip by-pass capacitance.

4 Circuit Testing

Circuit testing will be done upon the return of the fabricated chip from the foundry. The first section of this chapter describes the built in testing connections.

4.1 Testing circuits

The Table 4.1 gives a table of the additional probe pads added to the circuit. In addition to the eight major output pins, pins 3–7, 13–19, 24, 25, 32, and 33 on the package are also used for testing. Each of the testing pins are briefly discussed below. Probe pads numbering corresponds to the previous pin number appended with a letter. The letter is added alphabetically to the next pad encountered when moving the row of pins to the row of probe pads.

4.1.1 Probe calibration

Probe pad connections R_{50in} , R_{50out} , SH_1 , SH_2 , OP_{in} , OP_{out} , are connections either end of a 50Ω resistor, a short circuit, and an open circuit used for calibration of the probes.

4.1.2 On chip voltage verification

V_{dd} and several *gnd* probe pads are present for measuring the on chip supply voltage. V_{cm} , V_{ref}^+ , and V_{ref}^- allow measurement of these inputs internally.

4.1.3 Capacitor linearity

The four probe pads *capcal1b*, *capcal1t*, *capcal2b*, and *capcal2t* allow access to the bottom and top plates of $800fF$ capacitors made of poly1:poly2, and Metal1:Metal2. The intention is to measure the linearity of these two capacitor types.

Name	Location	Function
R_{50in}	5a	50 Ω for probe calibration
R_{50out}	5b	50 Ω for probe calibration
SH_1	5c	Short circuit for probe calibration
SH_2	5d	Short circuit for probe calibration
OP_{in}	5e	Open circuit for probe calibration
OP_{out}	5f	Open circuit for prove calibration
Gnd	5g	Power
V_{dd}	5h	Power
V_{cm}	15a	Reference voltage
V_{ref}^+	15b	Reference voltage
V_{ref}^-	15c	Reference voltage
Gnd	15d	Power
capcal2b	15e	800fF poly capacitor
capcal2t	15f	800fF poly capacitor
Ptest2	25a	Transistor test. Channel length 1.8
Ptest1	25b	Transistor test. Channel length 0.6
Testt	25c	Transistor test. All gates
Ntest1	25d	Transistor test. Channel length 0.6
Ptest3	25e	Transistor test. Channel length 3.0
Ptests	25f	Transistor test. PMOS sources
Ntest2	25g	Transistor test. Channel length 1.8
Ntests	25h	Transistor test. NMOS sources
INVtest	25i	Transistor test. Inverter output
Ntest3	25j	Transistor test. Channel length 3.0
capcal1t	35a	800fF metal capacitor
capcal1b	35b	800fF metal capacitor
ϕ_2	40a	Clock
ϕ_1'	40b	Clock
ϕ_1	40c	Clock
ϕ_2'	40d	Clock
Gnd	40e	Power

Table 4.1: Table of Probe Pads

4.1.4 Transistor Tests

The probe pads 25a to 25b give access to measure some basic device parameters. Six transistors and a basic inverter all contain a common gate input (Testt). The drains and sources of each of the NMOS and PMOS transistors are individually accessible. All individual transistors have gate widths of $3\mu m$ (NMOS) or $4.2\mu m$ (PMOS) wide. Three channels lengths for each type of transistor is present; 0.6, 1.8, and $3.0\mu m$.

4.1.5 Clock signals

Four of the seven clocks are present on probe pads so that the relative overlap of the clock signals can be assessed.

4.1.6 Quadrature SDM

Package pins 3 – 7 and 13 – 19 give access to the intermediate signals of the quadrature SDM. These include the the input to the first OTA. and the outputs of each of the four OTAs. See Table 1.2 for definitions.

Additionally pins D1 and D2 give the voltage fed back on to the positive side of the two MASH stages. The values on the pins D1 and D2 are routed through analog pins containing our analog buffer design. Their value should be V_{ref}^+ or V_{ref}^- , therefore the actual value found on these pins will give an estimate of the accuracy of our analog buffer.

4.1.7 Digital stage outputs

The pins 24, 25, 32, *and*, 33 are the bit streams generated by each of the MASH stages that are used as inputs to the digital filters.

4.2 Tests of Device

The following tests were proformed on the fabricated device. Five samples are available for testing they are labeled T1CK-AM (numbers 1 through 5.)

4.2.1 Static Power Test

Purpose:

Approximate the power used by the chip and test for gross defects in fabrication and/or design.

Theory:

Simulations of the circuit with a 5 V supply and a 5 MHz clock yielded an average current of 14 mA. An average of above 20 mA would be cause for concern.

Equipment:

1. T1CK-AM (#2)
2. Voltage supply
3. 100Ω resistor
4. Volt meter.

Procedure:

Power the T1CK-AM through a 100Ω source resistor in series with the supply and vdd. Gradually increase the supply voltage at V_{dd} to 5V while observing the current through a 100Ω source resistor. No clock signal is applied.

Results:

At Vdd of 5V the 100Ω resistor dropped 0.5V. Static current is 5mA and static power consumption is 25mW.

Conclusion:

Static power consumption is well within expectations.

4.2.2 Capacitor Bank Modulator Test

Purpose:

Verify the function of the sequencing of the modulating capacitors.

Theory:

The waveform at the input to the first stage of the sigma-delta modulator will depend on the modulating frequency as well as the the signal applied. A DC signal at the input will appear as a sinusoid at the first stage input if the quantized band selected for conversion is other than the baseband.

Equipment:

1. T1CK-AM (#1)
2. Evaluation test board.
3. Oscilloscope

Procedure:

1. Apply a $200mV$ DC signal to the input of the ADC.
2. Apply a 4 MHz clock input
3. Set the band select bits to $f_0f_1f_2f_3 = 0000$ (pins 23,22,2,38) and record the frequency of the inputs to the first stage (pins 3 or 4).
4. Repeat by setting each pin to 1, one pin at a time.

Results:

The results are given in Table 4.2.

Conclusion:

1. The frequency shifting functions in units of $f_s/32$ is possible.
2. The bit labels ($f_0f_1f_2f_3$) on the board are reversed relative to the design description of the ADC.

$f_0f_1f_2f_3$	Shape	Period ($\mu m sec$)	Frequency ($k Hz$)
0000	DC	-	0
0001	Stepped sinusoid	8	$125(f_s/32)$
0010	Stepped sinusoid	4	$250(f_s/16)$
0100	Stepped sinusoid	2	$500(f_s/8)$
1000	Stepped sinusoid	1	$1000(f_s/4)$

Table 4.2: Signal at first integrator input stage given the frequency select settings.

4.2.3 Baseband Signal A/D Conversion Test

Purpose:

Verify the function of Sigma-Delta A/D Converter with input test frequencies near baseband (DC). Verify function of the digital filter at the output of the In-Phase half of the circuit.

Theory:

The circuit will behave as a conventional sigma-delta ADC when the frequency select bits are all set low. The modulator is disabled and the largest sampling capacitor is always used at the input to the first integrator. The quadrature side uses only the smallest sampling capacitor, so its output is greatly diminished. The accuracy of the digital filter in the in-phase half of the circuit can be checked by calculating output values from the raw outputs of the two stages.

Equipment:

1. T1CK-AM (#1)
2. Evaluation test board w/power supply
3. HP 8642A Signal Generator
4. HP 8645A Agile Signal Generator
5. Tektronix 9504 Fast Data Cache

6. Unix work station running Matlab

Procedure:

1. Set the frequency select bits $f_3f_2f_1f_0 = 0000$.
2. Apply 4.096MHz clock signal with an amplitude of 850mV to the clock input of the test board.
3. Apply 101.125kHz test signal with an amplitude of 120mV to the signal input of the test board.
4. Collect 32768 samples using data cache.
5. Process data in Matlab.

Results:

The frequency spectrum of the digital signal taken from the output of the Sigma-Delta A/D Converter appears in Figure 4.1. There is significant noise shaping of higher frequencies, and the signal appears on the correct bin for the given sample rate. The digital filter had 28 errors out of 32768 samples calculated, and those results appear in Figure 4.2.

Conclusion:

The Sigma-Delta A/D Converter is working as expected, although the flattening of the spectrum near DC shows a loss in resolution of the converter. The digital filter on the in-phase side is working as expected. The errors could be attributed to the difference in timing between the on-chip clock and the drivers on the test board that send the outputs to the data cache. The on-chip clock is not pinned out, which makes alignment difficult. Ongoing tests are focused on the slope of the noise floor near DC and the timing of the circuit in relation to the data cache.

4.2.4 Modulated Signal A/D Conversion Test

Purpose:

Verify the function of Sigma-Delta A/D Converter with input test frequencies outside of baseband (i.e. greater than f_s/OSR) for this converter. Verify

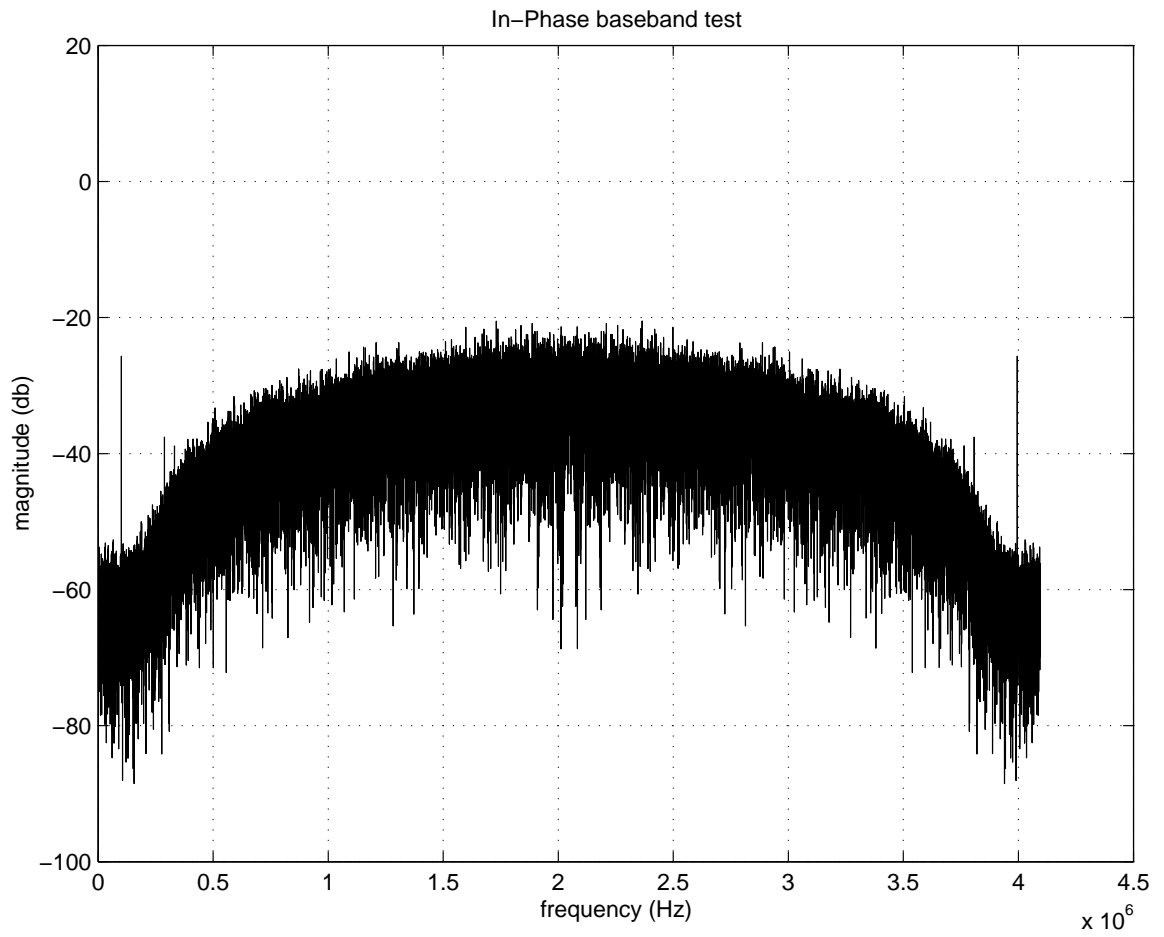


Figure 4.1: Baseband Test Data

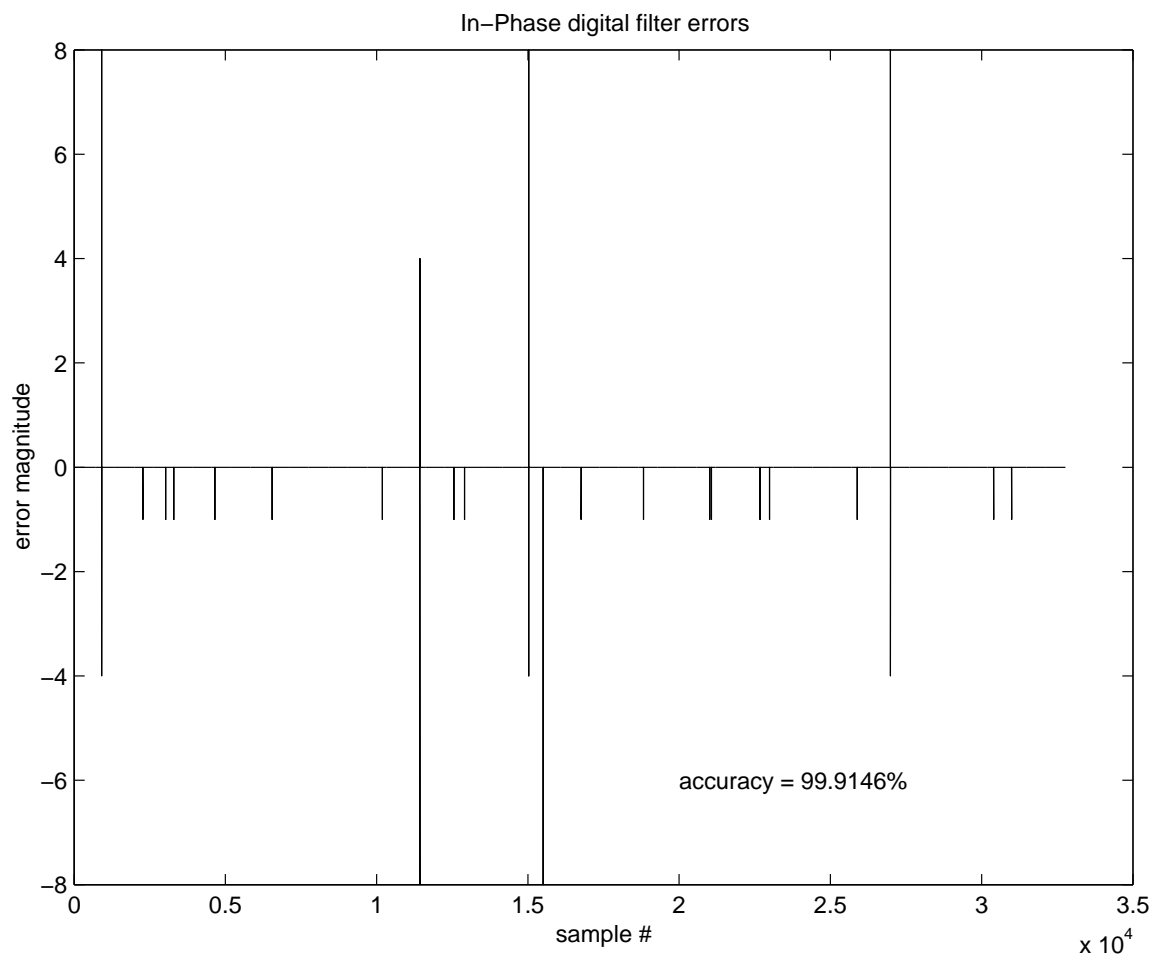


Figure 4.2: Digital Filter errors in baseband test

function and accuracy of the digital filter at the output of both the In-Phase and Quadrature halves of the circuit.

Theory:

The modulator will shift the frequencies of interest down near baseband, so that the Sigma-Delta A/D Converter will process the signal as a baseband input. Both the In-Phase and Quadrature channels will use the modulating capacitors, so the signal should be processed by both converters. When the outputs from the two sides are added together, the image frequency of the input signal will be cancelled.

Equipment:

1. T1CK-AM (#1)
2. Evaluation test board w/power supply
3. HP 8642A Signal Generator
4. HP 8645A Agile Signal Generator
5. Tektronix 9504 Fast Data Cache
6. Unix work station running Matlab

Procedure:

1. Set the frequency select bits $f_3 f_2 f_1 f_0 = 0111$, which will set frequency of modulation on the input signal to $7 * f_s / \text{OSR} = 896\text{kHz}$.
2. Apply 4.096MHz clock signal with an amplitude of 850mV to the clock input of the test board.
3. Apply 853.125kHz test signal with an amplitude of 120mV to the signal input of the test board.
4. Collect 32768 samples using data cache.
5. Process data in Matlab.

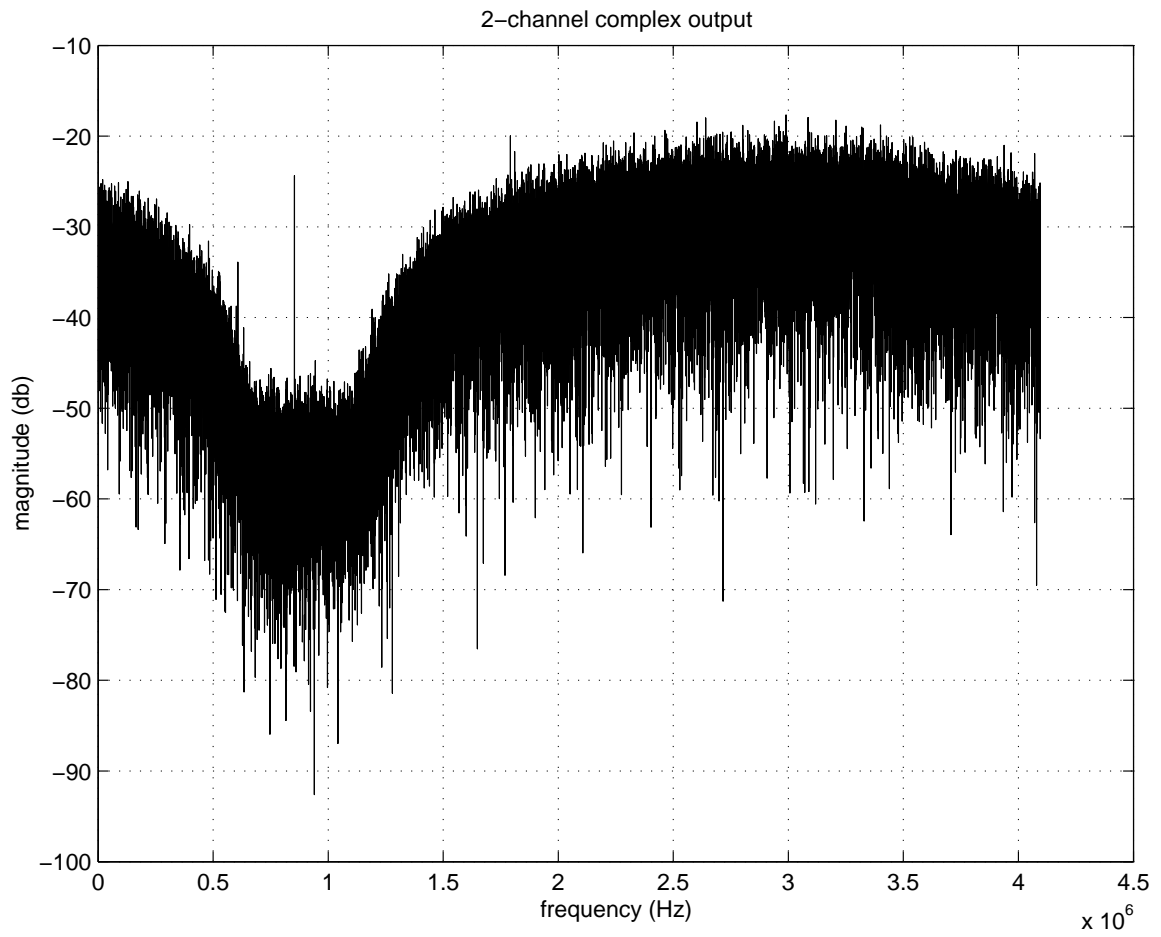


Figure 4.3: Modulated Signal Test Data

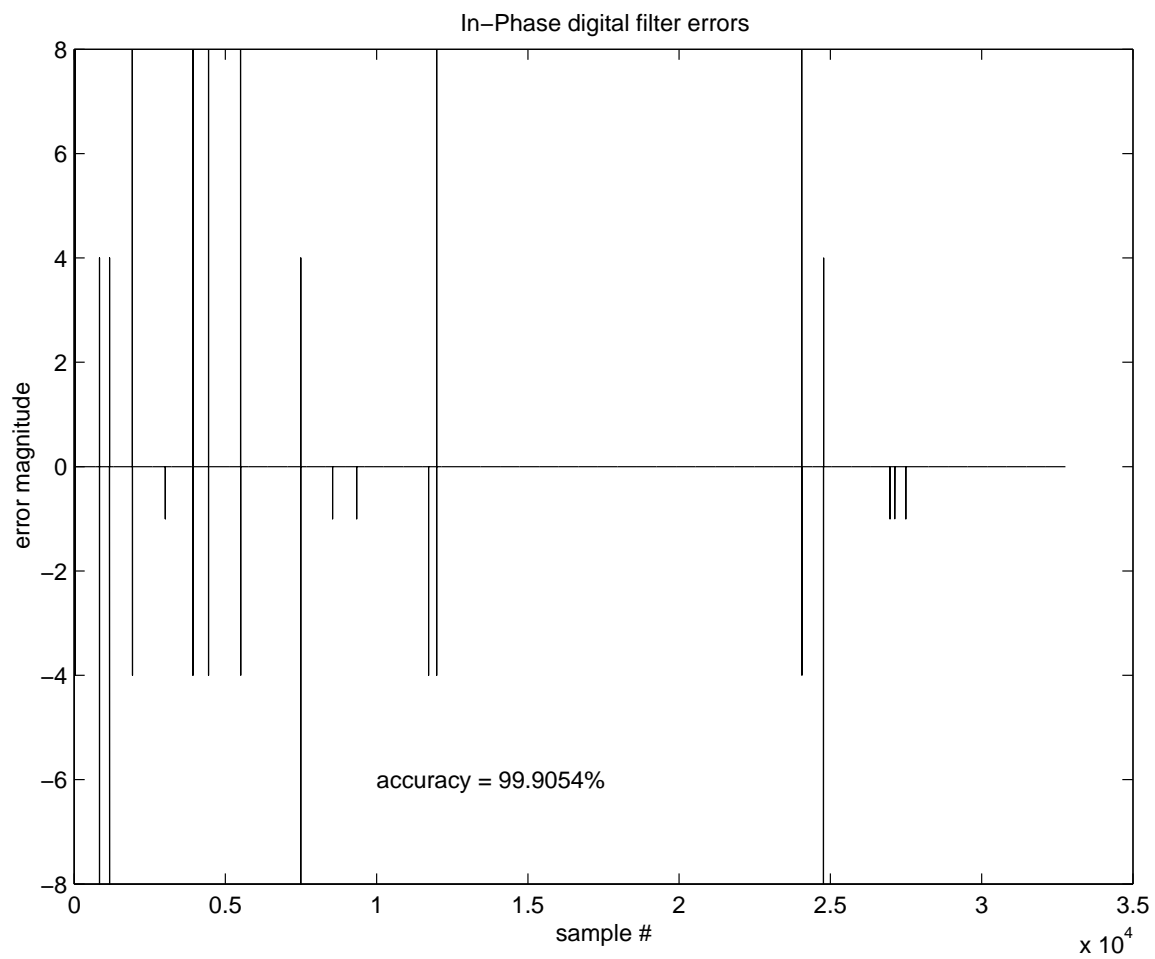


Figure 4.4: Digital Filter errors in modulated test (In-Phase)

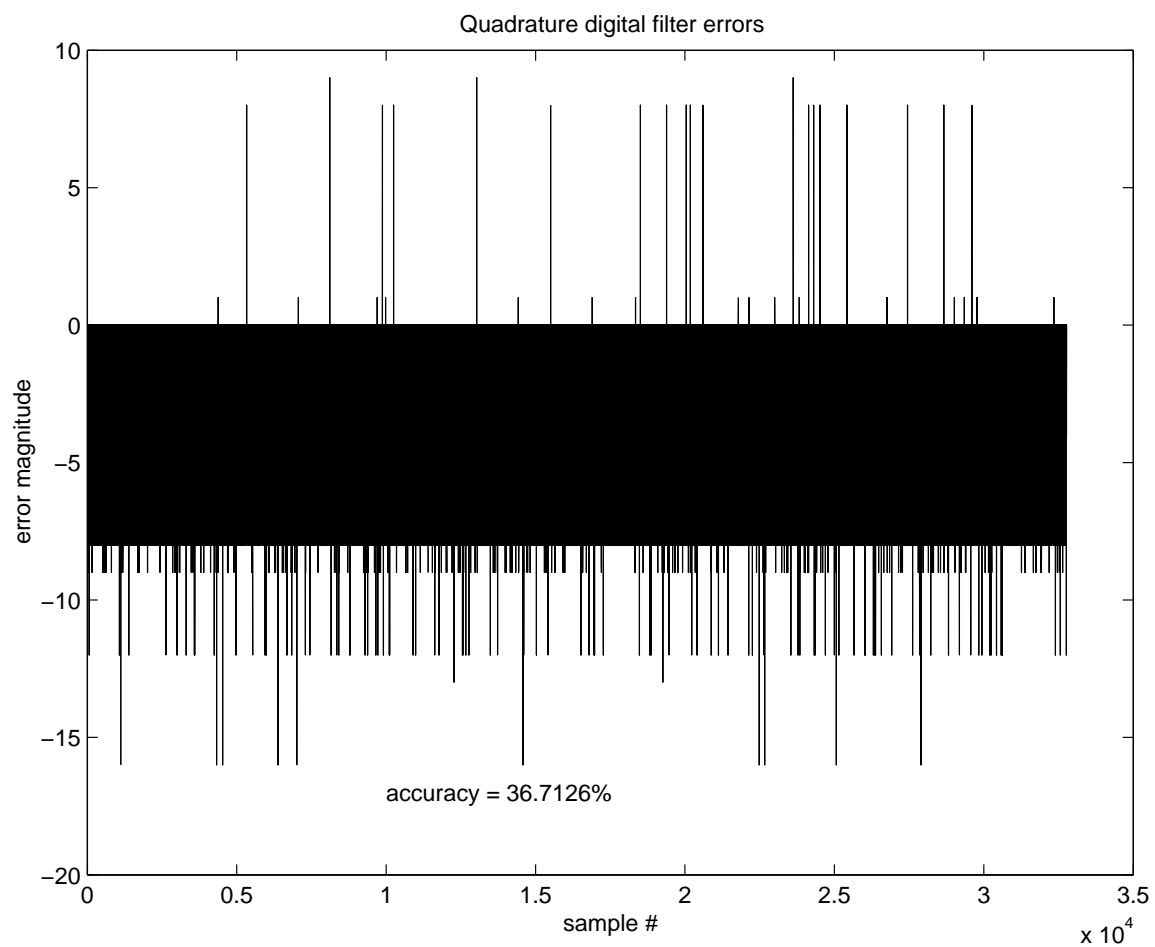


Figure 4.5: Digital Filter errors in modulated test (Quadrature)

Results:

The results of the complex modulation and A/D conversion test are shown in Figure 4.3. The noise shaping of the Sigma-Delta A/D converter has been modulated to provide the best resolution near the test frequency, which appears on the correct bin. Figures 4.4 and 4.5 show the accuracy of the digital filters in both the In-Phase and Quadrature channels. The In-Phase side again had few errors (31 out of 32768 samples) while the quadrature side had errors on roughly 2/3 of the samples.

Conclusion:

The test signal has been modulated correctly and sent through the Sigma-Delta A/D Converter as a baseband signal, which proves that the converter can be used to convert signals at frequencies higher than f_s/OSR . The resolution of the converter is consistent with what was seen previously in the baseband test. In looking at the plots of the digital filter errors for the two channels, it would appear that timing is again an issue. However, the large number of errors in the Quadrature side would appear to indicate that the filter itself is somehow flawed. The filters in both the Quadrature and In-Phase channels are copies of each other, so there may be a bad connection or a bad gate somewhere.

4.2.5 Evaluation of Nmos transistors

Purpose:

Three nmos transistors of channel widths $3\mu m$ and lengths of 0.6, 1.8, and $3.0\mu m$ were fabricated and probe pads for each terminal were brought to the surface. This test evaluates the threshold voltage and channel length modulation coefficient.

Theory:

The threshold voltage is best obtained from a $I_{DS} - V_{GS}$ characteristic by extrapolation of the steepest slope to $I_{DS} = 0$.

The channel length modulation coefficient is obtained by extrapolating the active portion of the $I_{DS} - V_{DS}$ characteristic to $I_{DS} = 0$. This is done for a range of V_{GS} levels.

Equipment:

1. T1CK-AM (#5)
2. Summit probe station (model 11741-6).
3. Two Keithly source measurement units (model 236)

Procedure:

For each of the three nmos transistors obtain:

1. $I_{DS} - V_{GS}$ characteristic
 - a. Set $V_{BS} = 0V$.
 - b. Set $V_{DS} = 0.1V$.
 - c. Linearly step V_{GS} from 0 to 5.0V (total of 50 steps).
2. $I_{DS} - V_{DS}$ characteristic
 - a. Set $V_{BS} = 0V$.
 - b. Obtain five sets of data with $V_{GS} = 1, 1.5, 2, 3, 4, \text{ and } 5V$.
 - c. Linearly step V_{DS} from 0 to 5.0V (total of 50 steps).

Results:

Figures 4.6 to 4.8 show the $I_{DS} - V_{GS}$ characteristics of the NMOS transistor of three different channel lengths. The threshold voltages (V_t) based on the three curves vary from 0.86 to 0.9 V. These are slightly higher than the 0.8V given for the parameter by MOSIS. This difference may be related to a difference in methodology for obtaining the parameter.

The voltage measured here are more precisely referred to as V_{on} . It typically is 2 to 4 times kT/q higher than the V_t (at $\Psi_s(inv) = 2\Psi_B$) used in determining subthreshold currents. Considering this bias in our measurements, agreement is excellent.

The first three figures also show the effects on the lateral electric field on the carrier mobility within the channel. The drain current falls off with increasing gate voltage because carriers are confined more closely to the channel-oxide interface and the electron surface mobility falls.

Figures 4.9 to 4.11 show the $I_{DS} - V_{DS}$ characteristics for a series of V_{GS} . The curves are very flat in the active region indicating little channel length modulation for all channel lengths. The characteristics for the 3.0μ channel device show nearly a quadratic dependance of current on the overdrive voltage

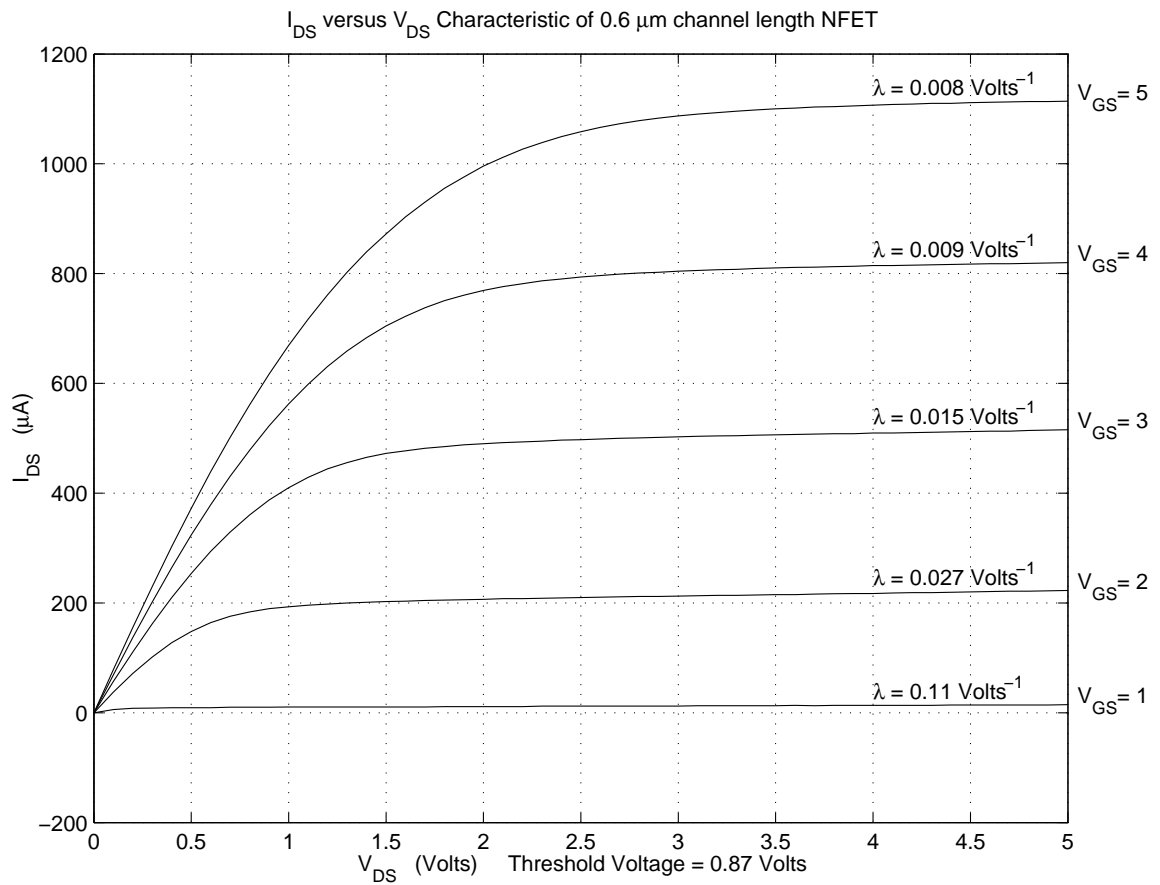


Figure 4.6: NMOS $W/L = 3/0.6$.

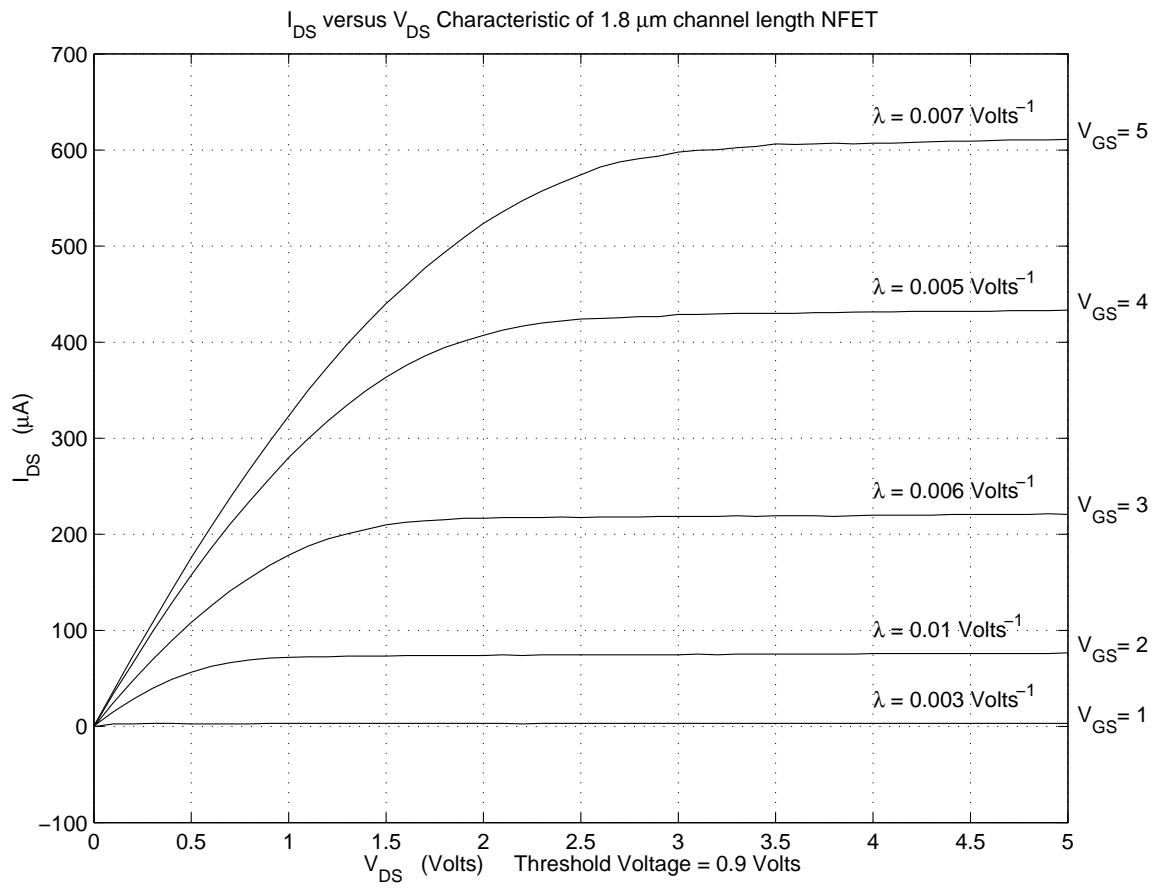


Figure 4.7: NMOS $W/L = 3/1.8$.

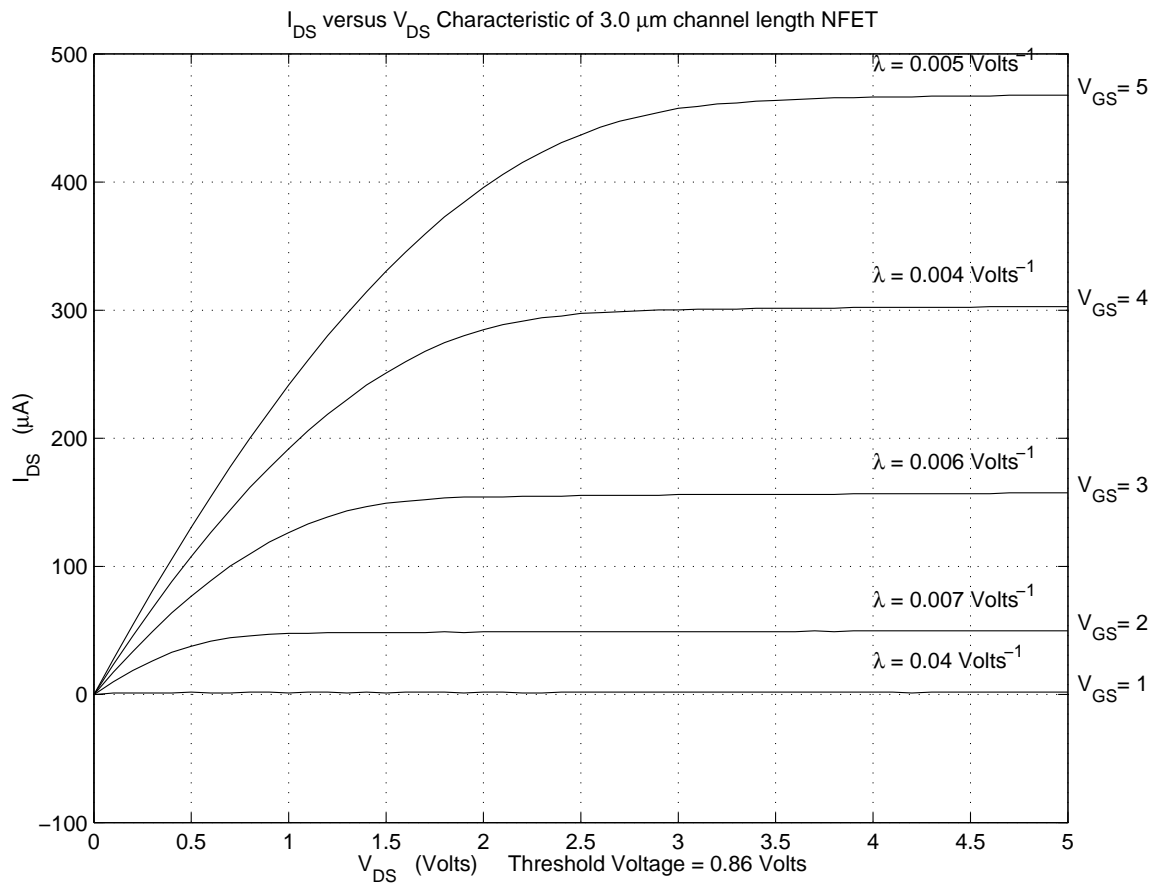


Figure 4.8: NMOS $W/L = 3/3$.

$(V_{GS} - V_t)$. The $0.6\mu m$ device shows a near linear dependence indicating the effects of velocity saturation due to the high field along the length of the channel.

Conclusion:

1. Threshold voltages agree well with the process specifications utilize in the design.
2. Channel length modulation is small for devices of all sizes.
3. Velocity saturation is present in the minimal channel length device.

4.3 Additional Test Proposals

The following additional tests on the fabricated device are proposed.

1. Test other chips for functionality.
2. Test the linearity of the metal - metal capacitors and compare to the poly - poly capacitors on the sample capacitors in the corner of the silicon.
3. Test the signal at the intermediate integration stages for accuracy and clipping.
4. Test the on chip voltages for stability.

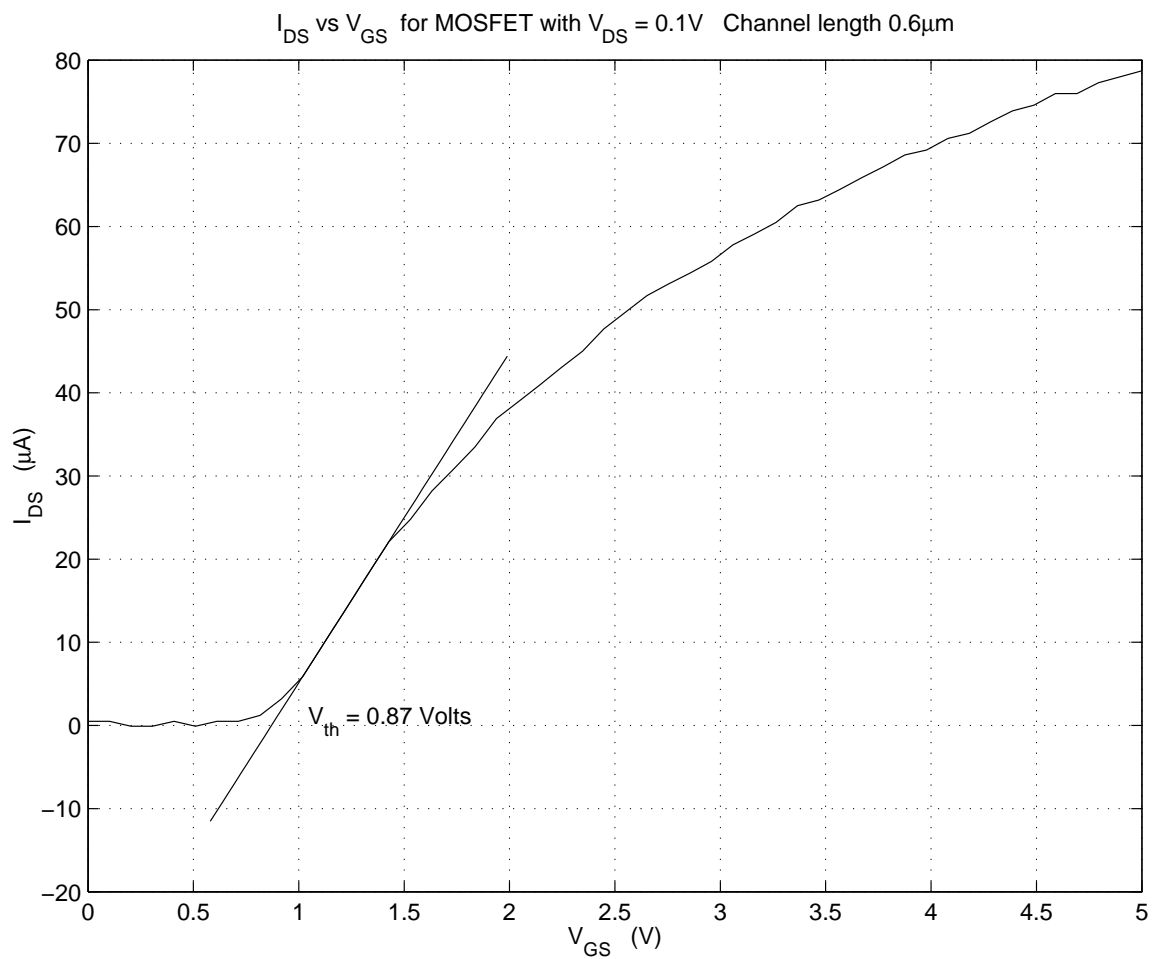


Figure 4.9: NMOS $W/L = 3/0.6$.

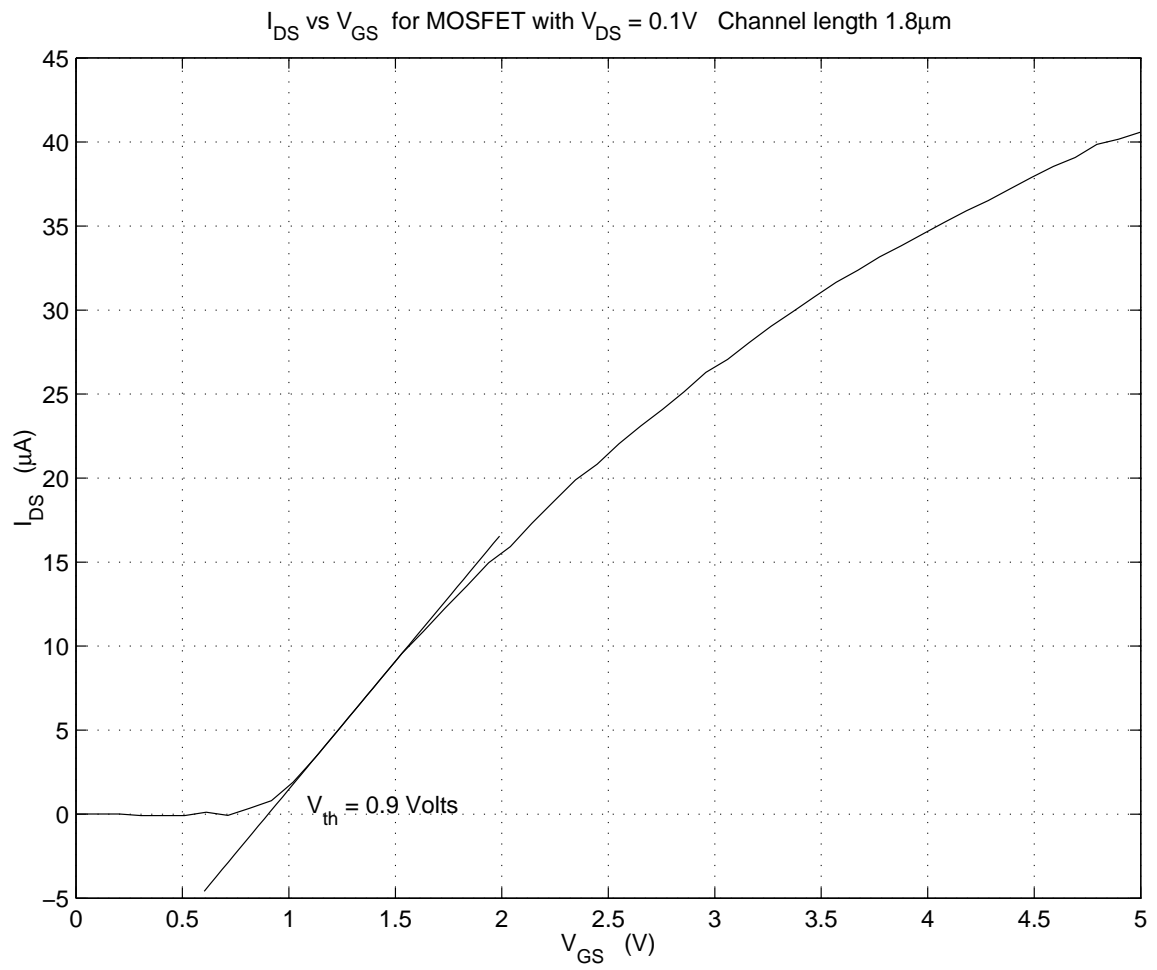


Figure 4.10: NMOS $W/L = 3/1.8$.

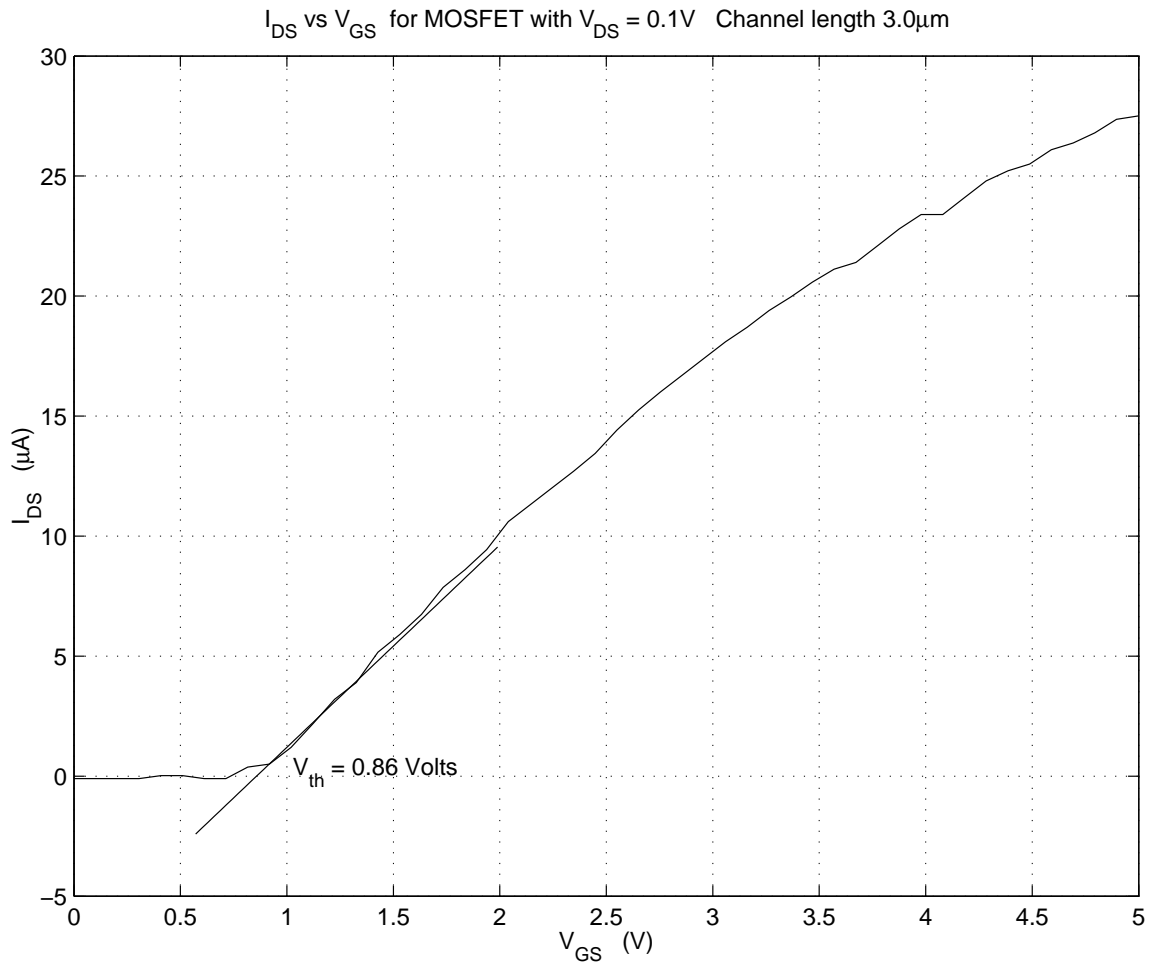


Figure 4.11: NMOS $W/L = 3/3$.

5 Summary

5.1 Comparison of simulation and experimental results

Lengthy simulation times and small data sets limited the amount of tests that were run on the fully assembled circuit. Functionality of the top level schematic has been verified, although reliable performance measures remain unknown. Definitive tests to determine the performance of the chip will be performed on the actual chips when they are returned.

5.2 Potential improvements

There are a variety of areas where improvements could be made to this design. Some of these areas arose from our loosely defined design methodology, while others were inherent in the physical process.

This section discusses the faults in our design methodology and resultant limitations in performance. Suggestions for improvement in the design are also discussed.

5.2.1 Design methodology

It would have been advantageous to carefully specify the performance required of each subcomponent earlier in the process. As we were designing subcomponents we had a good idea of the output that a component was required to produce and the signal input it should receive, but little idea of the resources a component would require to perform its function. The important resources we initially ignored were component power consumption and space requirements.

A certain amount of iterating between schematic design and layout is important during the design process. Our design process did this at the low level of the basic components, but we were unable to go back and forth between circuit design and layout at the top level. Clearly redesigning high in the hierarchy is an expensive proposition, but given our inexperience and our space constraints some iterations at the top level are essential. It would have

been beneficial to be able to redesign parts of the chip since this would relax some space constraints on the analog side of the circuit and we would not have been forced into some compromises we made. In retrospect we have adequate space, unfortunately it is not efficiently utilized in our design.

As well as a careful specification of the performance of each subcomponent in terms of electrical parameter it is important to translate these specifications into space and layout requirements. Insufficient definition of the required power line dimensions for each component lead to in-discriminant addition of contacts and metal lines to V_{dd} , gnd , and substrate. Sometimes we wanted to increase power line widths, but were unable. A careful definition of requirements of each component would have lead to a more effective and efficient layout.

5.3 Suggestions for improvements

We were unable to fully simulate our circuit for sufficient time to have a clear idea of how well it will perform in terms of effective bits of resolution. Because of this, areas where our design is lacking are not obvious. Speed is a clear area to improve. A few potential areas that may reduce the precision of the converter can be identified. These include overall layout, transmission gate design and modulator capacitors.

5.3.1 Operating frequency

We aimed for a $20MHz$ sampling rate, but intend to run the circuit only at $5MHz$. The primary deterrent to faster operation is the OTA. We may be able to squeeze 8 to $10MHz$ from the design, but a higher peak current from the OTA may be required in order to reach $20MHz$. An improved OTA design is needed for faster operation. The next component that would limit speed of operation is the comparator, but this limitation would not become significant unless the clock frequency exceeds $20MHz$.

5.3.2 Overall physical layout

The overall layout caused congestion on the analog side of the circuit that may result in loss of precision. The circuit layout is primarily dictated by the physical design of the modulator. The modulator is the largest component,

but was also the first component designed. A successful attempt was made to minimize the size of components in the modulator. Unfortunately, the space saved by the modulator design was not located in a position that was beneficial for the rest of the circuit.

The logic components for the modulator are in the shape of rectangles. If these could be redesigned with the shape effectively rotated 90 degrees, the free space could be move to the analog side of the circuit. This would have eliminated the need for a some compromises that we were forced to make on the analog side.

The congestion of the analog side lead to Metal 3 lines over integrating capacitors and sharing of N-wells between capacitors and PMOS. If space had been freed up then capacitors could have been shielded and placed in isolated N-wells to reduce substrate noise.

5.3.3 Transmission gates

Transmission gates were of two types, isolated NMOS, and PMOS/NMOS gates with inverters. Simulation of the NMOS gates suggests that the differential configuration of the design should lead to minimal net charge injection at the modulator sampling capacitors. Unfortunately the charge injection form the PMOS/NMOS gates is significantly modulated by their input voltage. Thus the differential configuration will not fully remove this source of error.

Simulation experiments of transmission gate charge injection included an NMOS with a dummy gate. This type of gate modulated charge injection less than the PMOS/NMOS gate, but the dynamic range is also less. We would like to further investigate transmission gate designs. The use of dummy gates on both sides of an NMOS/PMOS design might produce a superior transmission gate. We would like to simulate such a design and fabricate a variety of gates so they could be compared experimentally.

5.3.4 Modulator capacitors

The modulator capacitors place a limitation on precision, but fortunately in a predictable fashion. Theoretically, any effects due to mismatch in these capacitor sizes could be corrected in processing the outputs. Regardless, it would be preferable to have the required precision in the hardware. The necessary precision could only be added by increasing capacitor area. This

would require an obvious increase in chip area as well as a higher current capacity in the OTAs.

5.3.5 Coping with parasitics

We paid insufficient attention to parasitics early in the design. A valuable lesson learned is the rapid increase in capacitance as metal lines lengthen.

The capacitive load of the gate control lines of our modulator capacitors is up to $150fF$. We discovered this too late to be able to optimally fix this problem. The option of reducing line length is probably not viable since it places digital components adjacent to the analog components. The best solution is to drive the lines with a larger inverter. Unfortunately, changing inverter size was not an option at the time the problem was discovered, the line drivers were surrounded by other components. Any change in inverter size would lead to near total revision of the modulator layout. Although this would be a good idea for a number of reasons, it was not a viable alternative at the time of discovery.

The solution employed was to increase the non-overlap period on the clock so that the slow turn-on/off time produced by this capacitive load was not an issue. This was possible because there was plenty of free space around the clock.

There are two undesirable effects of the solution implemented. First, the solution imposes a limitation on the top operating frequency. The non-overlap period is about $6ns$. This would waste a significant part of the clock cycle if the design were able to operate near $20MHz$. Secondly, and possibly more important, the slow rise times of the gate control lines may have an adverse effect on charge injection from the gates.

A significant parasitic capacitance appeared on the clock lines. Our design utilizes a central clock. The combination of the large gate load for the clock and the even higher parasitic line capacitance was underestimated. Large clock buffers should be used to supply this large load. An even better design would be to distribute the clock buffering capacity. Since the NMOS/PMOS transmission gates used have an inverter incorporated, the NMOS and PMOS are seeing signals with significantly different rise time. The impact on charge injection is not known at this time.

The above discussion indicated that there is significant uncertainty with respect to transmission gate charge injection. Further simulation studies should be done to investigate this issue.

5.4 Project time commitment

The project was a valuable learning experience, but often moved too quickly to allow us to take full advantage of the opportunities. This is partly our own fault for so graciously accepting the project suggested by Professor Hummels. The project consumed us for the entire term. Collectively we spent 1200 to 1400 hours on this project.

Bibliography

- [1] Pervez M. Aziz, Henrik V. Sorenson and J. van der Spiegel, “An overview of sigma-delta converters,” *IEEE Signal Processing Magazine*, pp. 61–83, Jan. 1996.
- [2] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. DeMan, “Adaptive biasing cmos amplifiers,” *IEEE Journal of Solid State Circuits*, vol. 17, pp. 522–528, June 1982.
- [3] R. Castello and P. R. Gray, “A high performance micropower switched-capacitor filter,” *IEEE Journal of Solid State Circuits*, vol. 20, pp. 1122–1132, Dec. 1985.
- [4] R. Jacob Baker, Harry W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. Piscataway, New Jersey: IEEE Press, 1998.
- [5] A. Abo, *Design for reliability of low-voltage switched-capacitor circuits*. PhD thesis, University of California, Berkeley, 1999.

A Circuit Schematics

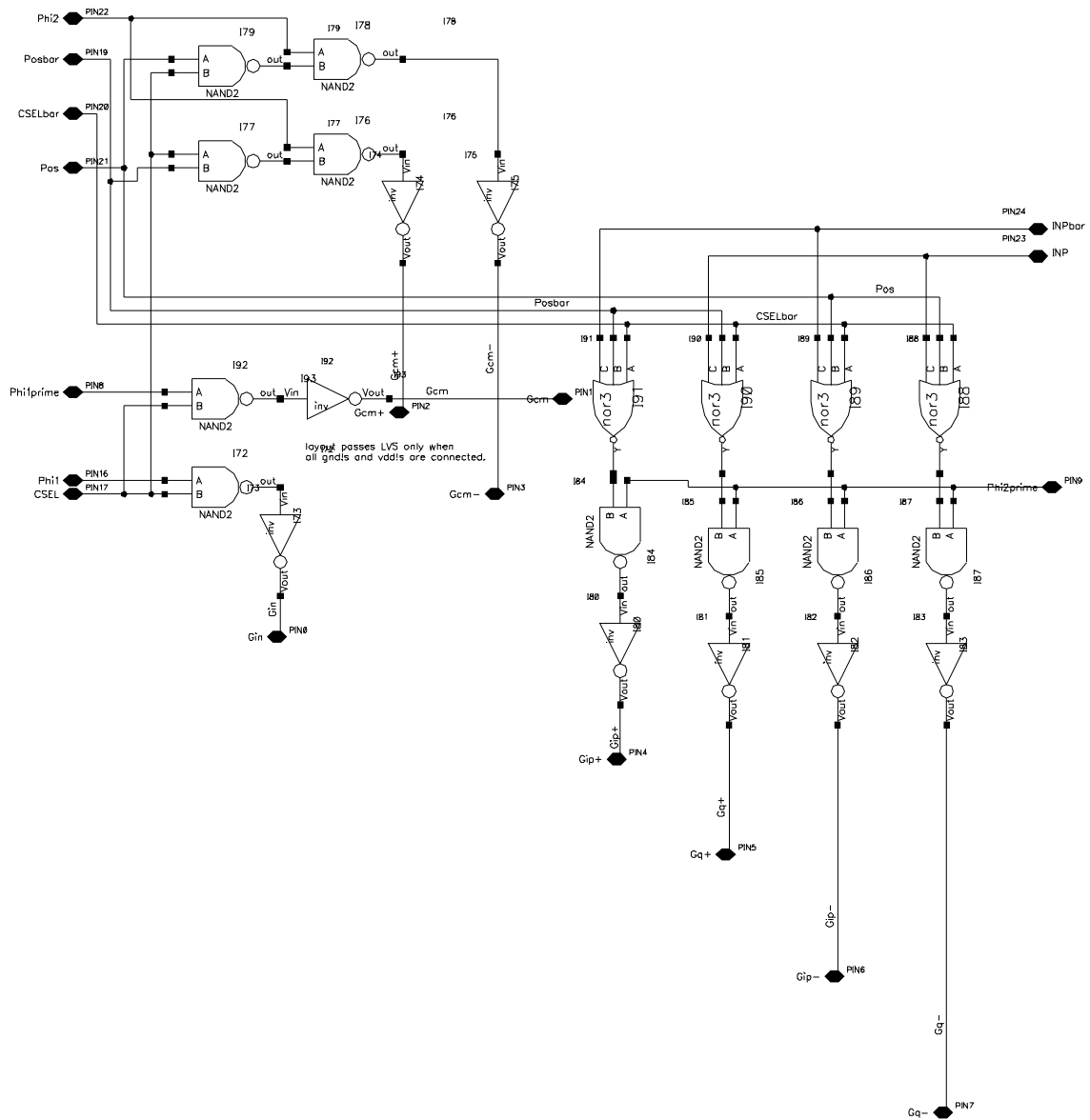


Figure A.1: Modulator capacitor gate control logic.

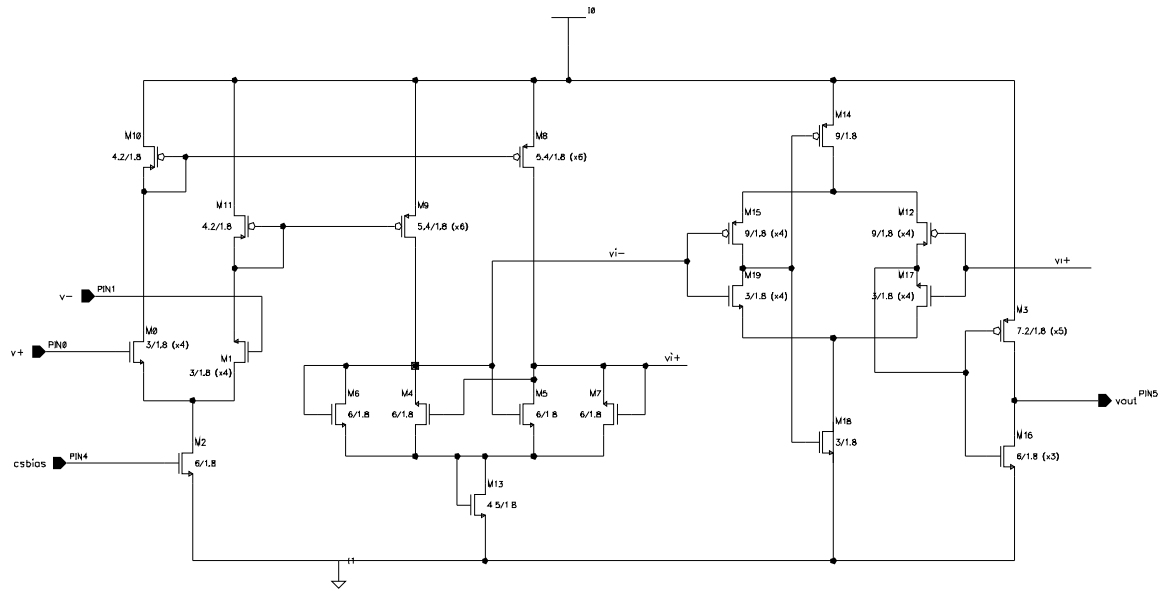


Figure A.2: Comparator and buffer schematic.

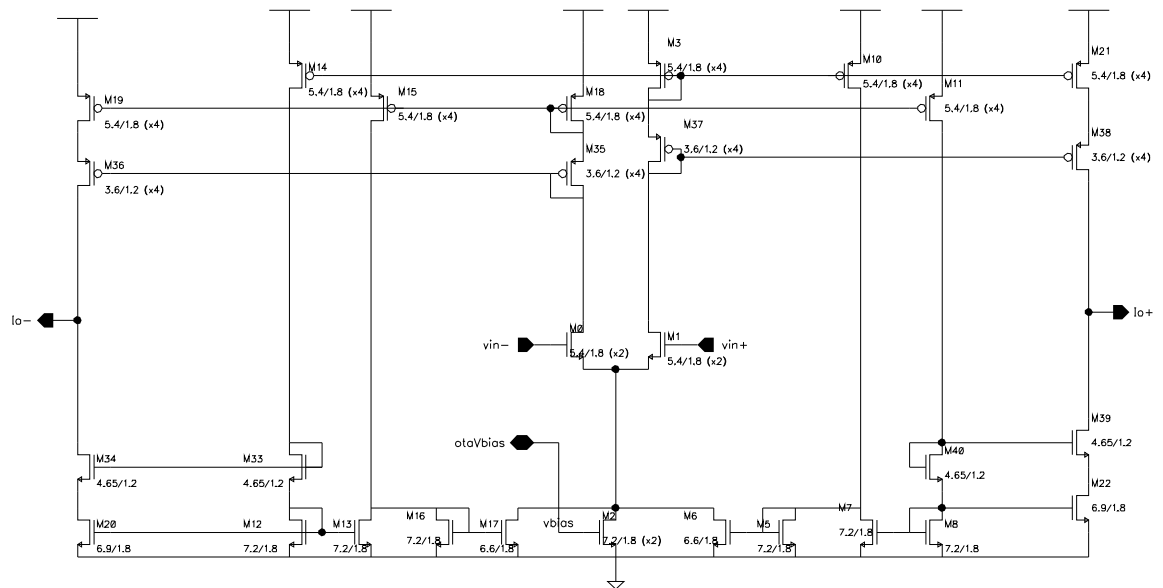


Figure A.3: OTA

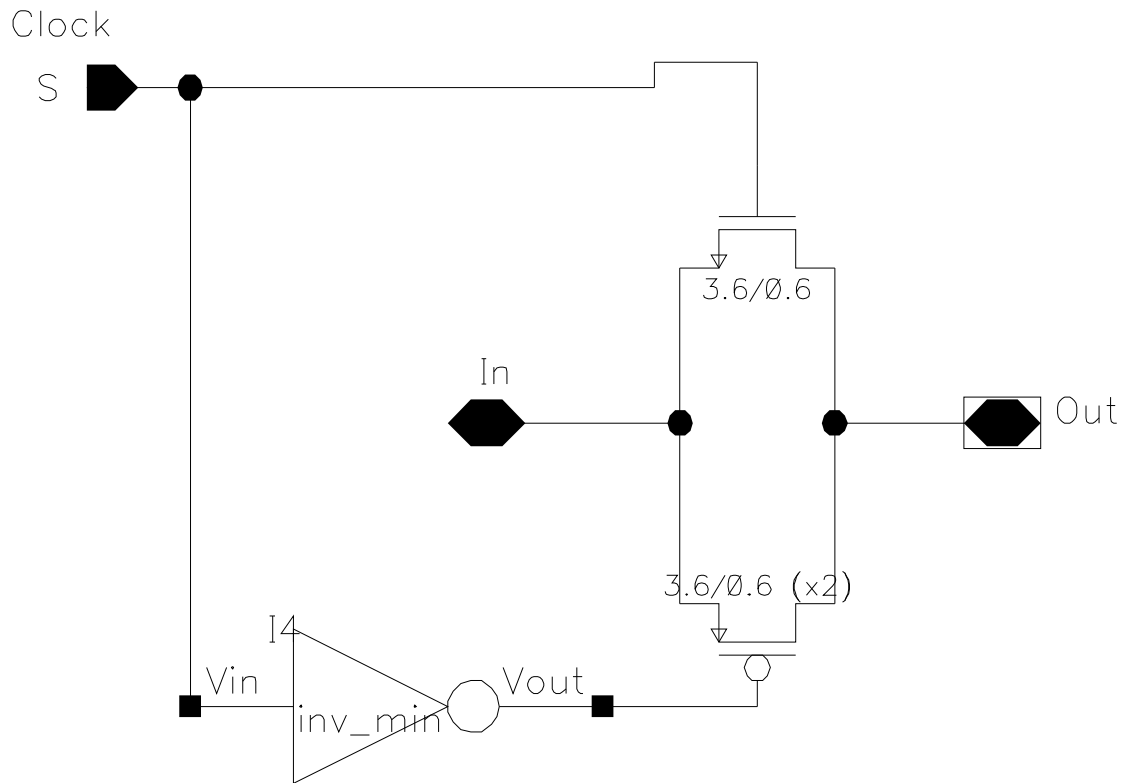


Figure A.4: Schematic of a NMOS/PMOS transmission gate. The other type of transmission gate used consisted of an NMOS transistor alone, of the same size as the NMOS above.

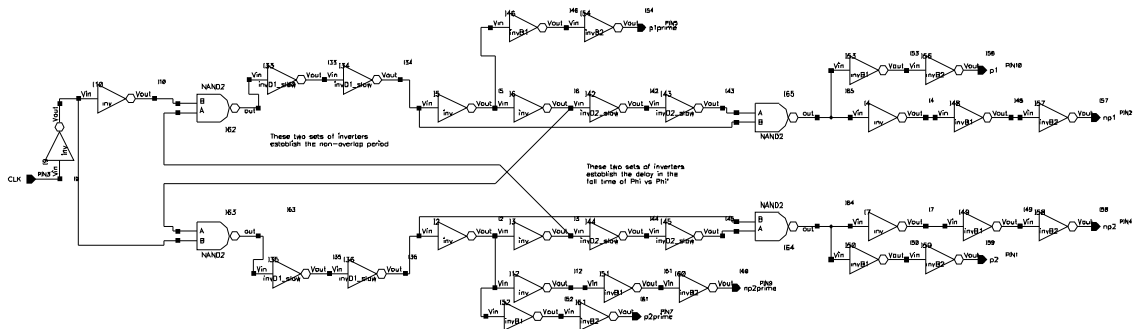


Figure A.5: The clock

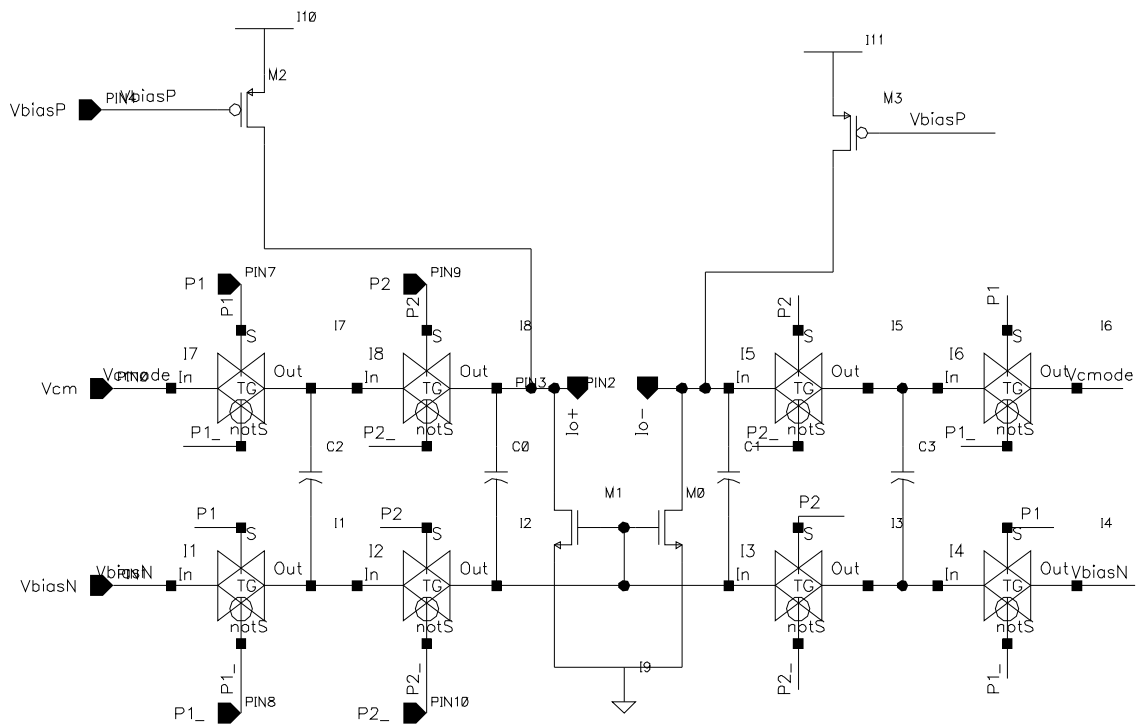


Figure A.6: CMF circuit.

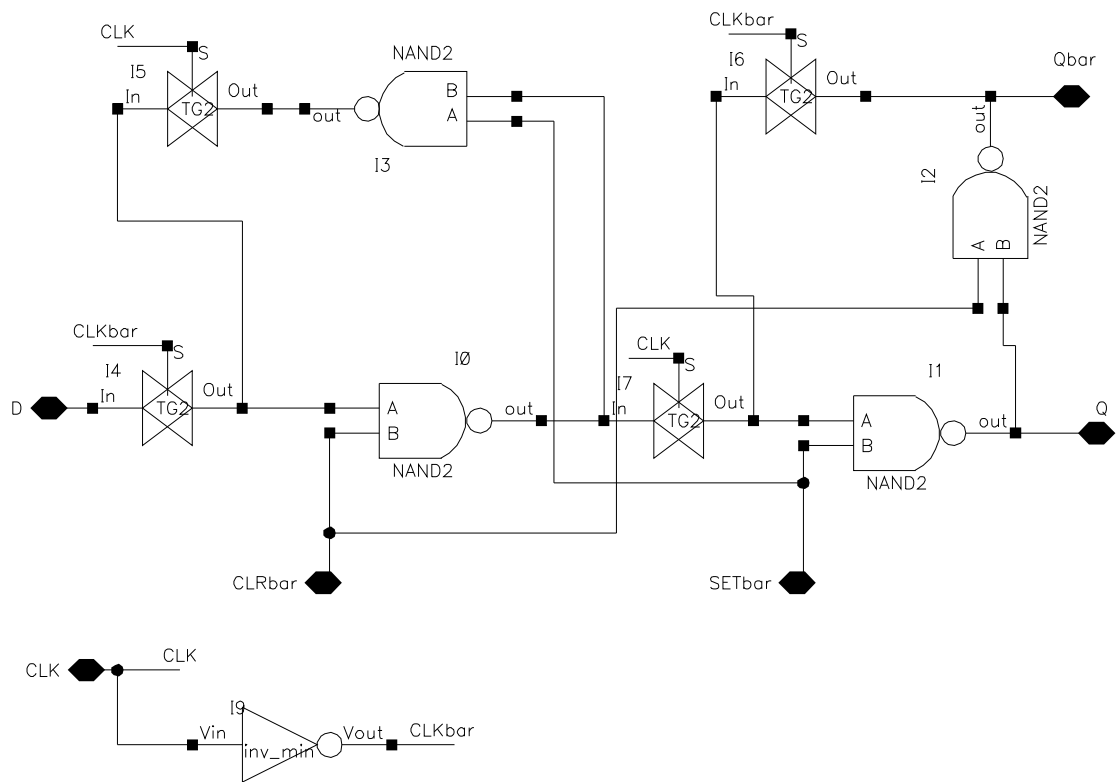


Figure A.7: Edge triggered flip-flop with clear and set.

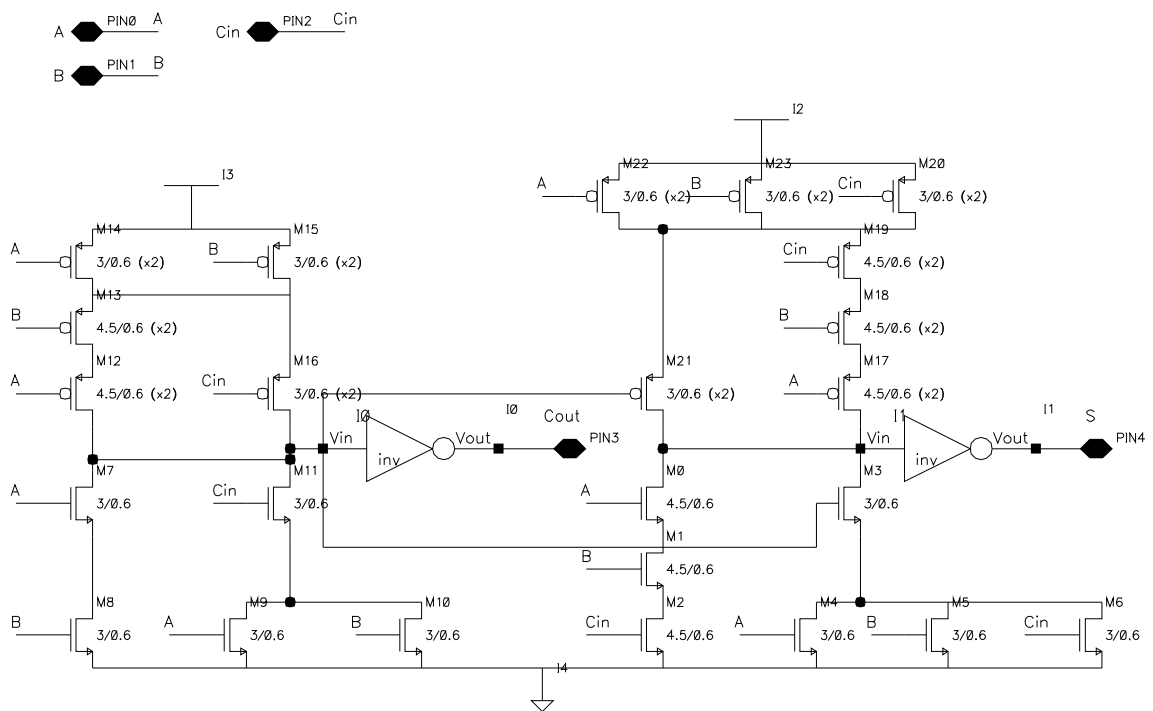


Figure A.8: Full adder with carry

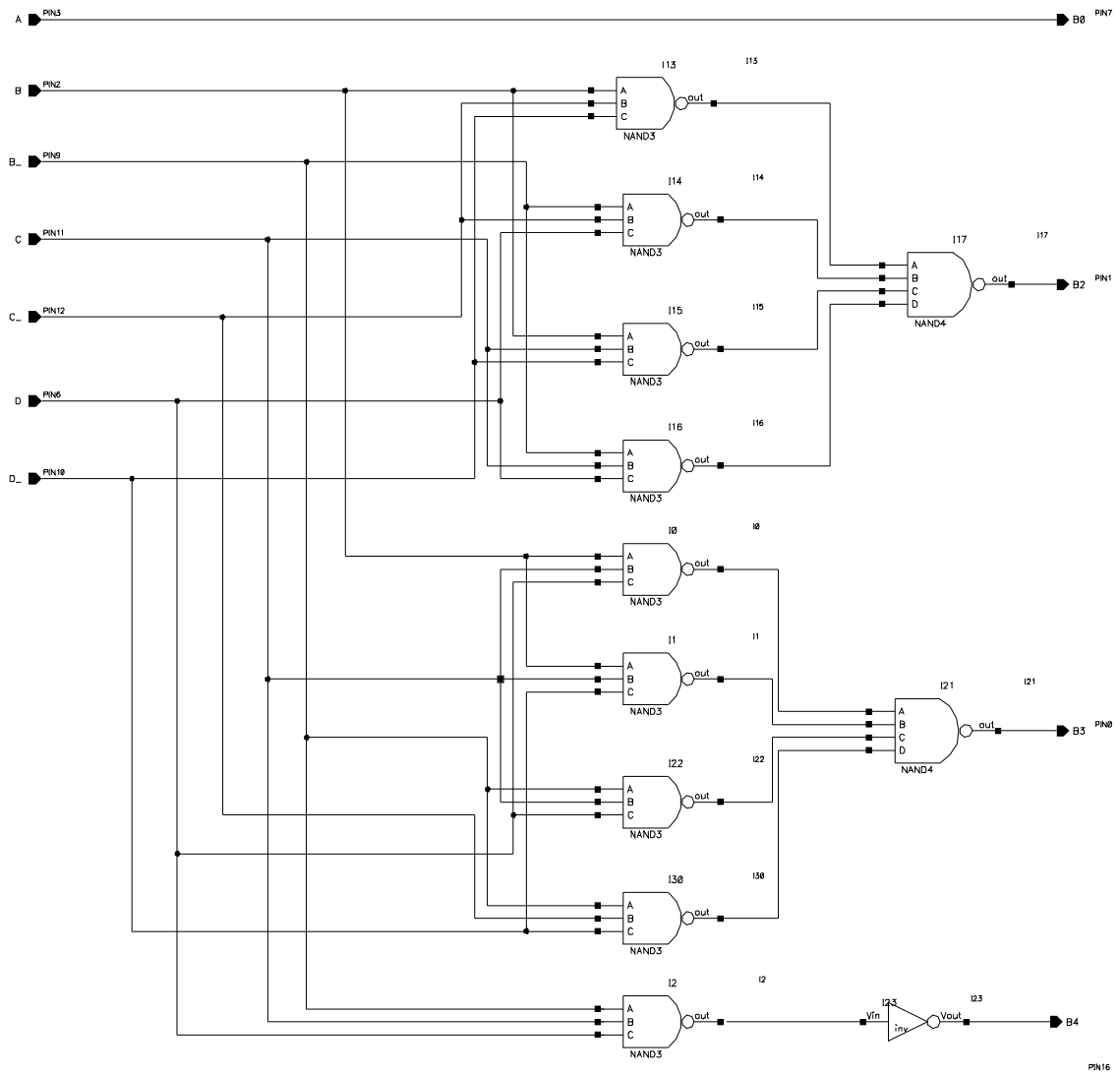


Figure A.9: Coding logic for output bits

B Circuit Physical Designs

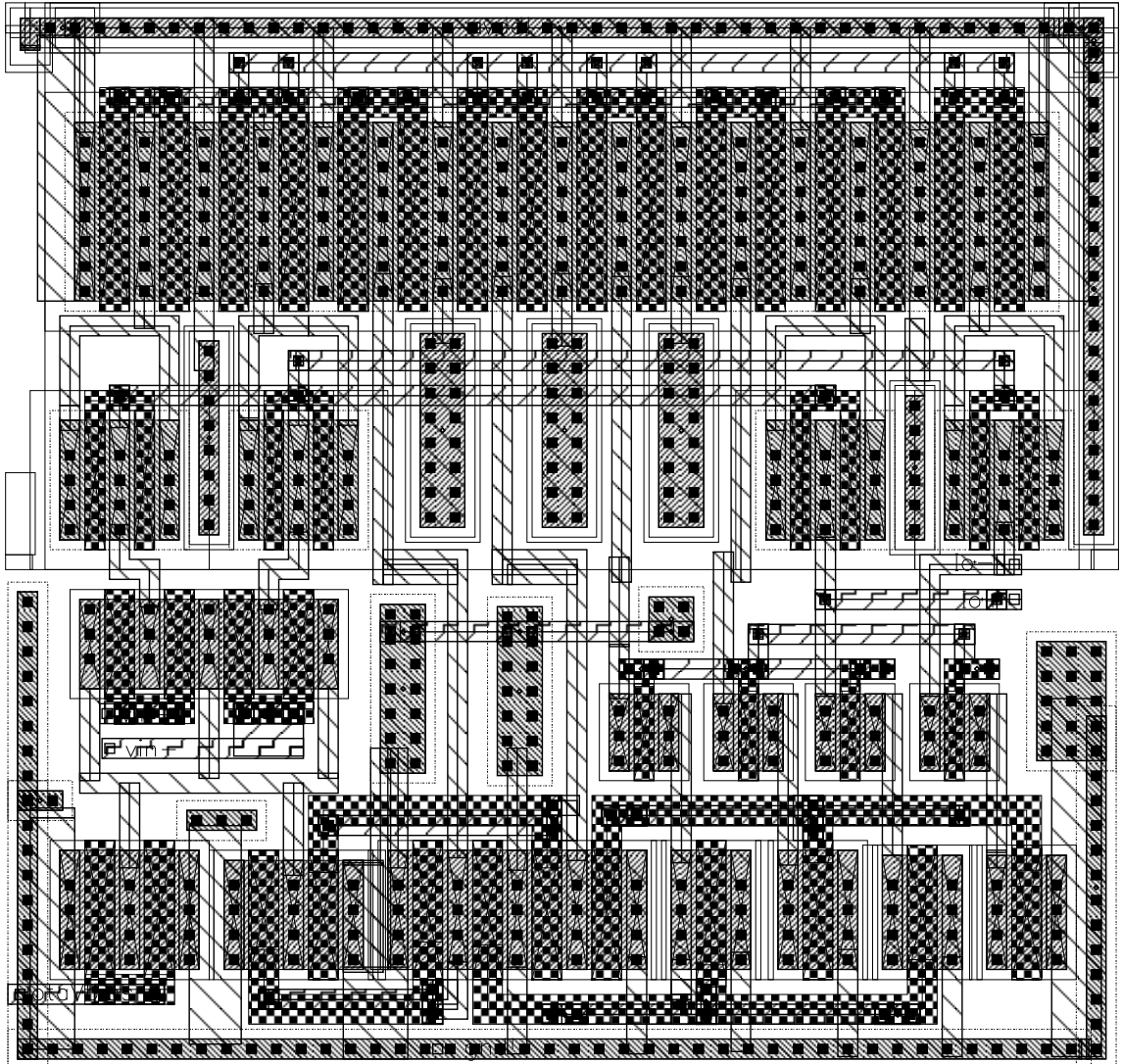


Figure B.1: OTA

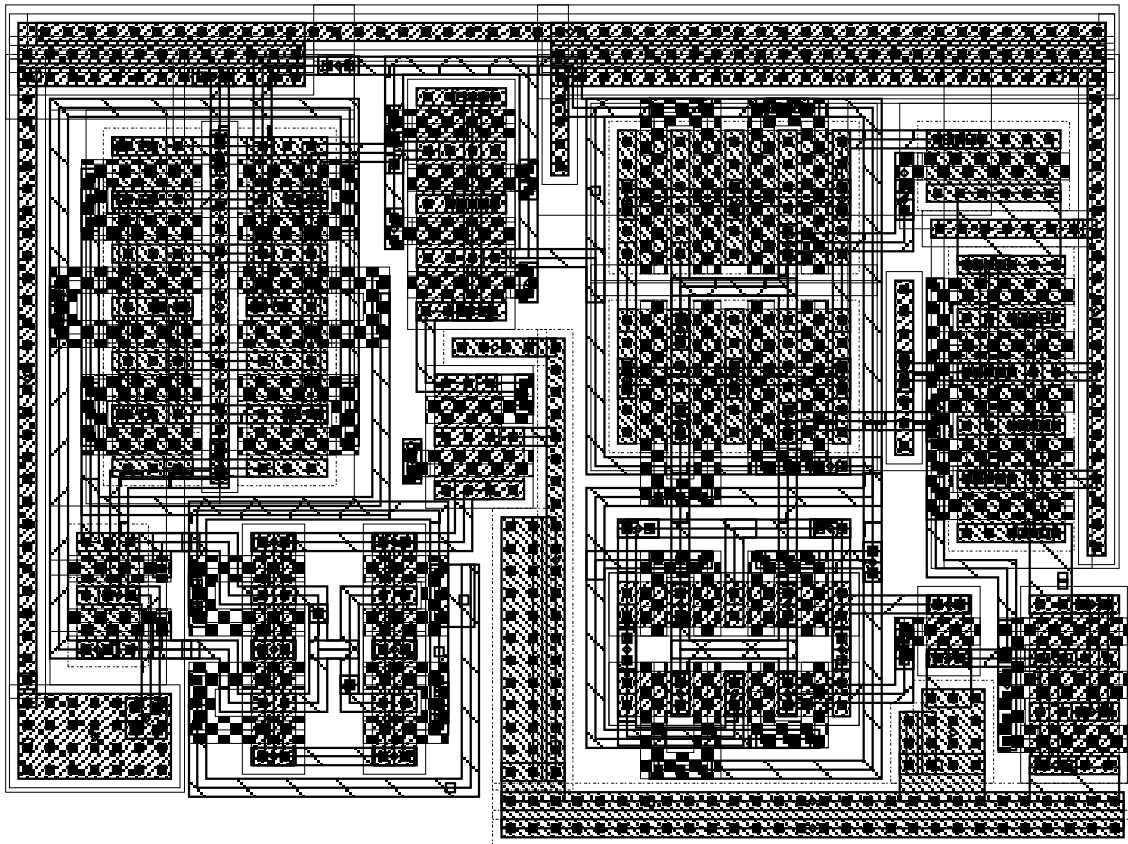


Figure B.2: Comparator

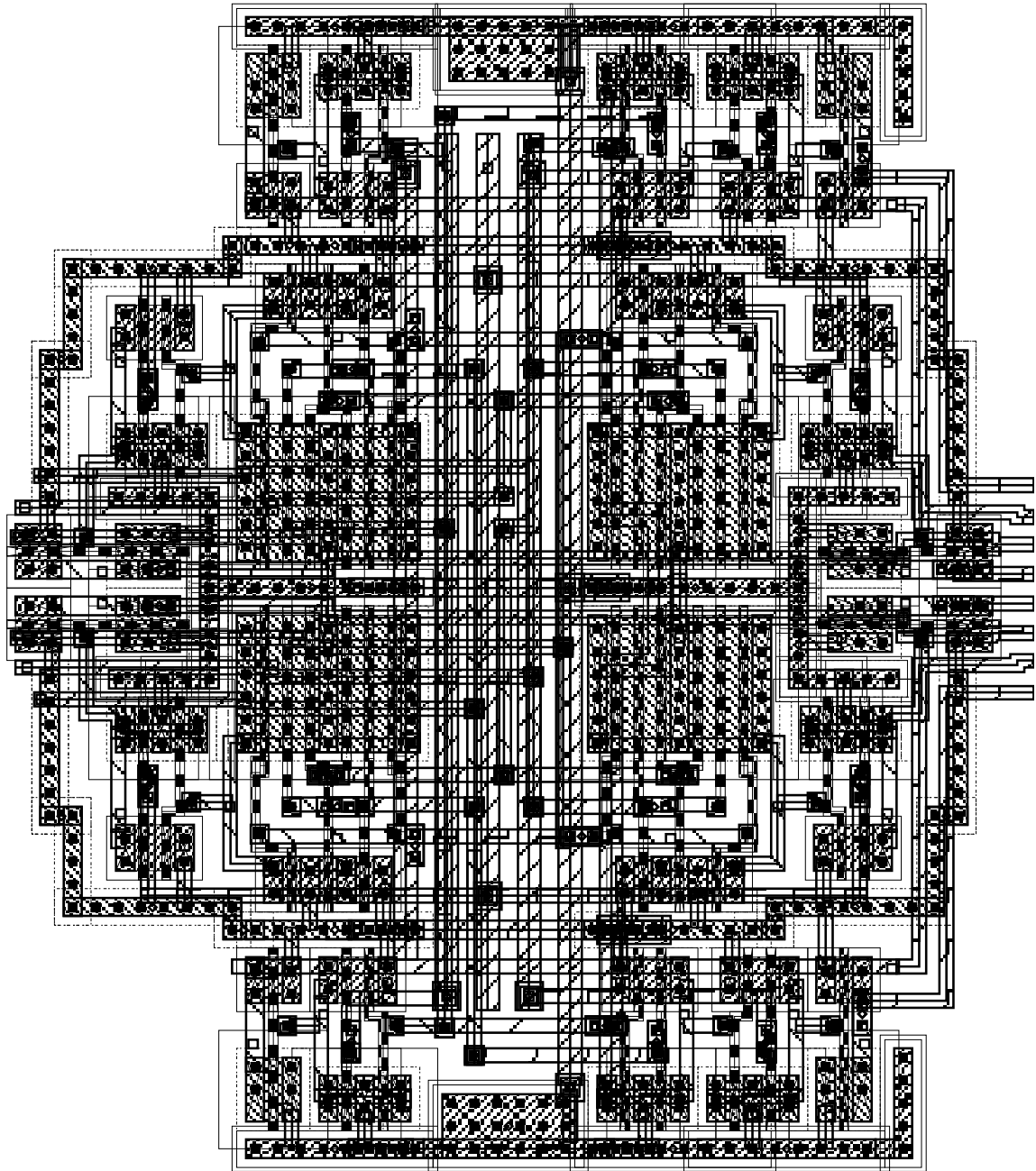


Figure B.3: Modulator capacitor gate control logic.

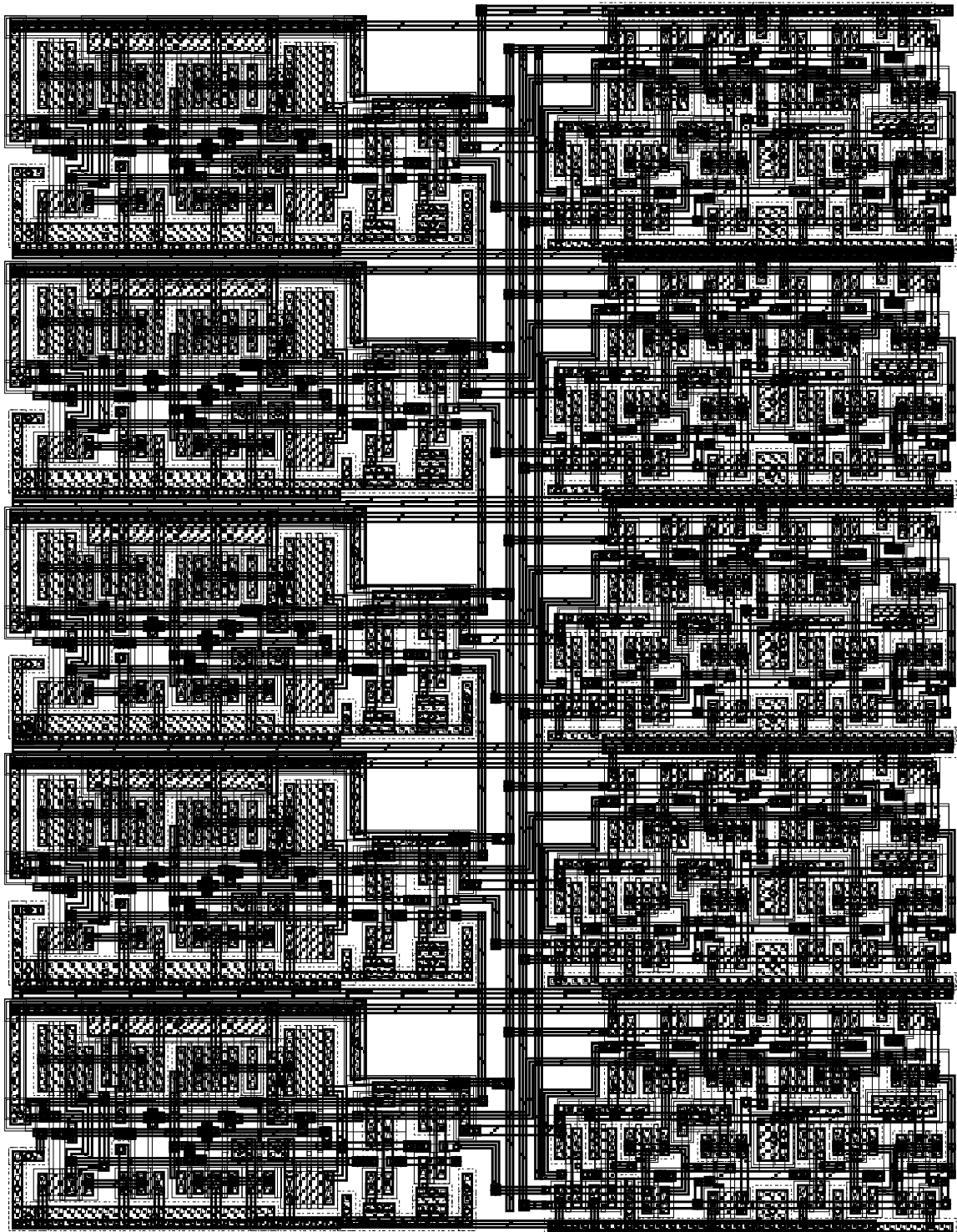


Figure B.4: Five bit modulo-32 counter

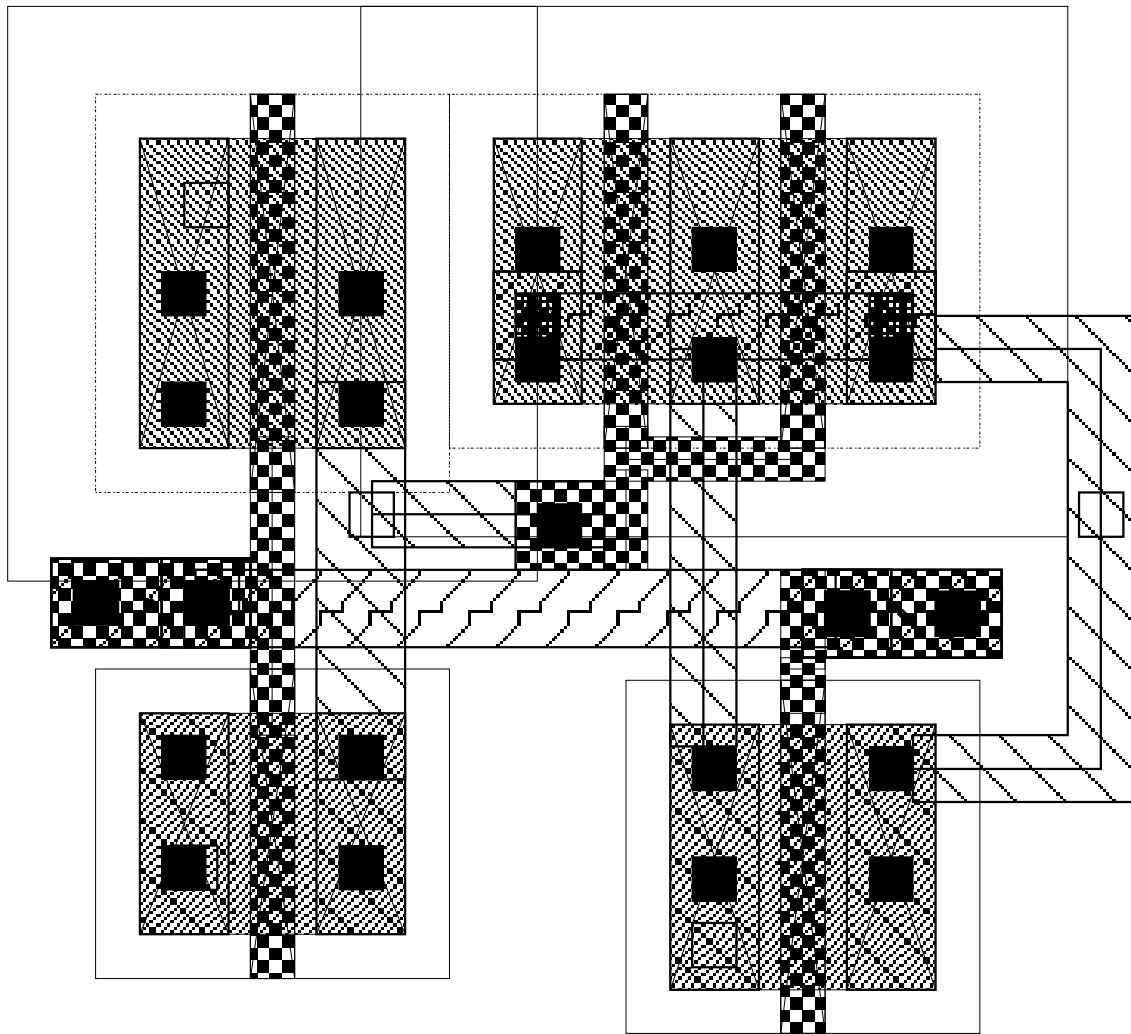


Figure B.5: NMOS/PMOS transmission Gate

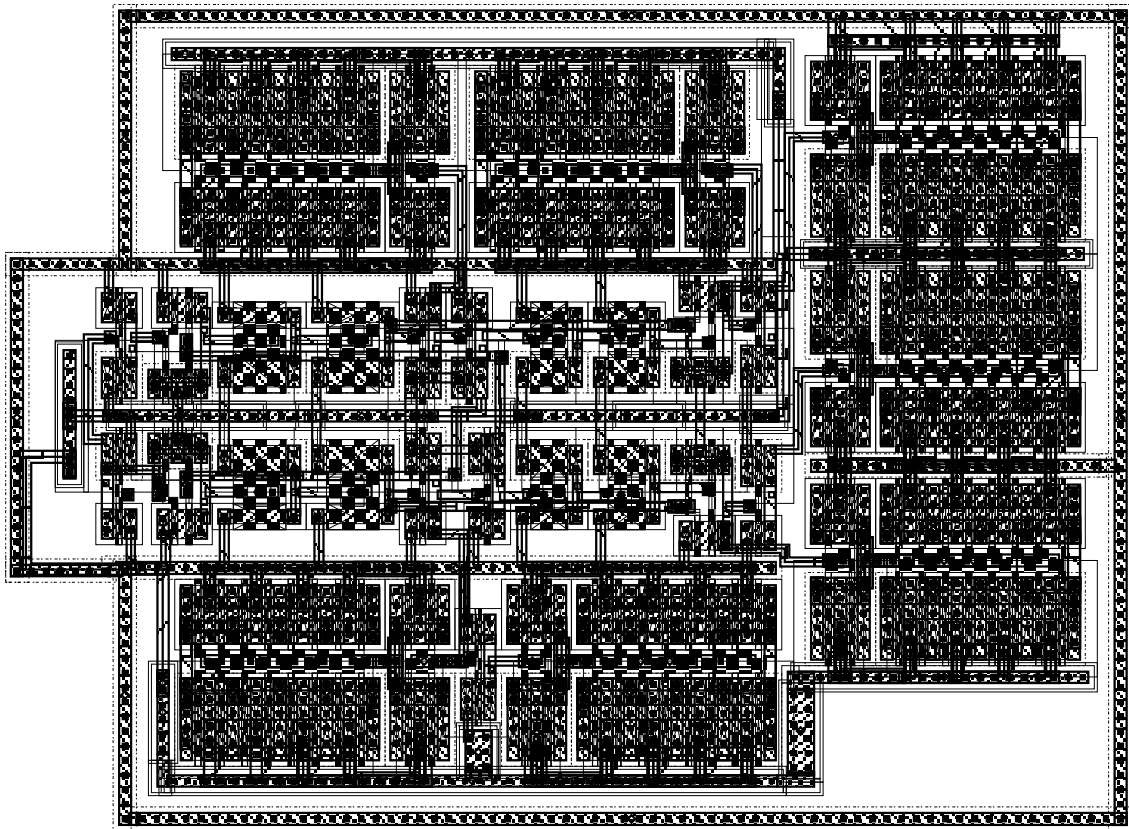


Figure B.6: The clock.

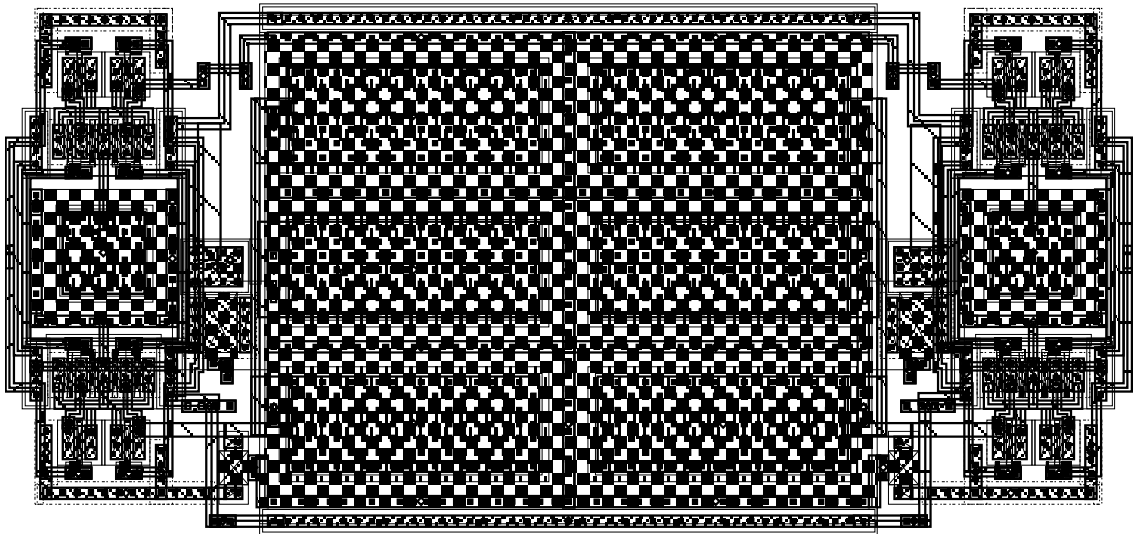


Figure B.7: CMFcircuit

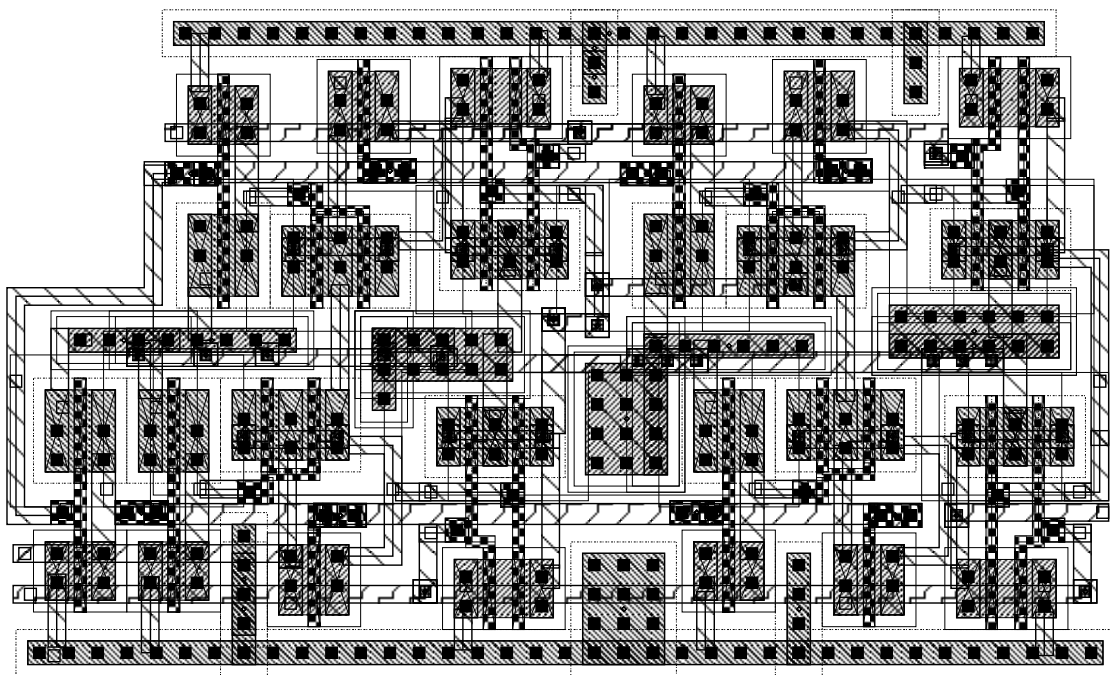


Figure B.8: Edge triggered flip-flop with clear and set.

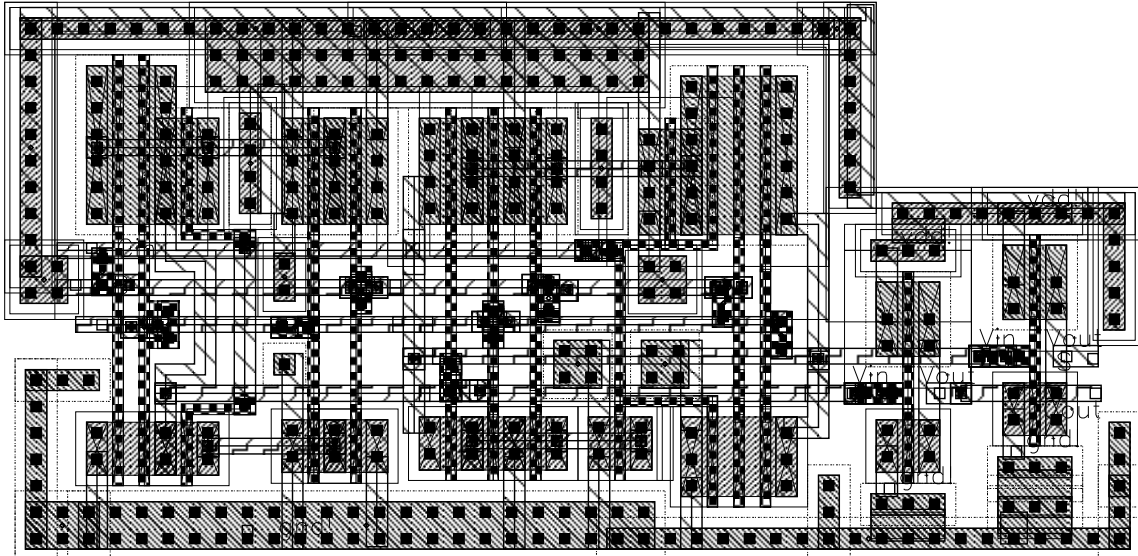


Figure B.9: Full adder with carry.

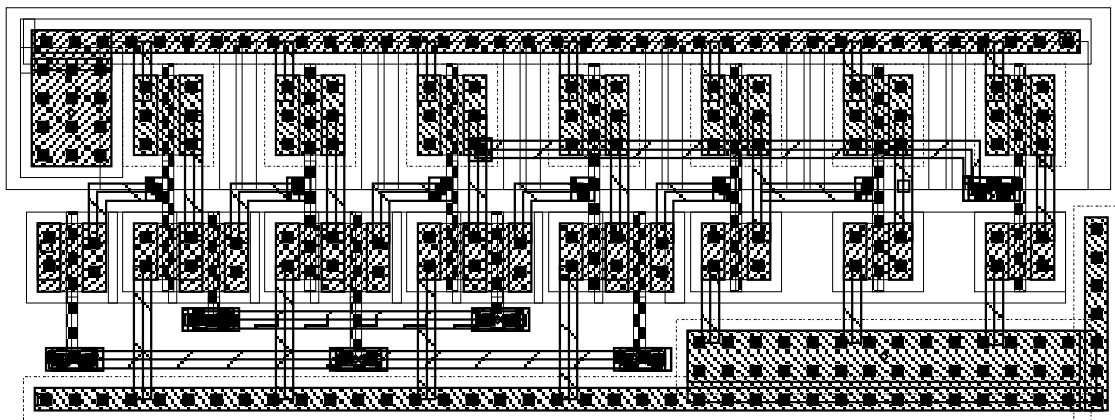


Figure B.10: Shift register.

C Selected Process Parameters

Parameter	Value	Units
$k'_n(\mu_n C_{ox}/2)$	58	$\mu A/V^2$
$k'_p(\mu_p C_{ox}/2)$	19	$\mu A/V^2$
μ_n Low-field mobility	467	$cm^2/V sec$
μ_p Low-field mobility	153	$cm^2/V sec$
C_{ox}	2.5	$fF/\mu m^2$
V_T (n-channel)	0.8	V
V_T (p-channel)	-0.93	V
Capacitance		
M2:M3 Area	32	$aF/\mu m^2$
Fringe	50	$aF/\mu m$
Poly:poly2 Area	940	$aF/\mu m^2$
Electromigration Limits	2.2	$mA/\mu m$
Fill Rules		
Poly 1	15	%
Metal 1	30	%
Metal 2	30	%
Antenna Rules		
Poly to Gate Area	< 100	$\mu m^2/\mu m^2$
Metal 1 to Gate Area	< 100	$\mu m^2/\mu m^2$
Metal 2 to Gate Area	< 100	$\mu m^2/\mu m^2$
Metal 3 to Gate Area	< 100	$\mu m^2/\mu m^2$
DIP40 temperature coefficient	25	deg C/W

Table C.1: Selected Process Parameters Considered in Design (Source – MO-SIS).

Biography of the Authors

Ron Bryant was born in London, England on May 26, 1952. He immigrated to the U.S. in 1957 and grew up in Pontiac, Michigan.

He entered the Massachusetts Institute of Technology in 1971 and obtained his Bachelor of Science degree in Chemistry in 1974 and Master of Science Degree in Biochemistry in 1975.

In September 1975 he enrolled in Medical School at the University of Michigan. He graduated in 1979 and began specialty training in Pathology at the University of Vermont. In 1983 he received specialty certification from the American Board of Pathology and began working at Eastern Maine Medical Center in Bangor, Maine. He retired from the position of Chief of Pathology at the medical center in December 1996. In January 1997, he was enrolled for graduate study in Electrical Engineering at the University of Maine and received a Master of Science degree in Electrical Engineering. Ron is currently a candidate for the Doctorate degree in Electrical Engineering from The University of Maine.

Scott Saucier was born in Bangor, Maine on November 16, 1976. He has lived in Bangor for most of his life, where he attended John Bapst Memorial High School.

Upon graduation in 1995 he began classes at the University of Maine where he studied Electrical Engineering. He began working on various research projects for the Communications Laboratory in the department in 1996, and received a Bachelor of Science degree in Electrical Engineering in 2000. Scott is currently a candidate for the Master of Science degree in Electrical Engineering.