Characterization of Fabricated Chips

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Abstract

The Sigma-Delta Modulator is use to eliminate the quantization error produced during analog to digital conversions. It performs its task by pushing this error into a higher frequency band so the original signal can be low pass filtered and recovered. The chip contains many smaller circuits including First Order Loop, Operational Amplifier, Comparator, Flip-Flop, and Digital to Analog Converter. The function of each of these circuits will be verified and compared to the results obtained using the simulations in Cadence. This is the desired procedure since it is easier to detect which circuit within the chip is not functioning properly. It was also intended to test the chip using Probe Station with LabView. However this procedure was not performed because the equipment did not arrive in the laboratory. The AutoRanger Circuit and some smaller circuits within the PID Controller were also characterized. The AutoRanger Circuit is use to measure resistance in sensor devices. It compares a sensor's resistance to a series of reference resistance within the chip. PID is the most popular algorithm used for industrial control systems. The tested PID controller consists of Variable Resistor and Operational Amplifier.

Introduction

Three different types of fabricated chips were characterized for this project. They are Sigma-Delta Modulator, PID Controller, and AutoRanger Circuit. These were final projects designed by graduate students taking ECE 547. Each of them contains 40 different pins and five chips of each type were tested. These chips were fabricated by MOSIS in a 0.5 micron AMI process. Different types of chips contain various components. The Sigma-Delta Modulator consists of First Order Loop, Operational

Amplifier, Comparator, Flip-Flop, and Digital to Analog Converter. The PID Controller consists of Comparator, Variable Resistor, Operational Amplifier, and Voltage Divider. The AutoRanger Circuit consists of Flip-Flop, Input Package, 3-bit Up/Down Counter, 3-8 Decoder, and BCD Encoder. Equipments manufactured by Agilent were used in the project. They include 33120 Signal Generator, 54621A Oscilloscope, 33120A Triple Output Power Supply, and 35620A Dynamic Spectrum Analyzer. A multimeter was also needed to test the variable resistor in the PID Controller.

Results and Discussion

Sigma-Delta Modulator

A. First Order Loop Testing

There is no pulse density modulated signal in the transient output when the amplitude of the input signal is 500mV. The amplitude had to be lowered to 160mV for the modulated signal to appear. Then a Spectrum Analyzer was used to measure resolution. Results show that increasing the clock frequency up to 3 MHz will increase resolution. The data collected for this test is illustrated in Tables 1-5 and Figures 1-5 of Appendix A.

B. Operational Amplifier Testing

The Operational Amplifier could not be tested because there is a buffer connected to the amplifier within the chip.

C. Comparator Testing

The output is a square wave with the same frequency of the input signal. This frequency is 1 kHz. The amplitude of the square wave is 2.344V. Therefore half of the maximum value is 1.172V. There is no ringing and a small offset of 0.156V. The data collected for the comparator is illustrated in the following table:

	propagation delay (ns)	max. frequency (MHz)	slewing (ns)
chip 1	109.2	4.6	77
chip 2	104	3.36	77
chip 3	107.3	4.3	73
chip 4	90	4	74
chip 5	140	4.5	74

D. Flip-Flop Testing

We were instructed to test the flip-flops using an input signal with a voltage of 2.5V peak-to-peak. However the flip-flop output was triggering on both the rising edge and the falling edge of the clock when the amplitude of the input signal is 2.5V peak-to-peak. The signal generators produce signals with overshoots. Therefore a 2.5V peak-to-peak signal produced by the generators actually has a higher peak-to-peak voltage if the overshoots are taken into considerations. The transmission gates within the D Latches do not support voltages higher than 2.5V. If the input signal has a voltage greater than 2.5V, the transmission gates inside these latches give the same output whether the state of the clock signal is high or low. This problem can be solved by lowering the voltage of the input signal to 1.5V. The actual voltage of the input signal would be approximately 2.3V if overshoots were taken into considerations. Then this flip-flop would function properly since this voltage is lower than 2.5V. No limitations were detected in the flip-flop at high frequencies. The data collected for the Flip-Flop is illustrated in the following table:

	rise time (ns)	fall time (ns)
chip 1	45	61
chip 2	46	60
chip 3	47	62
chip 4	46.3	62.5
chip 5	45	60

E. Digital to Analog Converter Testing

The oscilloscope showed a scaled version of the input signal. It was symmetrical around 0V. The output remained almost the same after the input frequency was increased to 10kHz. However the edges of the signal tilted a little from a vertical line. The data collected for the Digital to Analog Converter is illustrated in the following table:

	Peak to peak voltage	scale
chip 1	0.825	3.030
chip 2	0.807	3.098
chip 3	0.832	3.005
chip 4	0.850	2.941
chip 5	0.807	3.098

PID Controller

A. Comparator Testing

There are two separate tests for the comparator. The first test is to verify its functionality and the second test is to detect its offset voltage. The inverting terminal voltage varies between 0V and 5V during the first testing. The output voltage of the comparator is 0V when the inverting terminal voltage is less than half of the reference voltage of V_{dd}. The output voltage is approximately equal to the reference voltage when the inverting terminal voltage is greater than half of the reference voltage. There is no offset voltage in the comparator since the output voltage is equal to the non-inverting terminal voltage in the second testing. The data collected for the comparator is illustrated in Tables 1-5A and Figures 1-5 of Appendix B.

B. Variable Resistor Testing

The input voltage varies between 0V and 5V. Results show that increasing the input voltage up to 5V will decrease resistance. The data collected for the variable resistor is illustrated in Tables 6-10 and Figures 6-10 of Appendix B.

C. Operational Amplifier: DC Test

The input voltage varies between 0V and 5V and the output voltage usually varies between 2.77V and 2.56V. The offset voltage ranges from 0.18V to 0.19V. Results show that increasing the input voltage up to 5 V will decrease the output voltage. The data obtained for the DC test of the Operational Amplifier is shown in Tables 11-15 of Appendix B.

D. Operational Amplifier: AC Test

The AC Test had to be modified because the Operational Amplifier is not functional under the original conditions. The input signal had to be given an offset voltage of 2.6V and its amplitude had to be increased from 100 mV_{pp} to 1.5 $V_{pp.}$ The 100k resistor in the original experiment had to be replaced with a 20k resistor. According to the experimental data, the frequency when the gain is unity ranges from 525 kHz to 540 kHz. The data obtained for the AC test of the Operational Amplifier is shown in Tables 16-20 of Appendix B.

E. Voltage Divider Testing

The voltage dividers were tested using a power supply of 5V. The voltages generated by the voltage dividers of these five chips are as follows:

	Output Voltage
chip 1	4.56
chip 2	4.56
chip 3	4.55
chip 4	4.57
chip 5	4.57

AutoRanger Circuit

A. D Flip-Flop Testing

The D flip-flops of these five chips were tested using a square wave of 1 Hz and a reference voltage of 5 V. This flip-flop has one input pin and one output pin. There are two different types of inputs. They are 1 and 0. The input 1 is represented by a voltage of 5V and the input 0 is represented by a voltage of 0V. The output is exactly the same as the input. The output is 5V if the input is 5V and the output is 0V if the input is 0V. However the output appears on the oscilloscope one clock cycle after the change of input. The operations of these D Flip-Flops match the descriptions provided by the following truth table:

D input at (t)	D output at (t+1)
1	1
0	0

B. JK Flip-Flop Testing

The JK flip-flops of these five chips were tested using a square wave of 1 Hz and a reference voltage of 5V. This flip-flop has two input pins and one output pin. The two input pins are represented by J and K and the output pin is represented by Q. There are two different types of inputs. They are 1 and 0. The input 1 is represented by a voltage of 5V and the input 0 is represented by a voltage of 0V. The operations of these JK Flip-Flops match the descriptions provided by the following truth table:

J	K	Q(t)	Q(t+1)	Function
0	0	0	0	Hold
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

C. Input Package Testing

The voltage dividers were tested using a power supply of 5V. Pin 27 is the output of the 2.15V voltage divider and pin 28 is the output of the 4V voltage divider. The voltages generated by the voltage dividers of these five chips are as follows:

	pin 27	pin 28
chip 1	2.181V	4.150V
chip 2	1.810V	3.580V
chip 3	1.786V	3.565V
chip 4	1.995V	4.065V
chip 5	2.257V	4.193V

The operations of the input packages follow the descriptions provided by the table below. Pin 11 is the input of the package. The outputs of the package are Pin 27, Pin 28, Pin 31,

and Pin 32. Clocking occurs at pin 18 when the input voltage is less than approximately 1.8V. Then clocking also occurs at pin 17 when the input voltage is greater than approximately 3.8V.

Input (Pin 11)	Pin 31	Pin 32	Pin 17	Pin 18
Pin 11<Pin 27	0V	5V	Off-0V	Clocking
Pin 27<Pin 11<Pin 28	0V	0V	Off-0V	Off-0V
Pin 11>Pin 28	5V	0V	Clocking	Off-0V

D. 3-bit Up/Down Counter, 3-8 Decoder, BCD Encoder & Entire AutoRanger Circuit

The 3-bit up/down counters, 3-8 decoder, and BCD encoder of these five chips were tested using two different voltage sources. One of them is the input voltage source and the other is a reference voltage of 5V. LEDs were originally used to verify the operations of the devices. However they failed to test the operations of the chips. The LED at pin 37 blinks when the input voltage is greater than approximately 1.8V. It completely lights itself up when the input voltage is greater than approximately 3.8V. The LEDs at other pins of these devices did not function at all. Therefore the testing procedures had to be modified. Each of the pins was connected to the oscilloscope instead. Then the voltages of these pins were measured while the input voltage was varied at the same time. Each of these pins was separately tested instead. The pin is at the state of zero when the measured voltage is zero and at the state of one when the measured voltage is around five. As the input voltage varied quickly between 0V and 5V during this experiment, the patterns of how voltages in each of these pins toggled correspond to the descriptions provided by the following table:

Pins

State	40	1	2	3	4	5	6	38	39	7	8	9	10	35	36	37
-1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
2	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0
3	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1
4	0	0	1	0	0	0	0	0	0	0	1	0	0	1	0	0
5	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0	1
6	1	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0
7	1	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0

Conclusions:

According to the experimental data, five samples of the Sigma-Delta Modulator and four samples of the AutoRanger Circuit confirm the results obtained in Cadence Simulations. One of the AutoRanger Circuits did not function at all. The output of the voltage divider in the PID Controller is different from the simulated value. According to the software Cadence, this output is supposed to be a value between 2.3V and 2.7V. However the output voltage of the device is around 4.56V. These fabricated chips will be characterized again using Probe Station with LabView. This extra characterization will determine whether the designs of any of these chips needed to be modified.

Appendix A:

Chip 1			
clock frequency	peak (dB)	noise floor (dB)	resolution (dB)
1 MHz	-19.412	-48.477	29.065
2 MHz	-17.195	-56.069	38.874
3 MHz	-17.044	-76.104	59.06
4 MHz	-17.077	-66.101	49.024
5 MHz	-17.084	-66.759	49.675
6 MHz	-17.069	-70.446	53.377
7 MHz	-17.06	-66.036	48.976
8 MHz	-17.066	-61.195	44.129
9 MHz	-17.077	-60.962	43.885
10 MHz	-17.082	-61.116	44.034
11 MHz	-17.085	-62.905	45.82
12 MHz	-17.08	-63.781	46.701

Table 1:

Chip 2			
clock frequency	peak (dB)	noise floor (dB)	resolution (dB)
1 MHz	-20.181	-45.114	24.933
2 MHz	-17.626	-54.66	37.034
3 MHz	-17.41	-76.58	59.17
4 MHz	-17.445	-66.407	48.962
5 MHz	-17.455	-67.573	50.118
6 MHz	-17.437	-72.084	54.647
7 MHz	-17.425	-66.028	48.603
8 MHz	-17.432	-61.164	43.732
9 MHz	-17.451	-60.76	43.309
10 MHz	-17.459	-62.049	44.59
11 MHz	-17.457	-63.384	45.927
12 MHz	-17.449	-63.996	46.547

Table 2:

Chip 3			
clock frequency	peak (dB)	noise floor (dB)	resolution (dB)
1 MHz	-19.841	-47.18	27.339
2 MHz	-17.439	-55.081	37.642
3 MHz	-17.249	-75.792	58.543
4 MHz	-17.285	-66.218	48.933
5 MHz	-17.291	-67.237	49.946
6 MHz	-17.276	-70.925	53.649
7 MHz	-17.266	-65.855	48.589
8 MHz	-17.274	-62.069	44.795
9 MHz	-17.287	-60.967	43.68
10 MHz	-17.292	-61.401	44.109
11 MHz	-17.294	-63.102	45.808
12 MHz	-17.287	-63.744	46.457

Table 3:

Chip 4			
clock frequency	peak (dB)	noise floor (dB)	resolution (dB)
1 MHz	-19.746	-47.344	27.598
2 MHz	-17.381	-54.496	37.115
3 MHz	-17.182	-76.158	58.976
4 MHz	-17.217	-66.098	48.881
5 MHz	-17.227	-66.865	49.638
6 MHz	-17.209	-70.714	53.505
7 MHz	-17.199	-65.899	48.7
8 MHz	-17.207	-61.925	44.718
9 MHz	-17.219	-60.755	43.536
10 MHz	-17.225	-61.287	44.062
11 MHz	-17.227	-63.009	45.782
12 MHz	-17.22	-63.747	46.527

Table 4:

Chip 5

clock frequency	peak (dB)	noise floor (dB)	difference (dB)
1 MHz	-19.335	-47.935	28.6
2 MHz	-17.152	-56.377	39.225
3 MHz	-17.003	-76.473	59.47
4 MHz	-17.036	-66.063	49.027
5 MHz	-17.043	-67.104	50.061
6 MHz	-17.041	-70.699	53.658
7 MHz	-17.032	-65.749	48.717
8 MHz	-17.038	-61.521	44.483
9 MHz	-17.05	-60.562	43.512
10 MHz	-17.056	-61.149	44.093
11 MHz	-17.058	-62.928	45.87
12 MHz	-17.05	-63.497	46.447

Table 5:

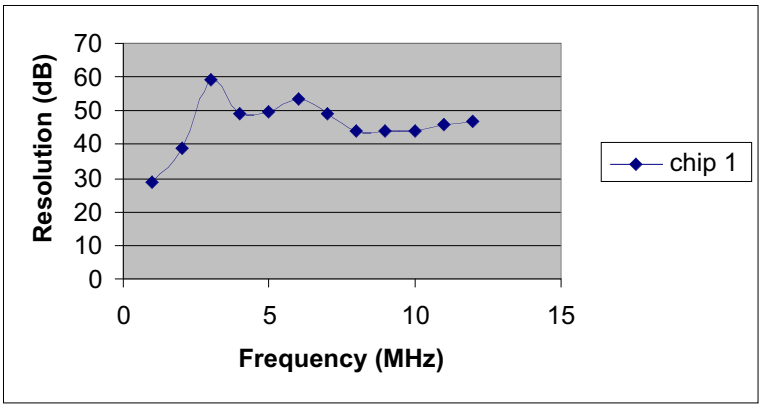


Figure 1:

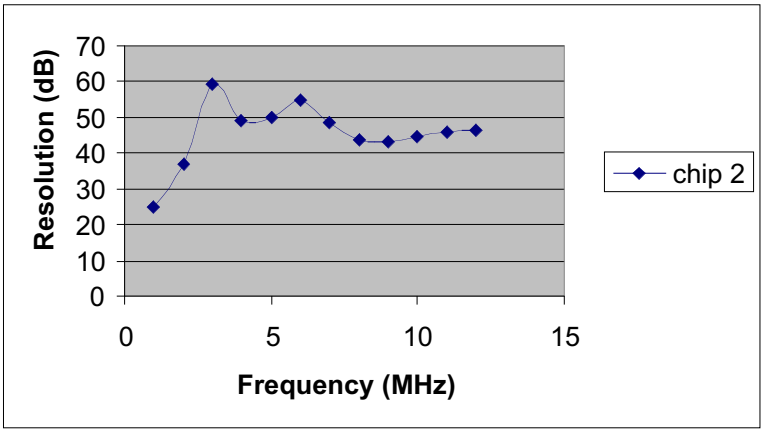


Figure 2:

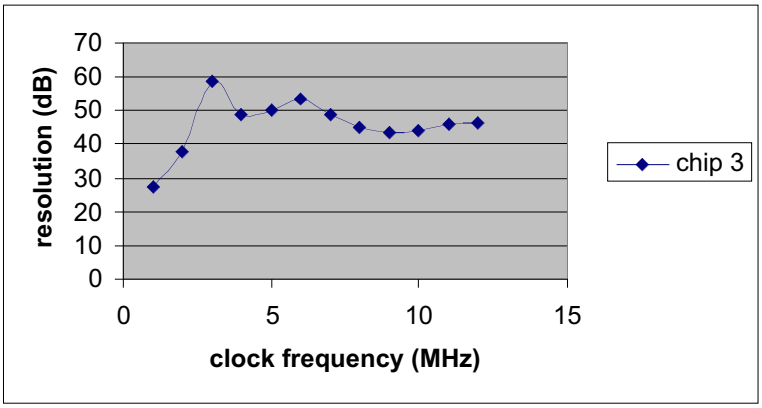
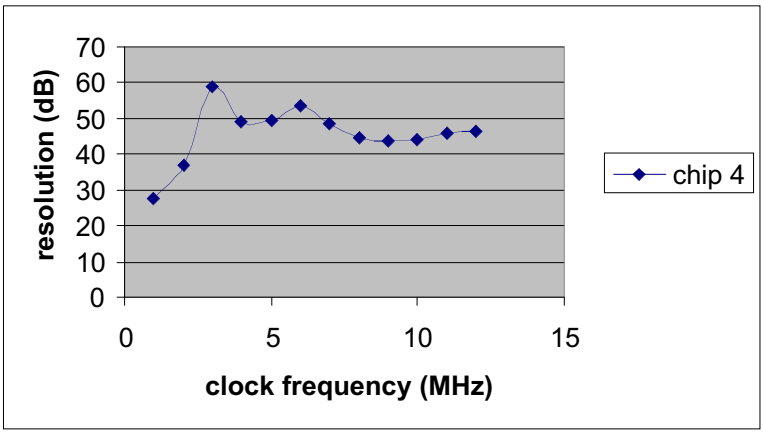


Figure 3:



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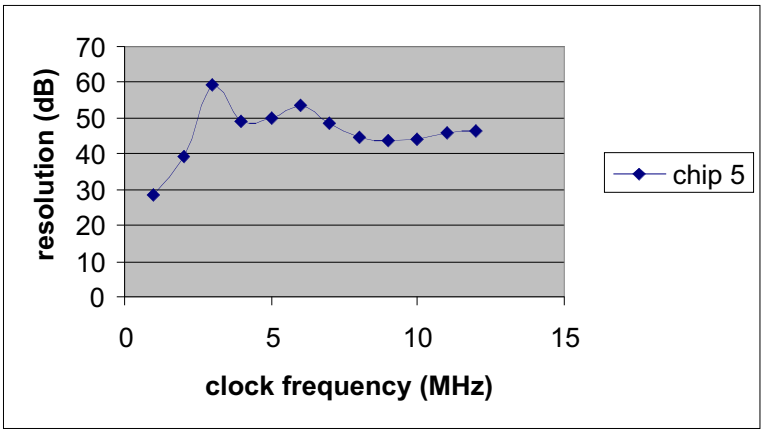

Figure 5:

Appendix B:

Chip 1							
Inverting Terminal Voltage	**Output Voltage VDD = 5V**	**Output Voltage VDD = 4.5V**	**Output Voltage VDD = 4V**	**Inverting Terminal Voltage**	**Output Voltage VDD = 5V**	**Output Voltage VDD = 4.5V**	**Output Voltage VDD = 4V**
Pin 23	**Pin 25**	**Pin 25**	**Pin 25**	**Pin 23**	**Pin 25**	**Pin 25**	**Pin 25**
0	0	0	0	2.6	4.83	4.48	4.03
0.1	0	0	0	2.7	4.84	4.49	4.03
0.2	0	0	0	2.8	4.85	4.49	4.03
0.3	0	0	0	2.9	4.86	4.49	4.03
0.4	0	0	0	3	4.86	4.49	4.03
0.5	0	0	0	3.1	4.87	4.49	4.03
0.6	0	0	0	3.2	4.87	4.49	4.03
0.7	0	0	0	3.3	4.87	4.49	4.03
0.8	0	0	0	3.4	4.87	4.49	4.03
0.9	0	0	0	3.5	4.87	4.49	4.03
1	0	0	0	3.6	4.87	4.49	4.03
1.1	0	0	0	3.7	4.87	4.49	4.03
1.2	0	0	0	3.8	4.87	4.49	4.03
1.3	0	0	0	3.9	4.87	4.49	4.03
1.4	0	0	0	4	4.87	4.49	4.03
1.5	0	0	0	4.1	4.91	4.49	4.03
1.6	0	0	0	4.2	4.91	4.49	4.03
1.7	0	0	0	4.3	4.91	4.49	4.03
1.8	0	0	0	4.4	4.9	4.49	4.03
1.9	0	0	0	4.5	4.91	4.49	4.03
2	0	0	3.94	4.6	4.91	4.49	4.03
2.1	0	0	4.02	4.7	4.91	4.49	4.03
2.2	0	4.3	4.03	4.8	4.9	4.49	4.03
2.3	0.02	4.44	4.03	4.9	4.91	4.49	4.03
2.4	4.51	4.47	4.03	5	4.91	4.49	4.03
2.5	4.78	4.48	4.03				

Table 1:

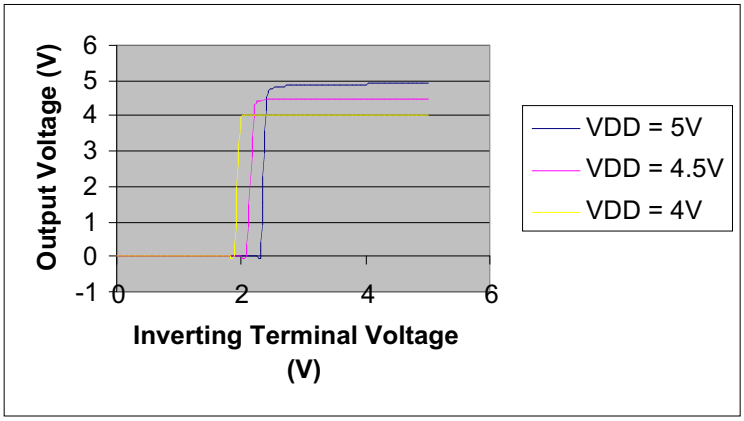

Figure 1:

Chip 2							
Inverting Terminal Voltage	**Output Voltage VDD = 5V**	**Output Voltage VDD = 4.5V**	**Output Voltage VDD = 4V**	**Inverting Terminal Voltage**	**Output Voltage VDD = 5V**	**Output Voltage VDD = 4.5V**	**Output Voltage VDD = 4V**
Pin 23	**Pin 25**	**Pin 25**	**Pin 25**	**Pin 23**	**Pin 25**	**Pin 25**	**Pin 25**
0	0	0	0	2.6	4.83	4.49	4.02
0.1	0	0	0	2.7	4.84	4.49	4.02
0.2	0	0	0	2.8	4.85	4.49	4.02
0.3	0	0	0	2.9	4.86	4.49	4.02
0.4	0	0	0	3	4.86	4.49	4.02
0.5	0	0	0	3.1	4.87	4.49	4.02
0.6	0	0	0	3.2	4.87	4.49	4.02
0.7	0	0	0	3.3	4.87	4.49	4.02
0.8	0	0	0	3.4	4.87	4.49	4.02
0.9	0	0	0	3.5	4.87	4.49	4.02
1	0	0	0	3.6	4.87	4.49	4.02
1.1	0	0	0	3.7	4.88	4.49	4.02
1.2	0	0	0	3.8	4.88	4.49	4.02
1.3	0	0	0	3.9	4.88	4.49	4.02
1.4	0	0	0	4	4.88	4.49	4.02
1.5	0	0	0	4.1	4.88	4.49	4.02
1.6	0	0	0	4.2	4.88	4.49	4.02
1.7	0	0	0	4.3	4.88	4.49	4.02
1.8	0	0	0	4.4	4.88	4.49	4.02
1.9	0	0	0	4.5	4.88	4.49	4.02
2	0	0	3.95	4.6	4.88	4.49	4.02
2.1	0	0	4.01	4.7	4.88	4.49	4.02
2.2	0	4.31	4.02	4.8	4.88	4.49	4.03
2.3	0.08	4.44	4.02	4.9	4.88	4.49	4.03
2.4	4.57	4.47	4.02	5	4.88	4.49	4.03
2.5	4.79	4.48	4.02				

Table 2:

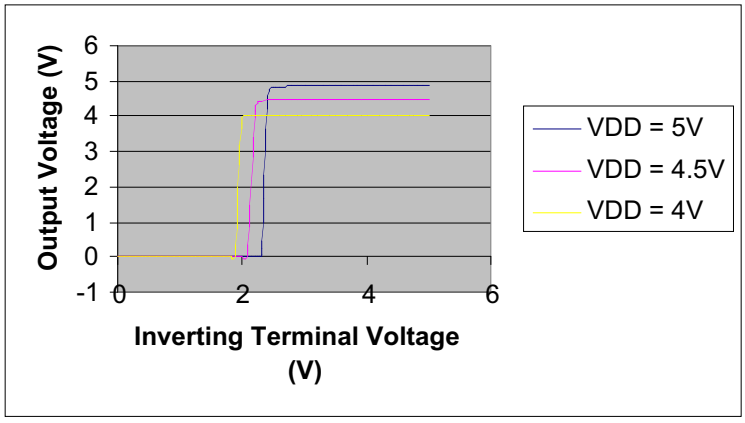

Figure 2:

Chip 3							
Inverting Terminal Voltage	**Output Voltage VDD = 5V**	**Output Voltage VDD = 4.5V**	**Output Voltage VDD = 4V**	**Inverting Terminal Voltage**	**Output Voltage VDD = 5V**	**Output Voltage VDD = 4.5V**	**Output Voltage VDD = 4V**
Pin 23	**Pin 25**	**Pin 25**	**Pin 25**	**Pin 23**	**Pin 25**	**Pin 25**	**Pin 25**
0	0	0	0	2.6	4.8	4.48	4.02
0.1	0	0	0	2.7	4.83	4.48	4.02
0.2	0	0	0	2.8	4.84	4.48	4.02
0.3	0	0	0	2.9	4.85	4.48	4.03
0.4	0	0	0	3	4.86	4.48	4.03
0.5	0	0	0	3.1	4.86	4.49	4.03
0.6	0	0	0	3.2	4.86	4.49	4.03
0.7	0	0	0	3.3	4.86	4.49	4.03
0.8	0	0	0	3.4	4.9	4.49	4.03
0.9	0	0	0	3.5	4.9	4.49	4.03
1	0	0	0	3.6	4.9	4.49	4.03
1.1	0	0	0	3.7	4.9	4.49	4.03
1.2	0	0	0	3.8	4.9	4.49	4.03
1.3	0	0	0	3.9	4.9	4.49	4.03
1.4	0	0	0	4	4.9	4.49	4.03
1.5	0	0	0	4.1	4.9	4.49	4.03
1.6	0	0	0	4.2	4.9	4.49	4.03
1.7	0	0	0	4.3	4.9	4.49	4.03
1.8	0	0	0	4.4	4.9	4.49	4.03
1.9	0	0	0	4.5	4.9	4.49	4.03
2	0	0	3.7	4.6	4.9	4.49	4.03
2.1	0	0	3.99	4.7	4.9	4.49	4.03
2.2	0	0.47	4.02	4.8	4.9	4.49	4.03
2.3	0	4.38	4.02	4.9	4.9	4.49	4.03
2.4	0.32	4.46	4.02	5	4.9	4.49	4.04
2.5	4.71	4.48	4.02				

Table 3:

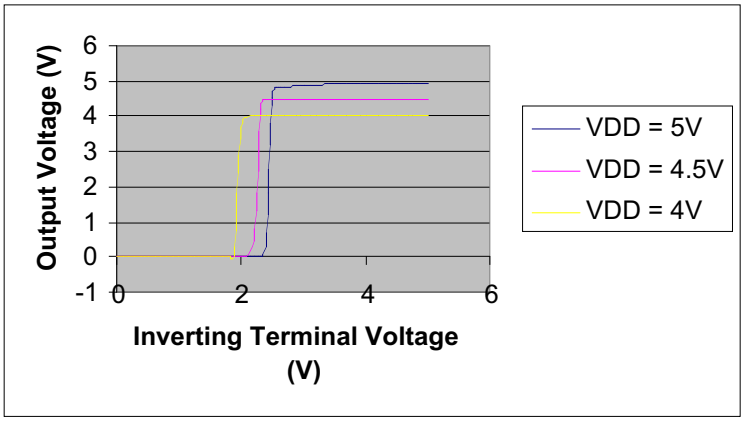

Figure 3:

Chip 4							
Inverting Terminal Voltage Pin 23	**Output Voltage VDD = 5V Pin 25**	**Output Voltage VDD = 4.5V Pin 25**	**Output Voltage VDD = 4V Pin 25**	**Inverting Terminal Voltage Pin 23**	**Output Voltage VDD = 5V Pin 25**	**Output Voltage VDD = 4.5V Pin 25**	**Output Voltage VDD = 4V Pin 25**
0	0	0	0	2.6	4.84	4.49	4.03
0.1	0	0	0	2.7	4.85	4.49	4.03
0.2	0	0	0	2.8	4.87	4.49	4.03
0.3	0	0	0	2.9	4.88	4.49	4.03
0.4	0	0	0	3	4.89	4.49	4.03
0.5	0	0	0	3.1	4.89	4.49	4.03
0.6	0	0	0	3.2	4.89	4.49	4.03
0.7	0	0	0	3.3	4.9	4.49	4.03
0.8	0	0	0	3.4	4.9	4.49	4.03
0.9	0	0	0	3.5	4.9	4.49	4.03
1	0	0	0	3.6	4.9	4.49	4.03
1.1	0	0	0	3.7	4.9	4.49	4.03
1.2	0	0	0	3.8	4.9	4.49	4.03
1.3	0	0	0	3.9	4.9	4.49	4.03
1.4	0	0	0	4	4.9	4.49	4.03
1.5	0	0	0	4.1	4.9	4.49	4.03
1.6	0	0	0	4.2	4.9	4.49	4.03
1.7	0	0	0	4.3	4.9	4.49	4.03
1.8	0	0	0	4.4	4.9	4.49	4.03
1.9	0	0	0	4.5	4.9	4.49	4.03
2	0	0	3.95	4.6	4.9	4.49	4.03
2.1	0	0	4.02	4.7	4.9	4.49	4.03
2.2	0	4.33	4.03	4.8	4.9	4.49	4.03
2.3	0.02	4.45	4.03	4.9	4.9	4.49	4.04
2.4	4.58	4.48	4.03	5	4.9	4.49	4.04
2.5	4.79	4.48	4.03				

Table 4:

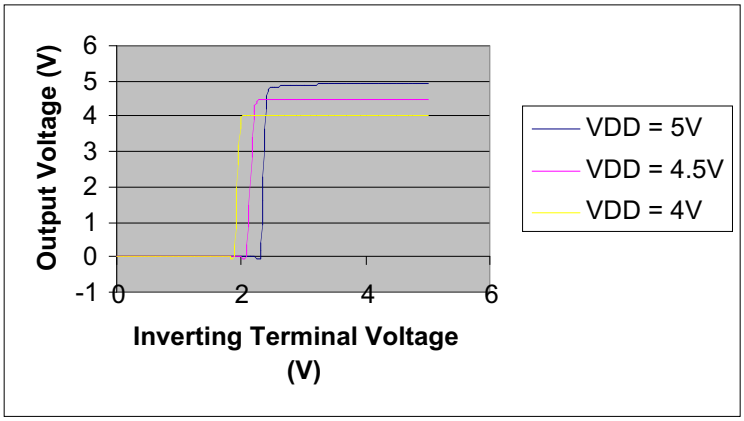

Figure 4: