ECE547 VLSI Layout and Design

PID Controller Project Final Report

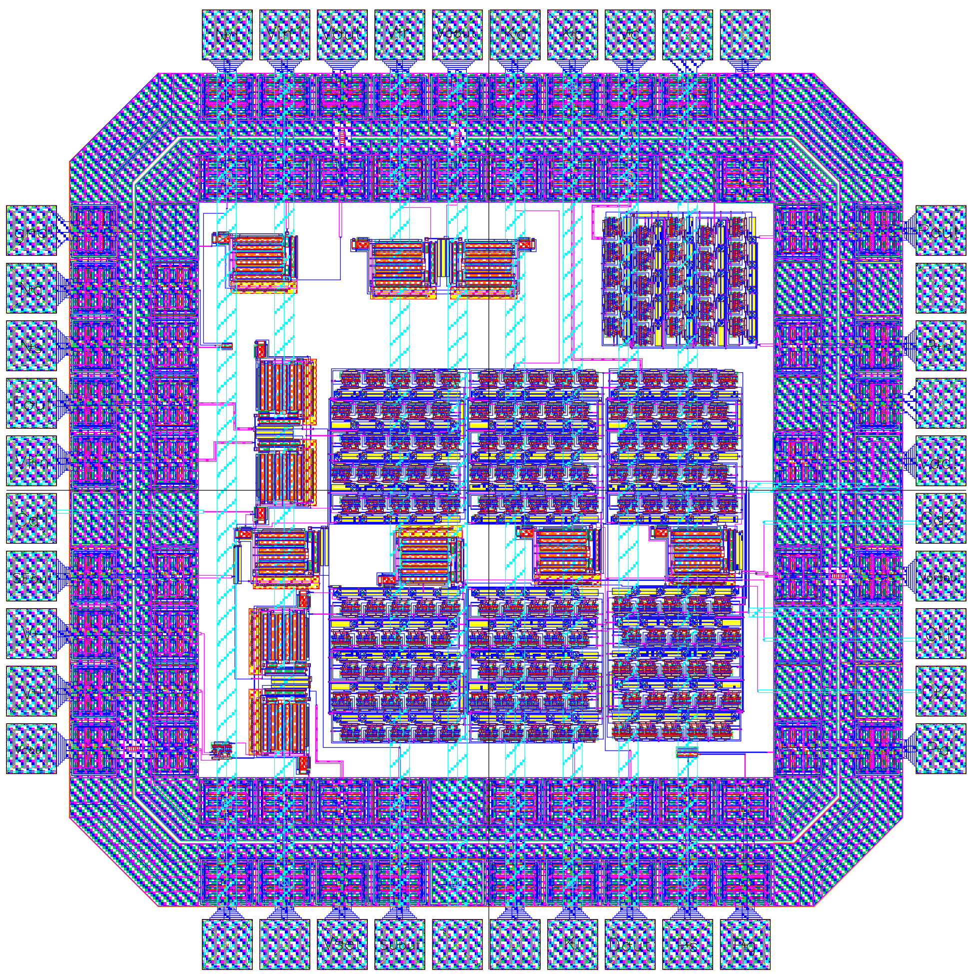
By Guang Chen; Zhiqiang Lin and Jie Zhou

Chapter 1 Project Overview

1.1 Project purpose

From SRD we know that they used isolated device to build up PID control for heater control system, they used Labview and PCI−GPIB board, the advantage of this control system is that it responses very fast, small steady error, very large gain, wide operation range. the disadvantage is the cost, this system is expensive and need more work on it

The classical PID control is very mature so maybe we can use VLSI technology to design the Proportional(P), Integral(I), and Derivative(D) parts in a chip. Inside the chip, we build up operation amplifiers, adjustable resistors, and combine them as a PID controller. Figure 1 is the overview of the chip. It is a 40 pins package.



1.2 PID control.

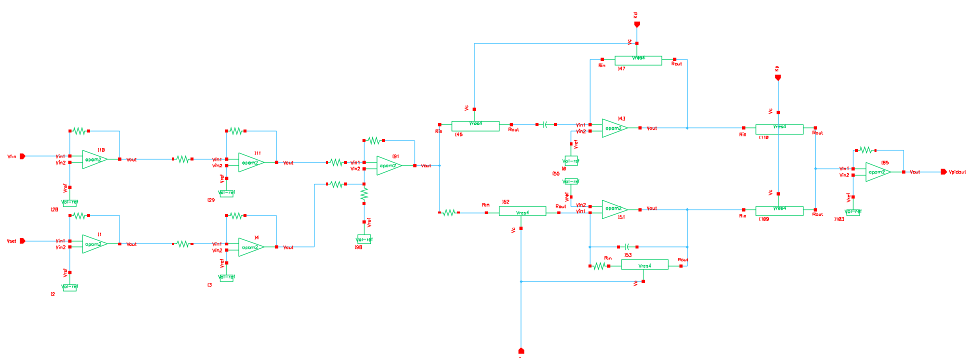
Proportional(P), Integral(I), and Derivative(D) form of control is the most popular algorithm used for industrial control, they are used very widely in industrial control systems.

We did a lot of work on how to get the desired PID controller, follow the steps below to obtain a desired response:

a. We design a general PID controller, we select the structure of the controller. Figure 2 is the schematic of the PID controller.

b. Designed the operation amplifier, adjustable resistor… and combined them to a single PID controller.

c. Build one order and two order operation plant to simulate the operation of the PID controller, find out what need to be improved, tune the three parameters (Kd, Ki, Kd) by adjusting the input voltage (0~5 V DC) until obtain a desired overall response for each operation plant.



1.3 VLSI technology

Integrated circuits (IC) technology is the enabling technology for a whole host of innovation devices and systems that have changed the way we live. There are some advantages at system level by using integrated circuits

. Smaller physical size

. Lower power consumption

. Reduced cost

1.4 CMOS technology

There are several different IC fabrication technologies. The most important difference between fabrication technologies is the type of transistors they can produce.

We choose COMS because of the extremely low power consumption of CMOS circuits. So we can put many transistors in a same chip by using CMOS.

Design and Testability

a. Hierarchical Design

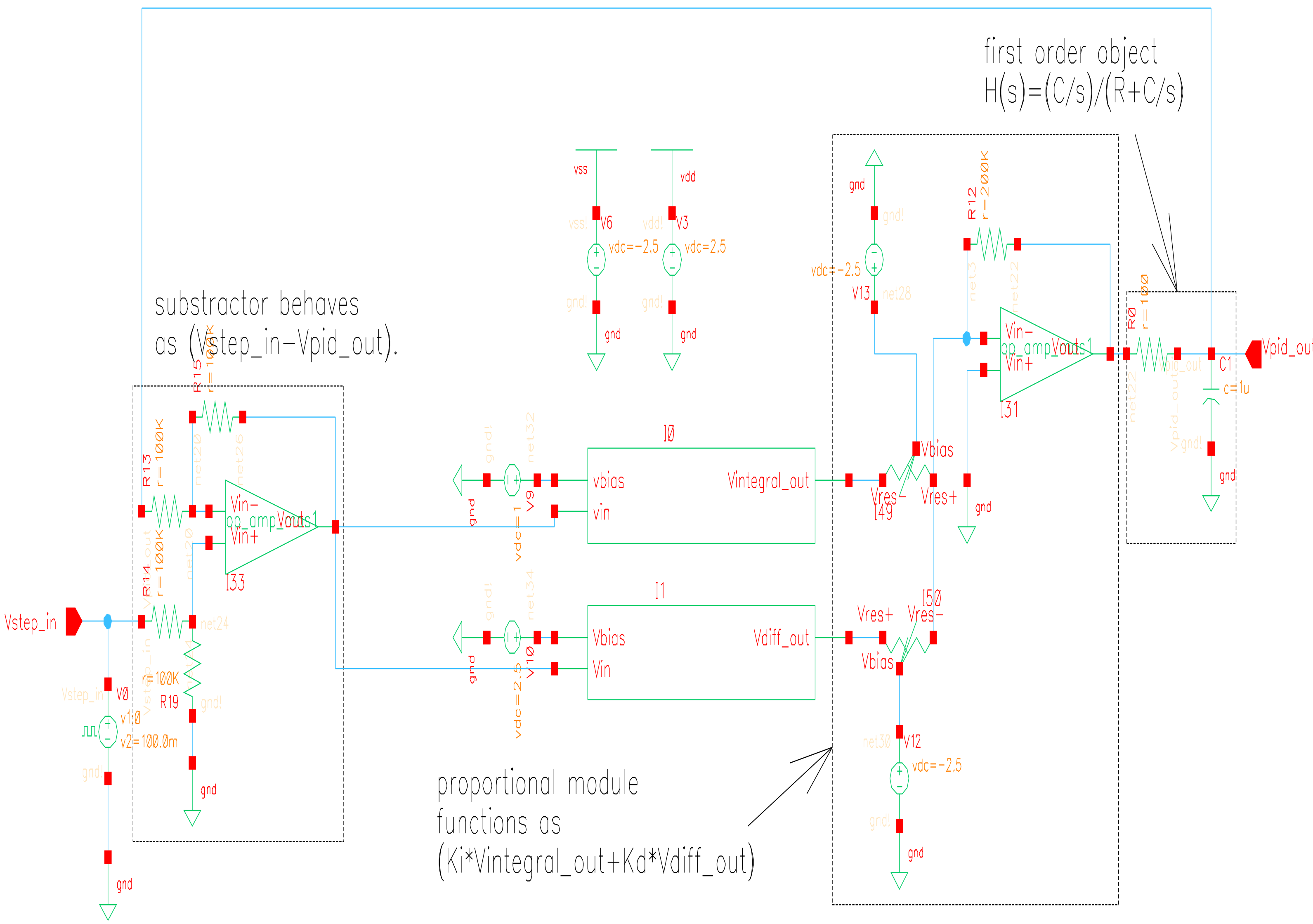
b. Design Abstraction

c. Computer−Aided Design(Cadence)

d. Testing

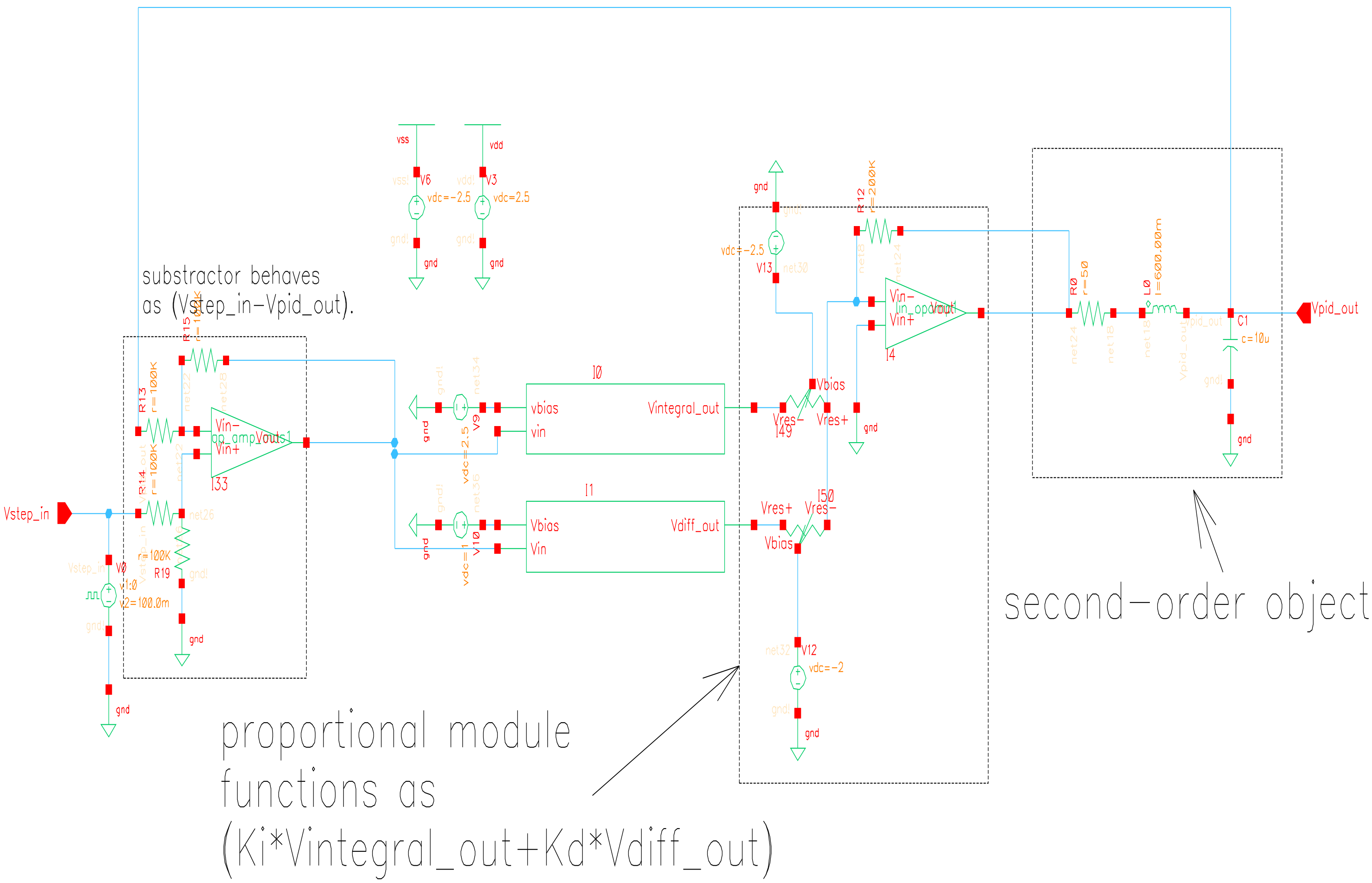
Chapter 2 circuits description:

1. PID controller working with a passive first−order object:
   Transfer function for a first−order object:
   H(s)=1/ (R*s/C+1)

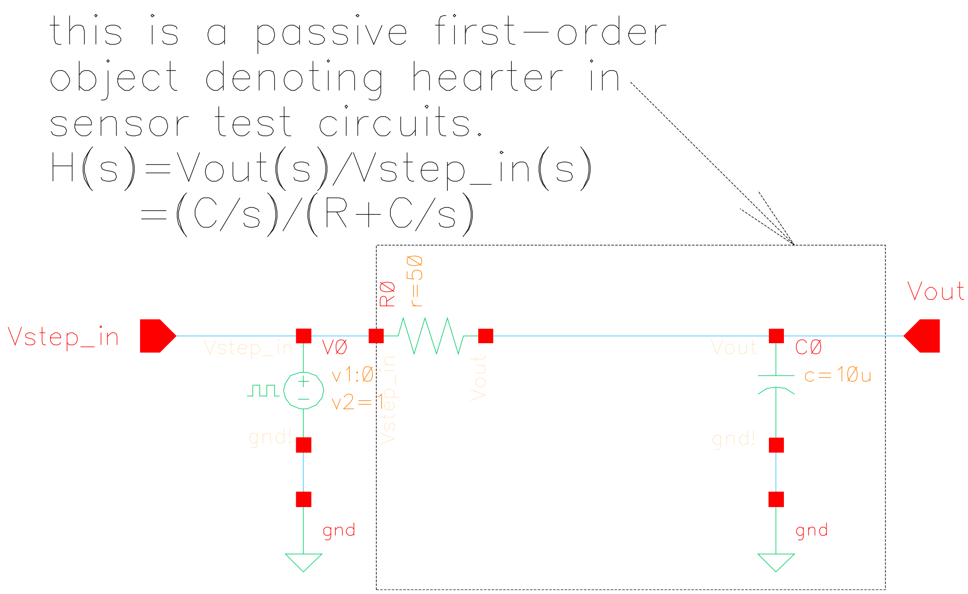


2. PID controller working with a passive second−order object:

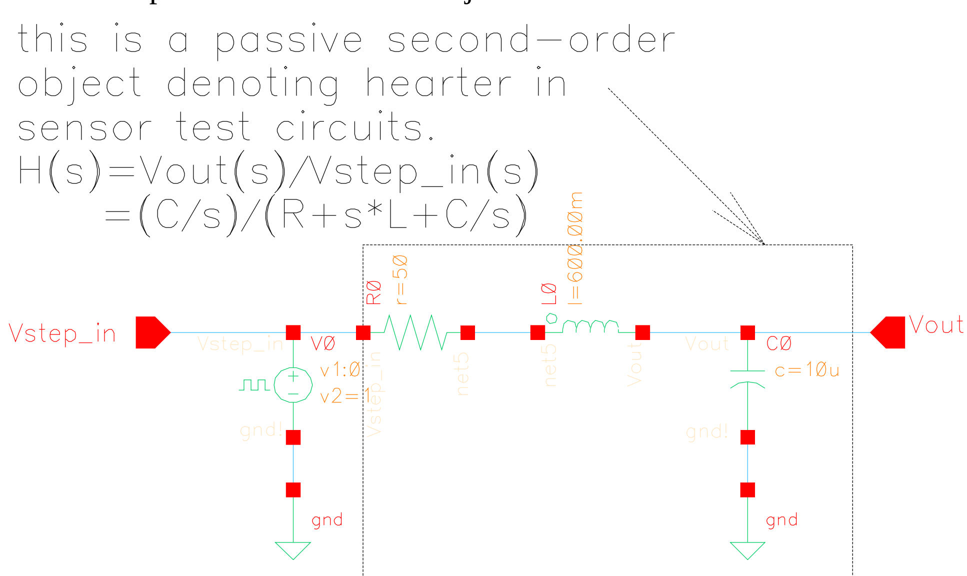
Transfer function for a second−order object: $H(s)=1/(L*s^2/C+R*s/C+1)$



3. Schematic of passive first−order object:

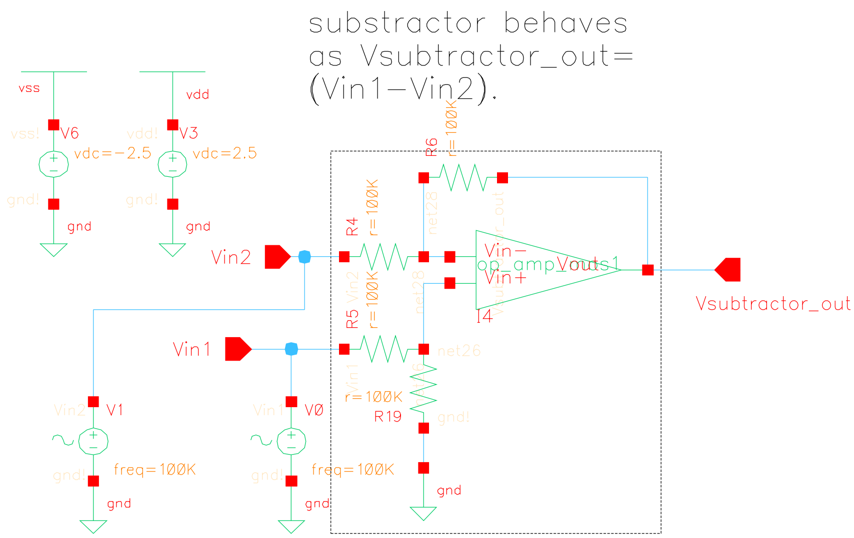


4. Schematic of passive second−order object:



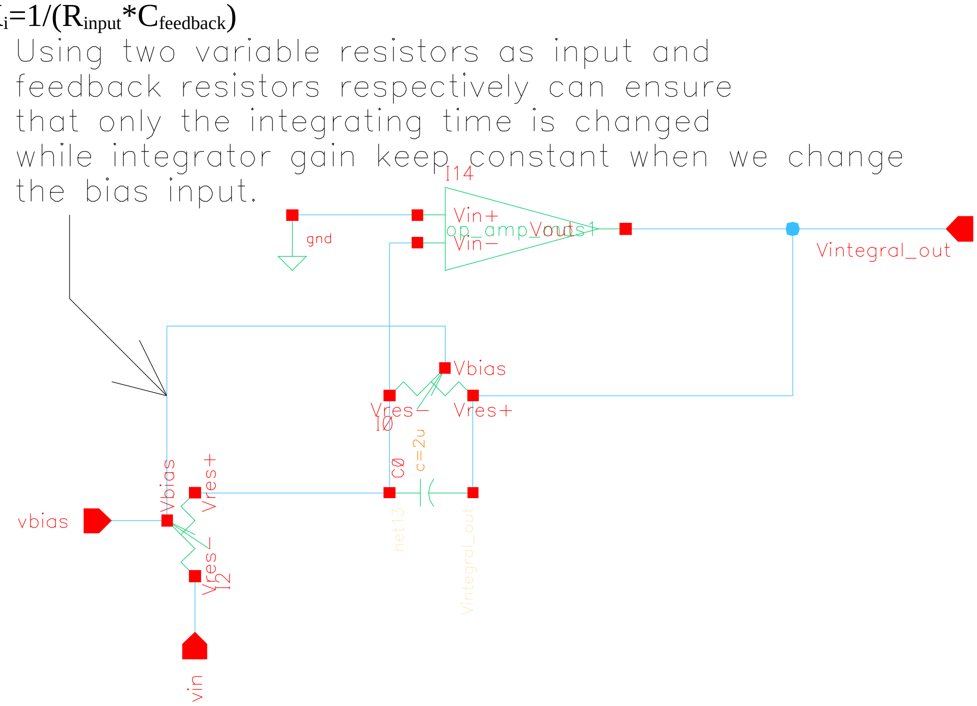
5. Subtractor used in the simulation of PID:

Subtractor is used to produce error signal from the difference between feedback(output of object) and set point.

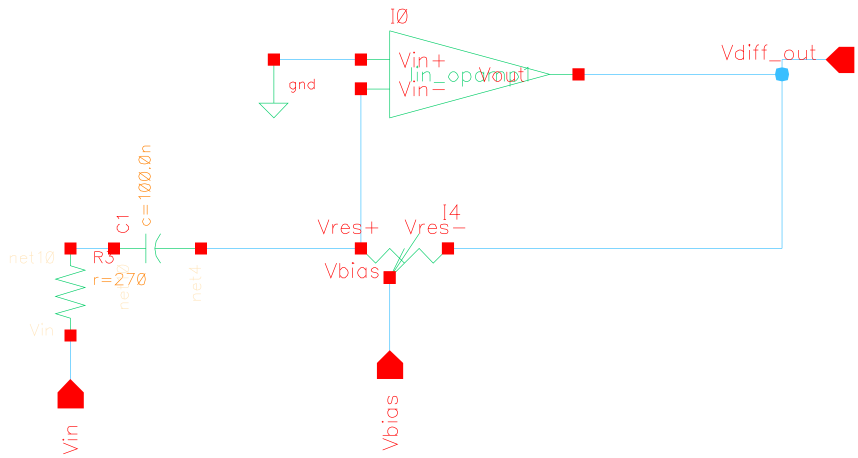


6. Integrator:

$K_i=1/(R_{input}*C_{feedback})$



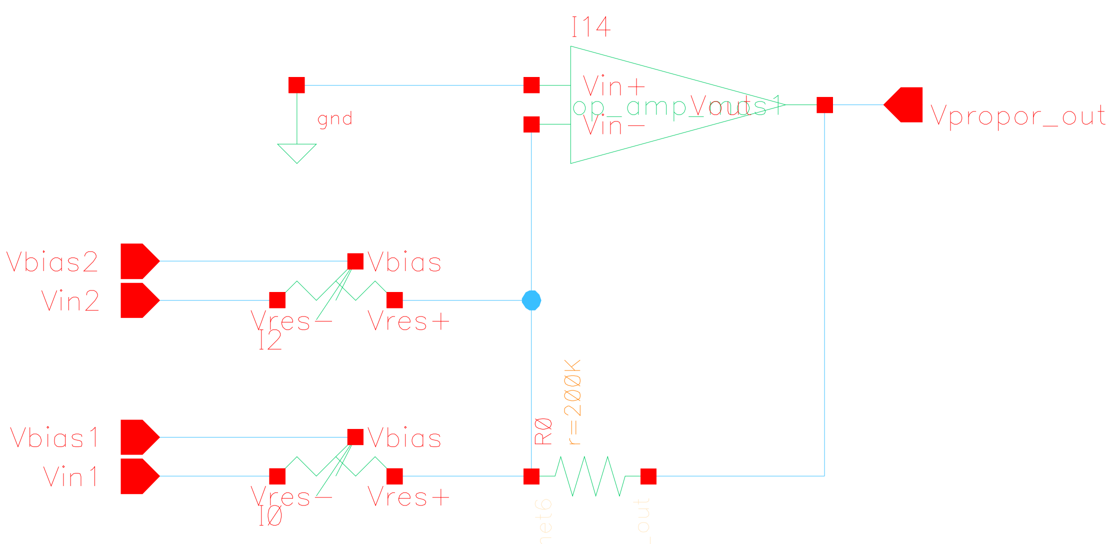
7. Differentiator:



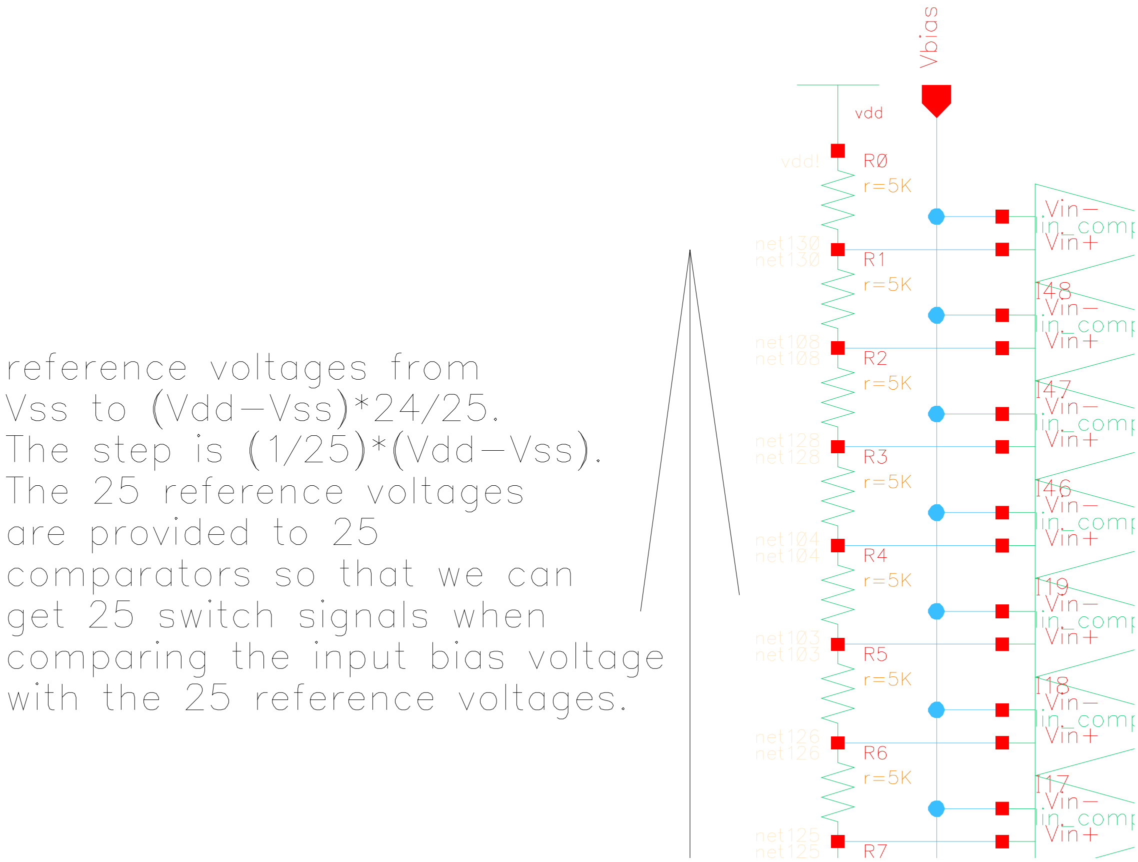
$K_d = R_{feedback} * C_{input}$

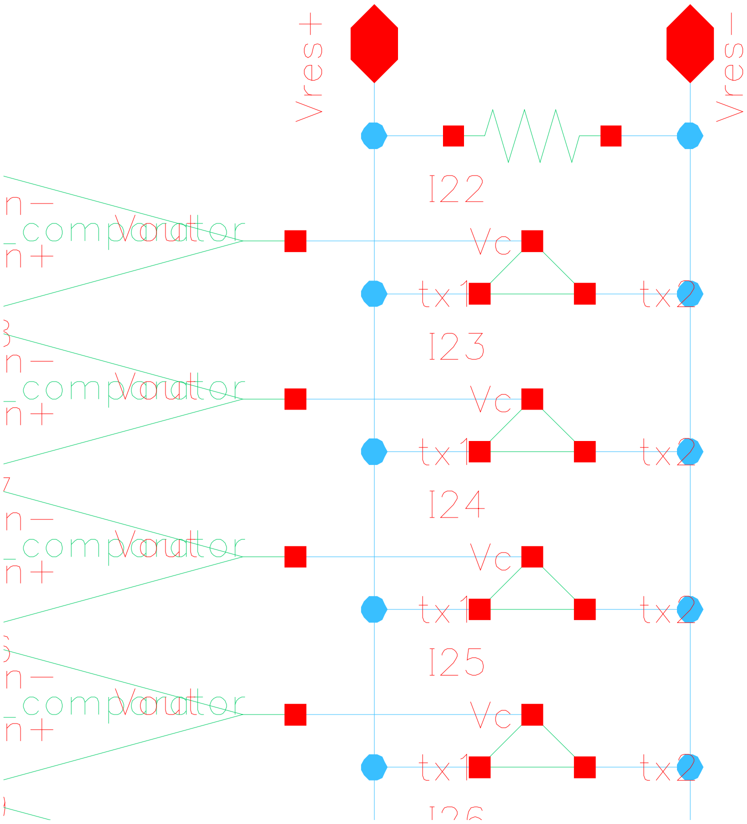
8. Proportional part:

The output of integrator and differentiator are connected to the proportional part through two variable resistors thus we can get individual gain for integrator and differentiator. $Kp = R_{feedback} / R_{input}$

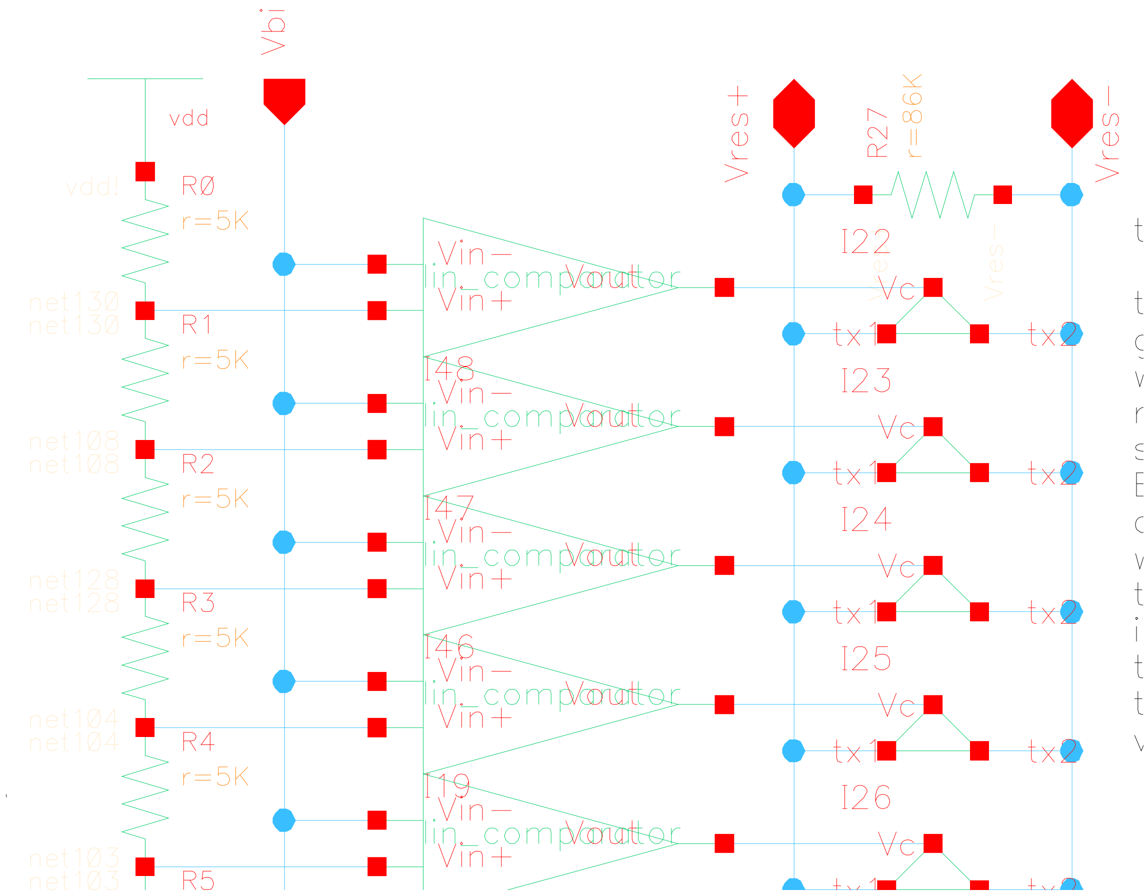


9. Voltage controlled resistor:

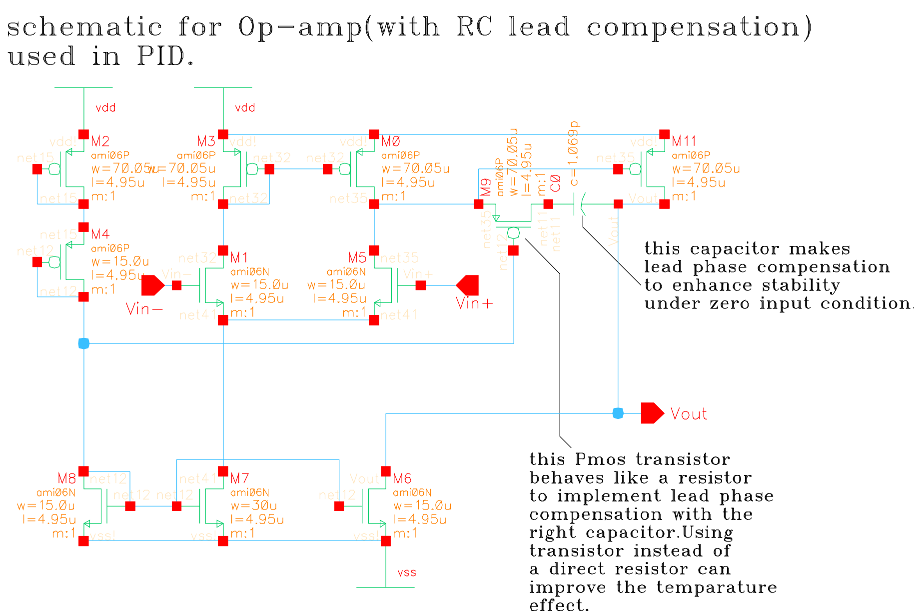




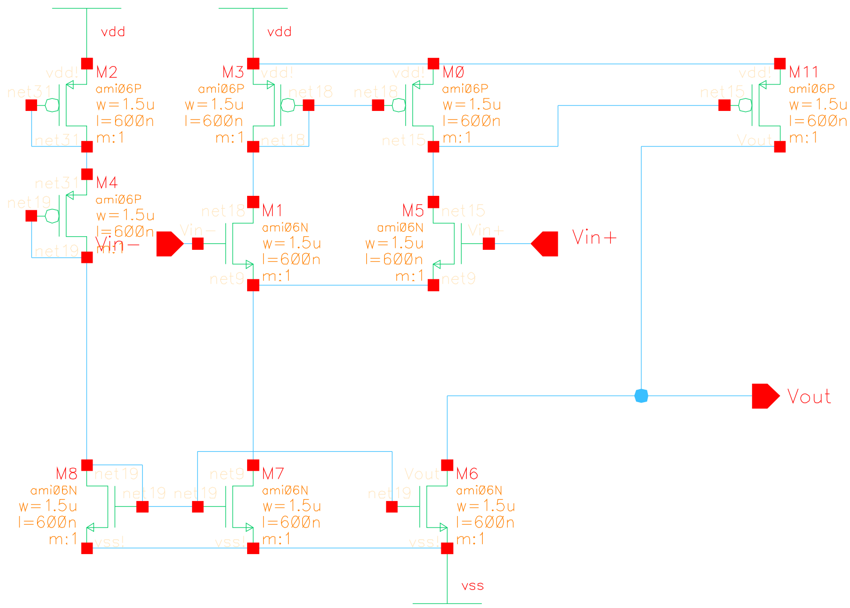
there are 25 in-parallel transmission gates(each gate with a 100k resistor in series).
By switching on or off the gates, we can change the number of in-parallel transmission gates, thus get a variable resistance.



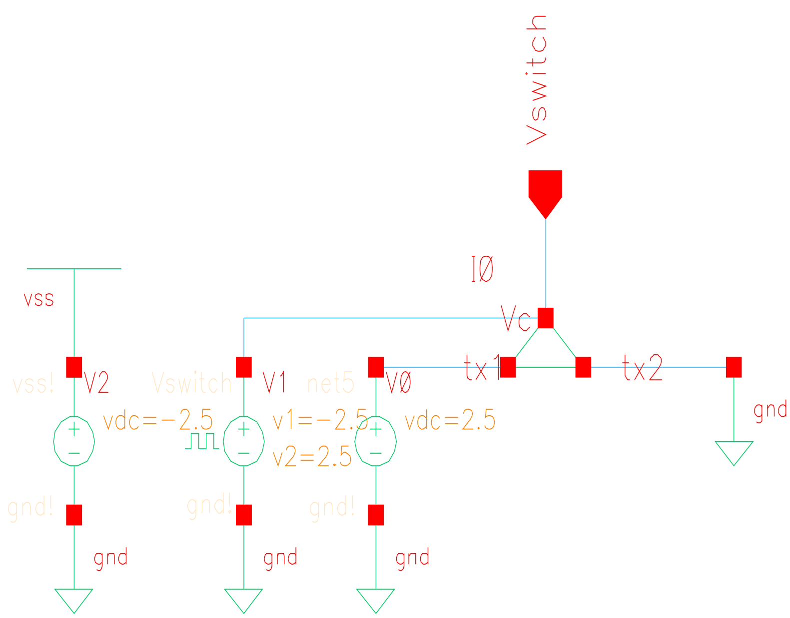
10. Operational amplifier:



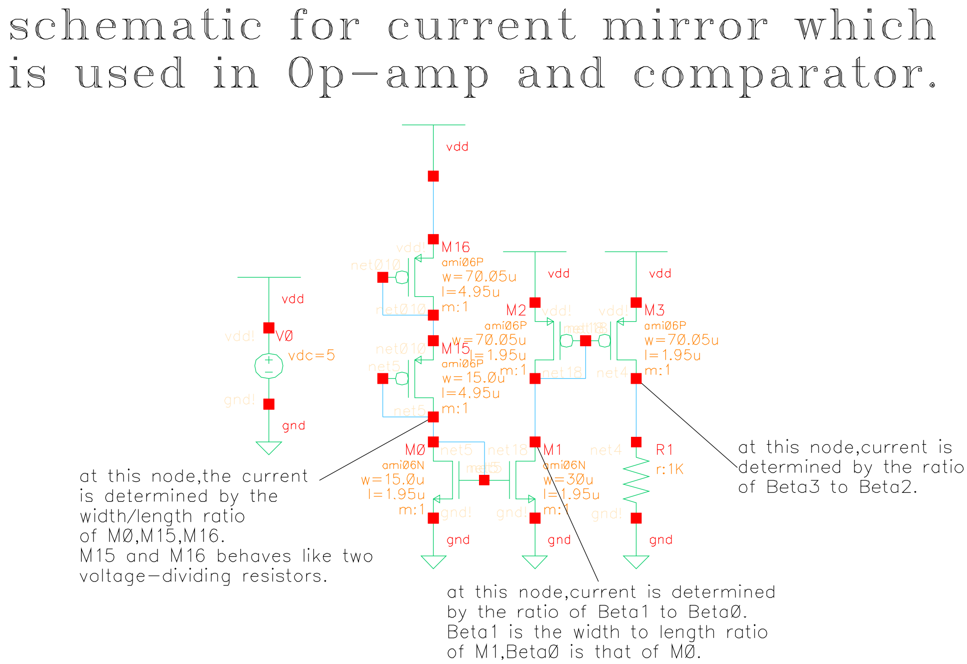
11. Voltage comparator used to produce 25 steps switching signal to implement 25 stage voltage controlled resistor:



12. Transmission gate used as switches to change the number of in−parallel resistors:

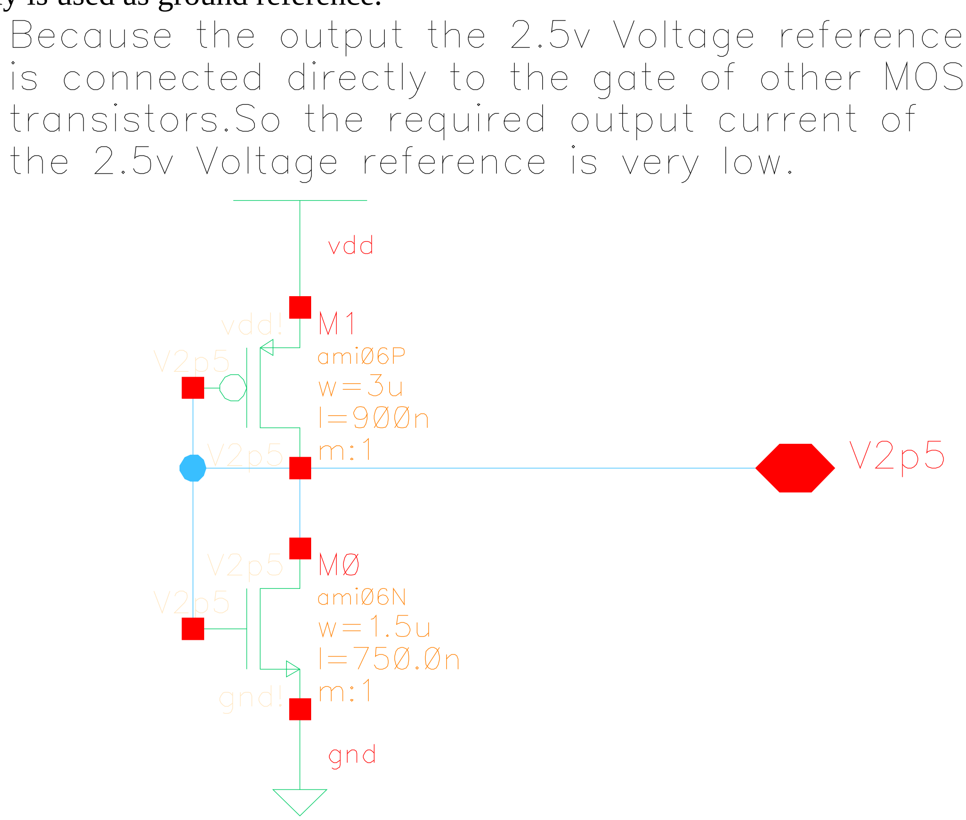


13. Current mirror used in comparator and Op−amp to provide current reference source:



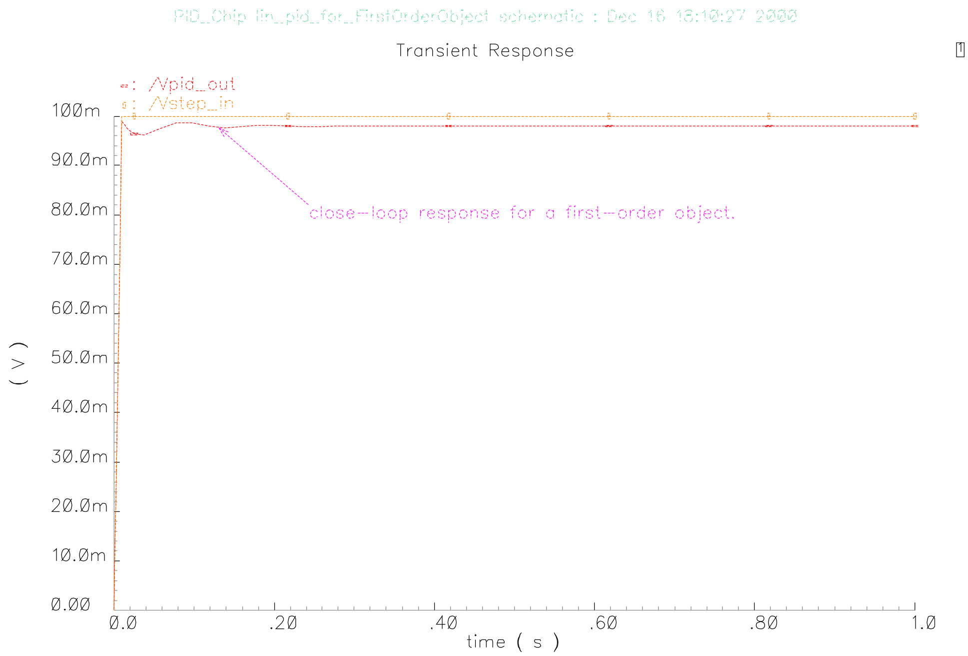
14.voltage divider to output (Vdd−Vss)/2:

the output of the voltage divider can be 0v or 2.5v depending on Vdd−Vss and usually is used as ground reference.

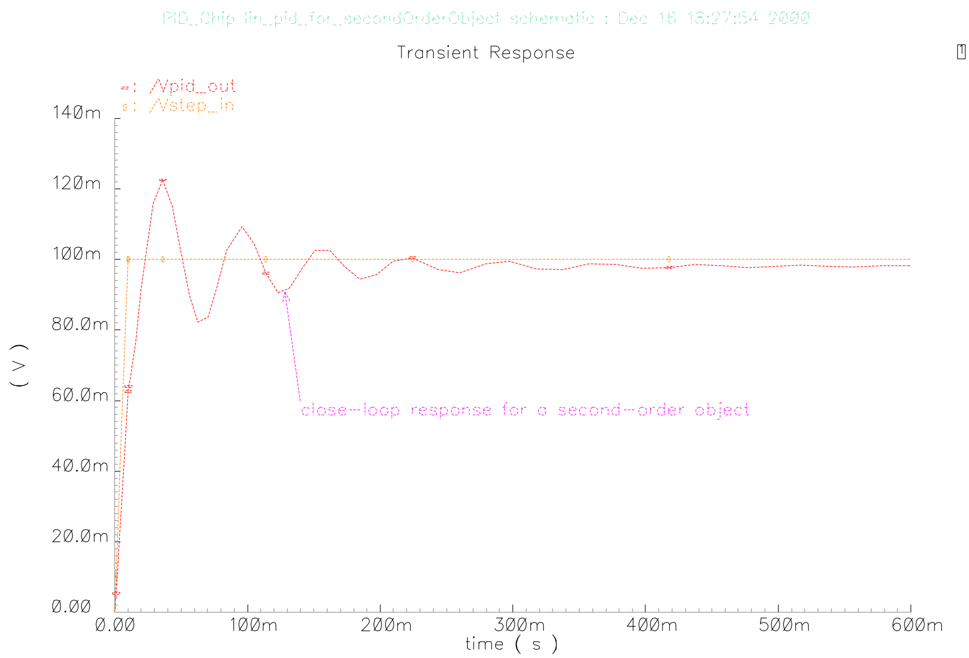


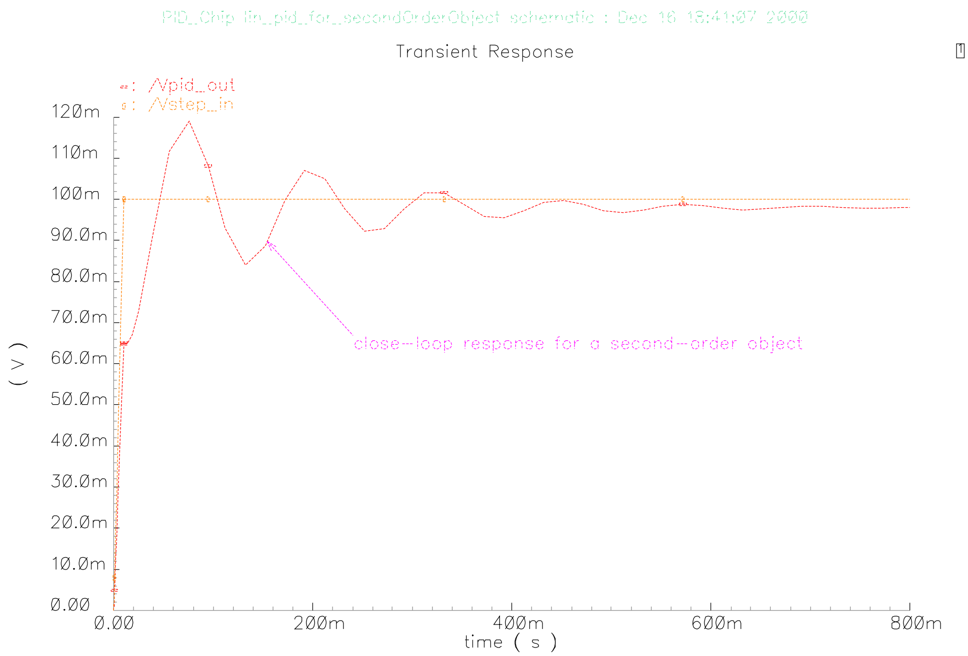
Chapter 3 Simulation

3.1Simulation for close−loop PID controller with a first order object:

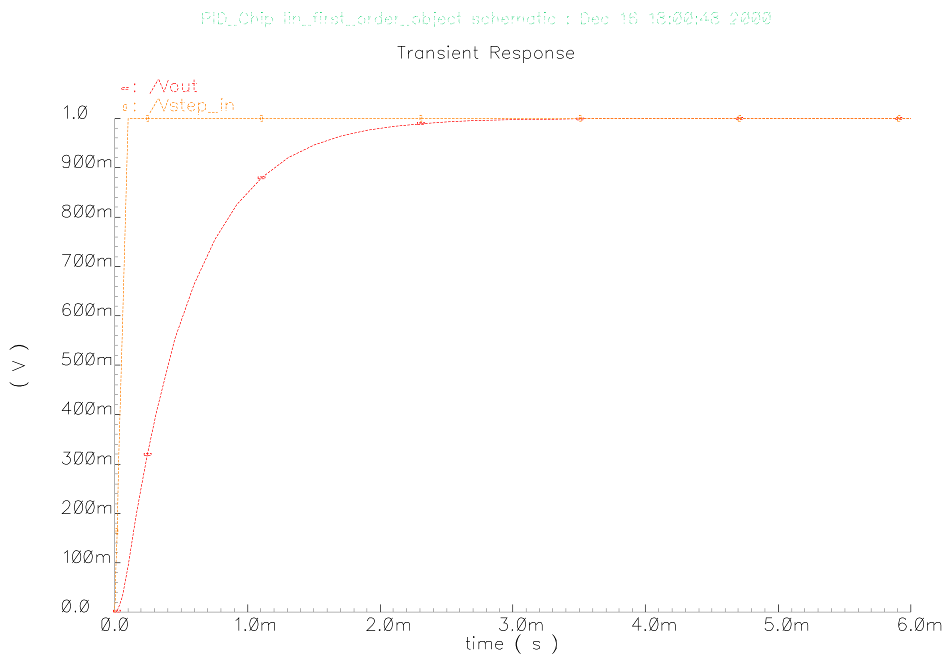


3.2Simulation for close−loop PID controller with a Second order object:

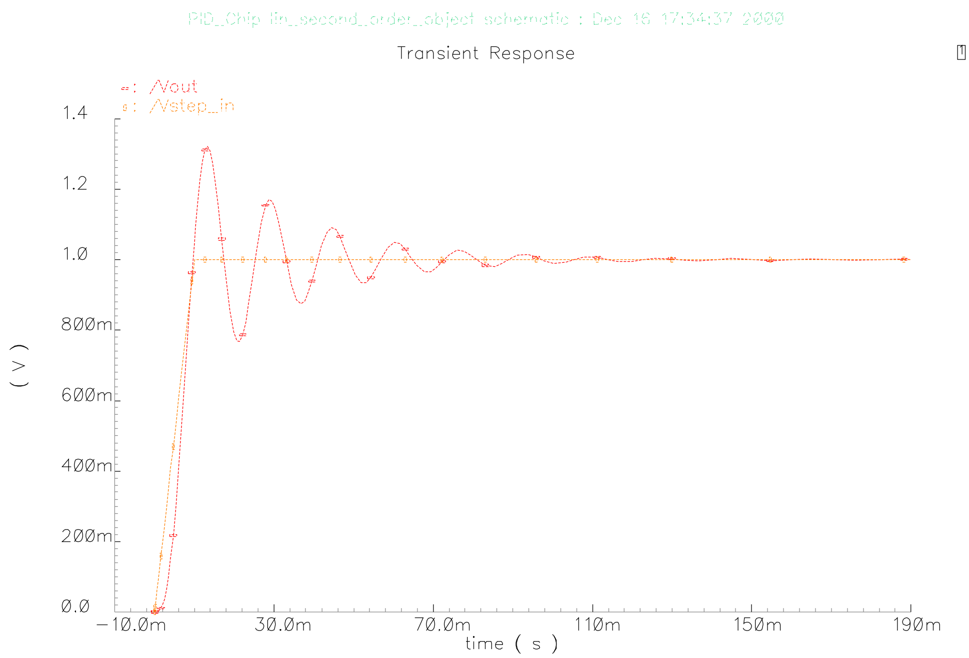



PID_Chip lin_pid_for_secondOrderObject schematic : Dec 16 18:41:07 2000
Transient Response
1
/Vpid_out
/Vstep_in
120m
110m
100m
90.0m
80.0m
70.0m
60.0m
50.0m
40.0m
30.0m
20.0m
10.0m
0.00
(V)
close-loop response for a second-order object
0.00
200m
400m
600m
800m
time (s)

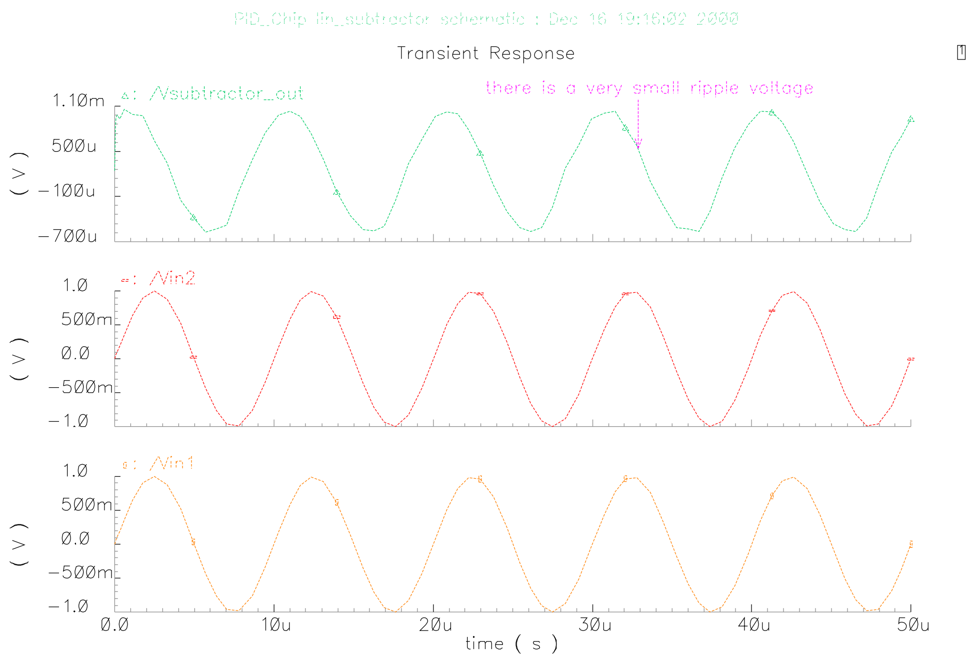
3.3Simulation for a first order object:



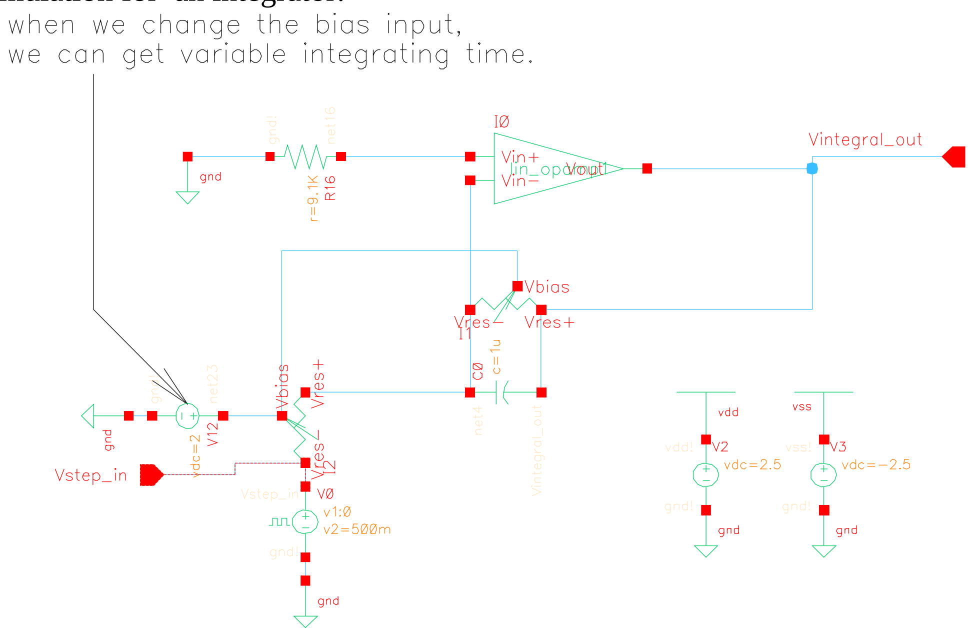
3.4Simulation for a Second order object:

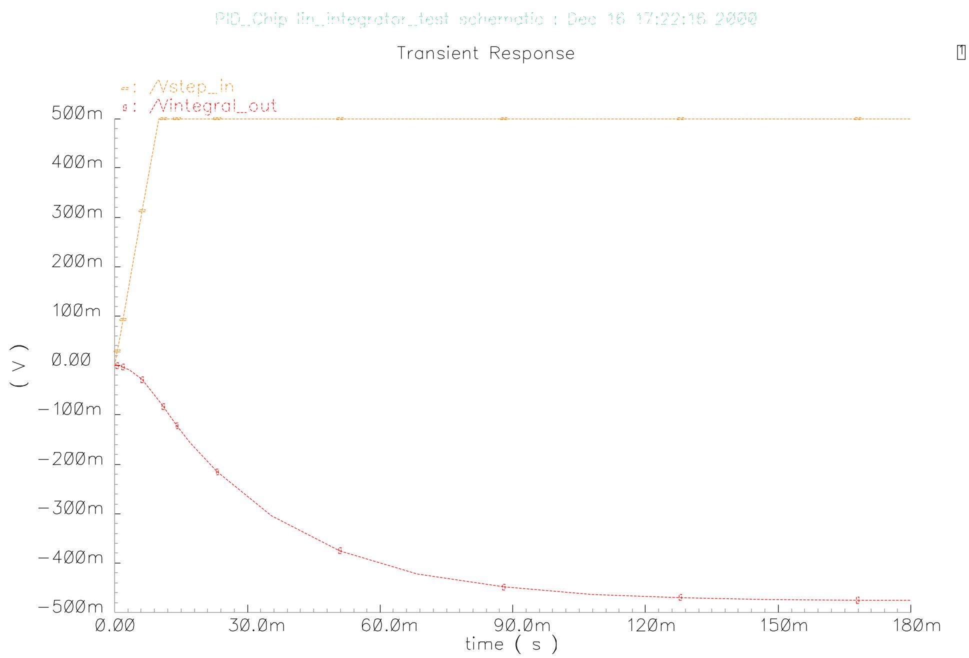


3.5Simulation for a subtractor:



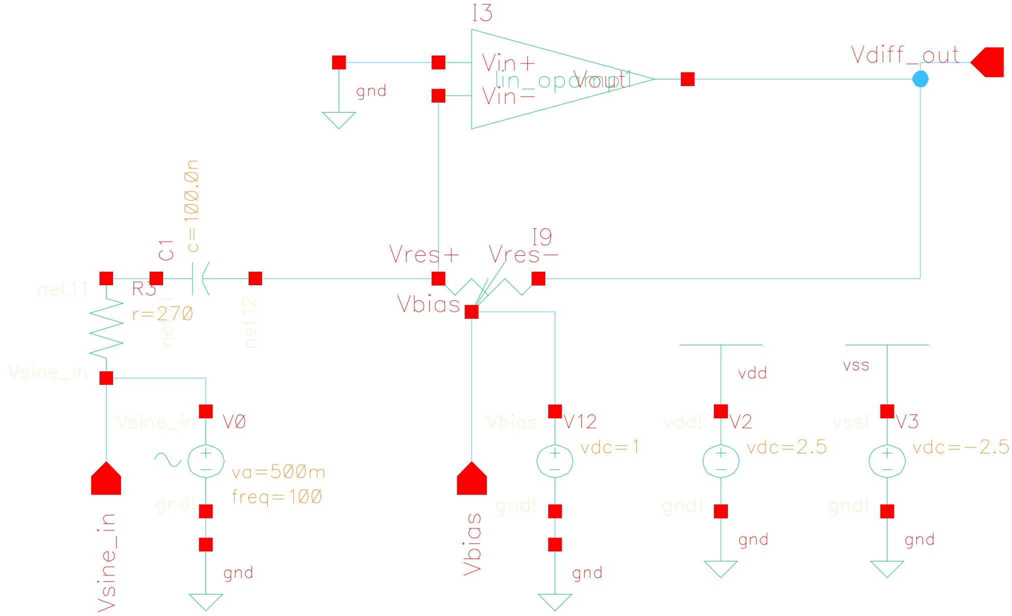
3.6Simulation for an integrator:

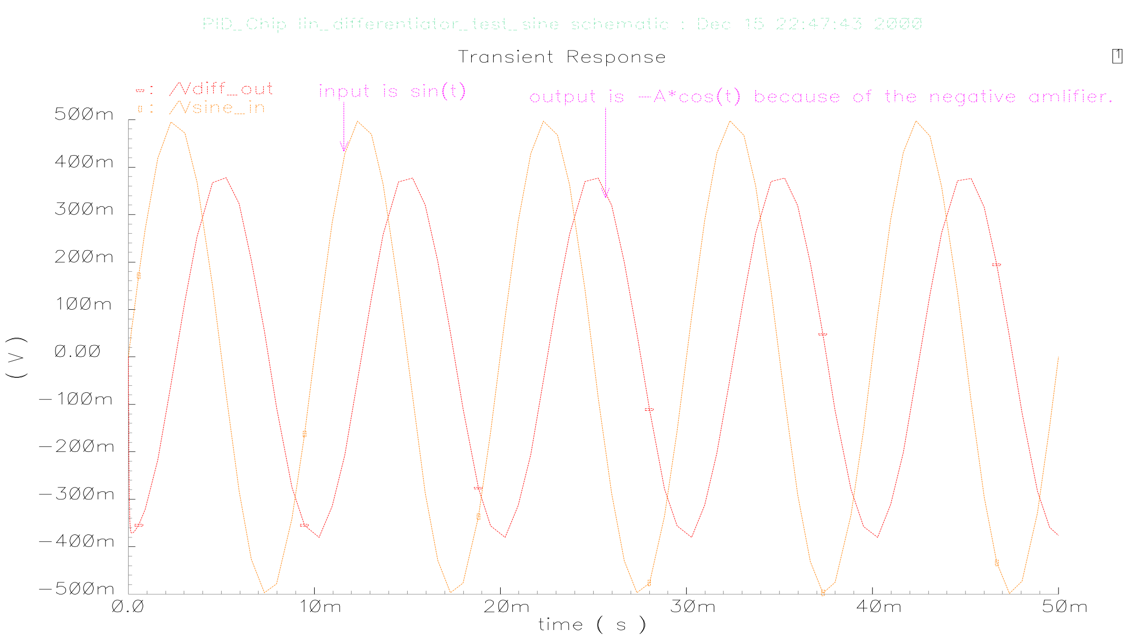


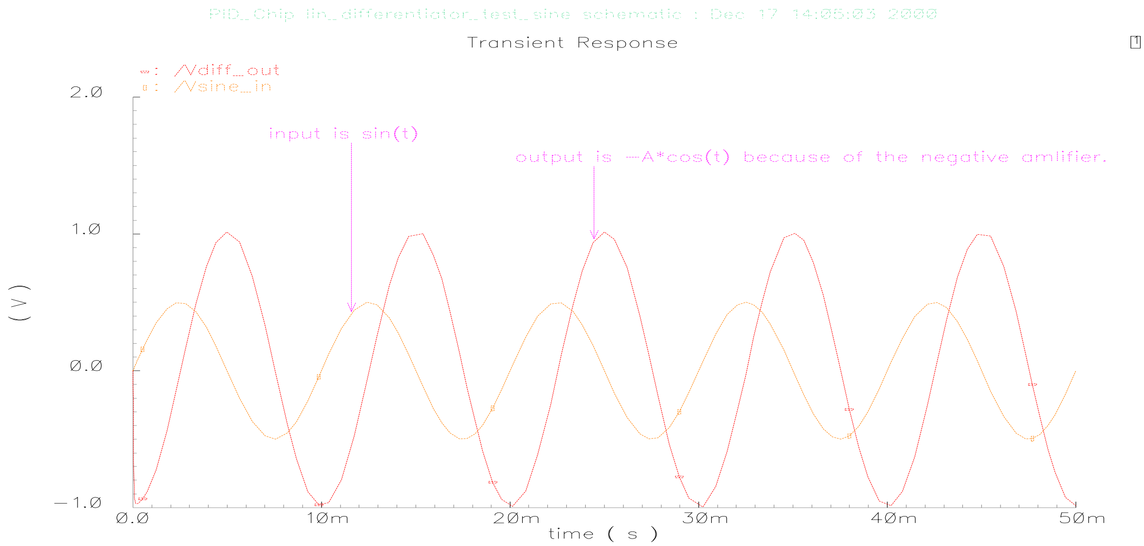


PID_Chip lin_integrator_test schematic : Dec 16 17:22:16 2000
Transient Response
/Vstep_in
/Vintegral_out
500m
400m
300m
200m
100m
0.00
-100m
-200m
-300m
-400m
-500m
(V)
0.00
30.0m
60.0m
90.0m
120m
150m
180m
time (s)

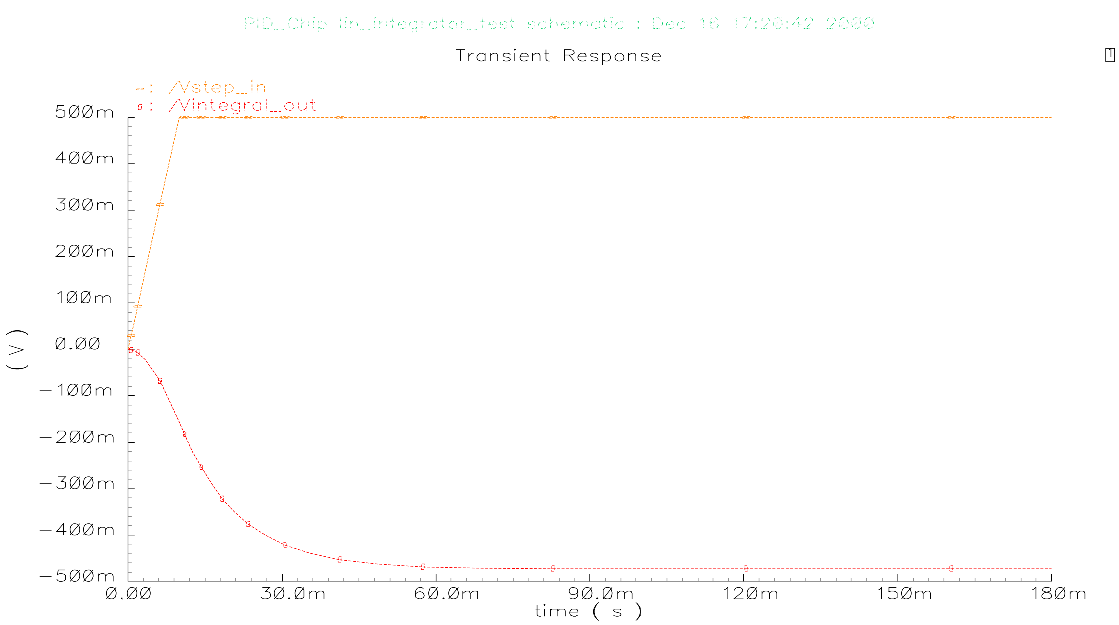
3.7Simulation for a differentiator:





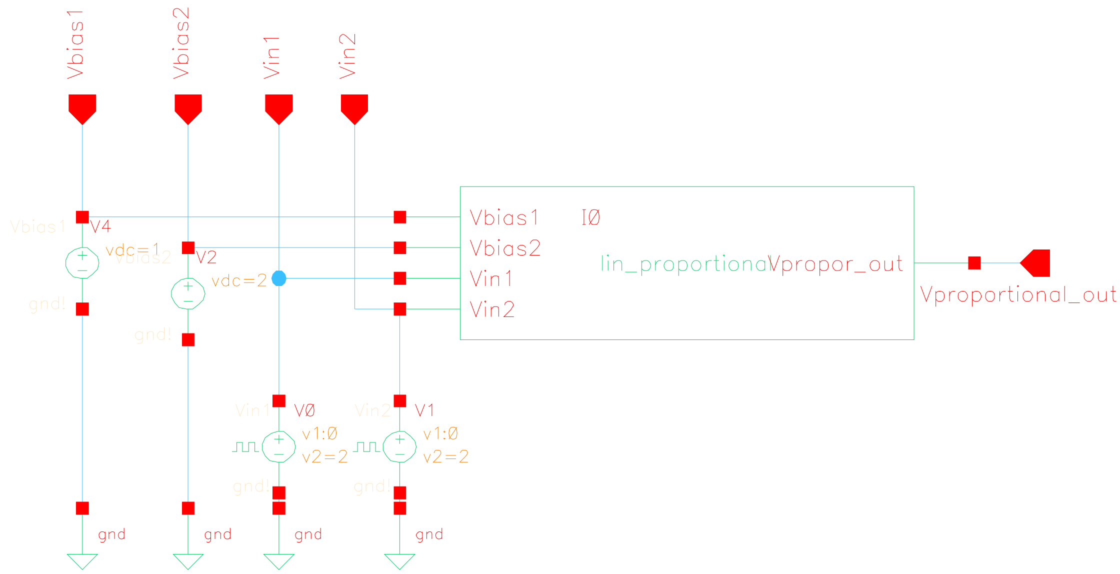


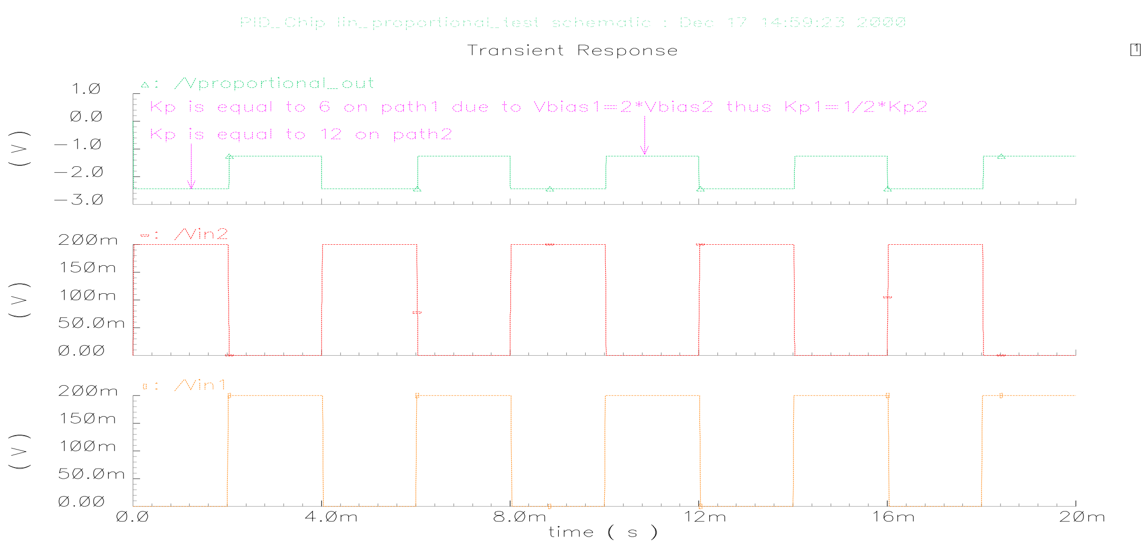
PID_Chip lin_differentiator_test_sine schematic : Dec 17 14:05:03 2000
Transient Response
/Vdiff_out
/Vsine_in
input is sin(t)
output is -A*cos(t) because of the negative amlifier.
2.0
1.0
0.0
-1.0
(V)
0.0
10m
20m
30m
40m
50m
time (s)



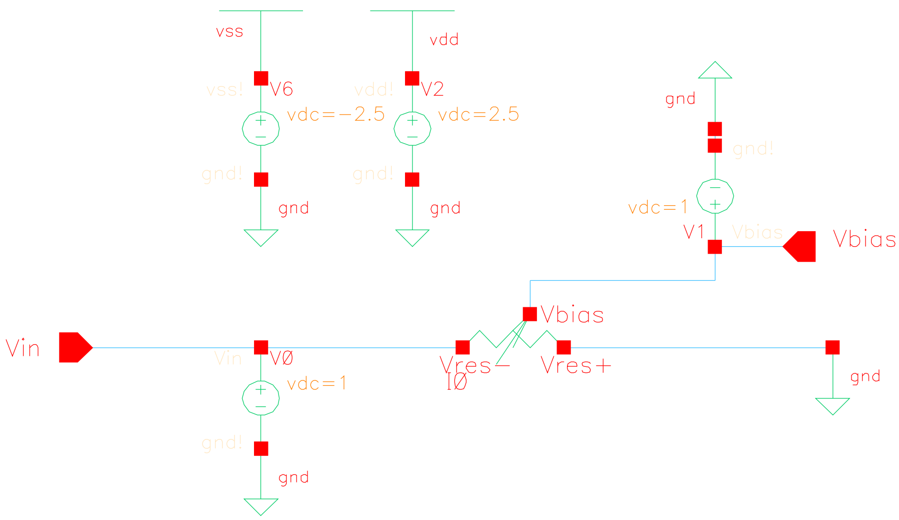
PID_Chip lin_integrator_test schematic : Dec 16 17:20:42 2000
Transient Response
/Vstep_in
/Vintegral_out
500m
400m
300m
200m
100m
0.00
-100m
-200m
-300m
-400m
-500m
(V)
0.00
30.0m
60.0m
90.0m
120m
150m
180m
time (s)

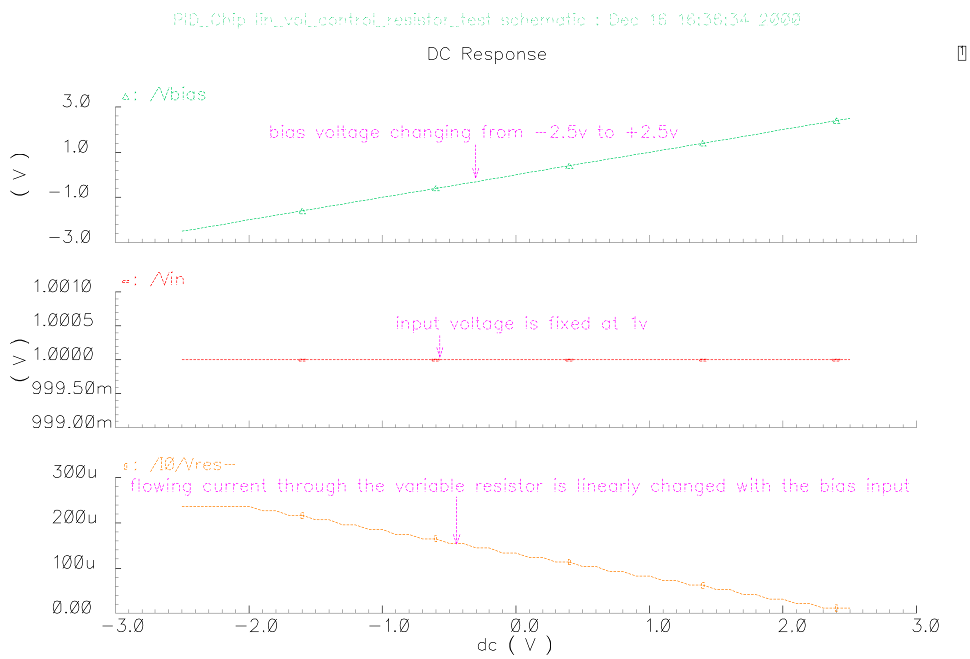
3.8Simulation for a proportional part:





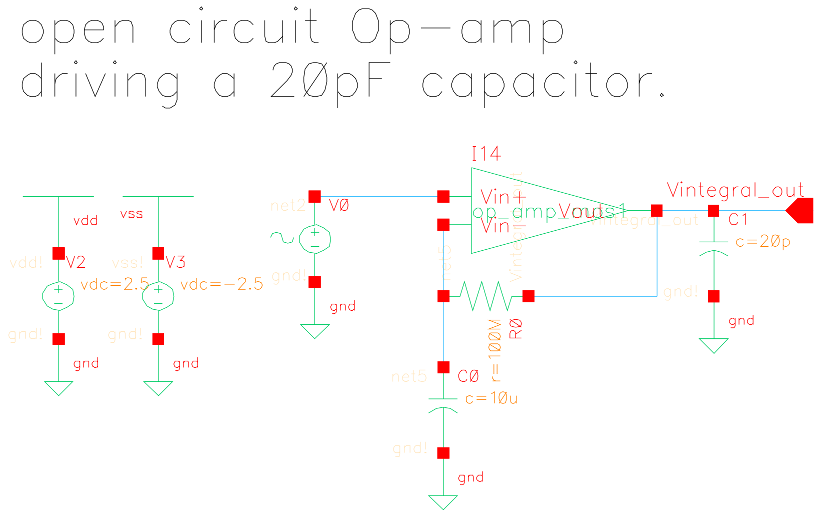
3.9Simulation for a VOLTAGE−CONTROLLED resistor:

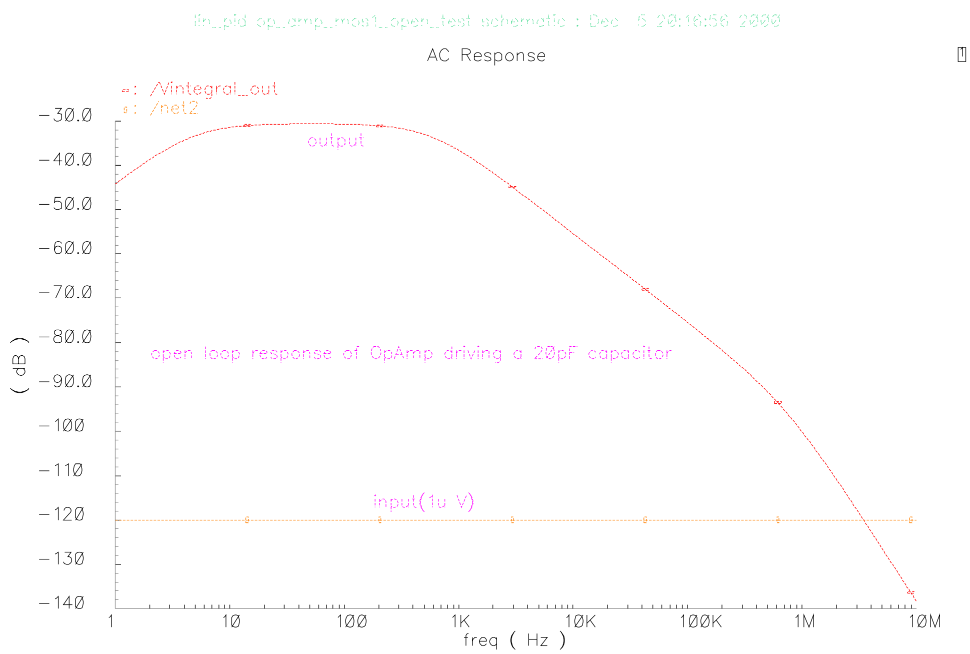


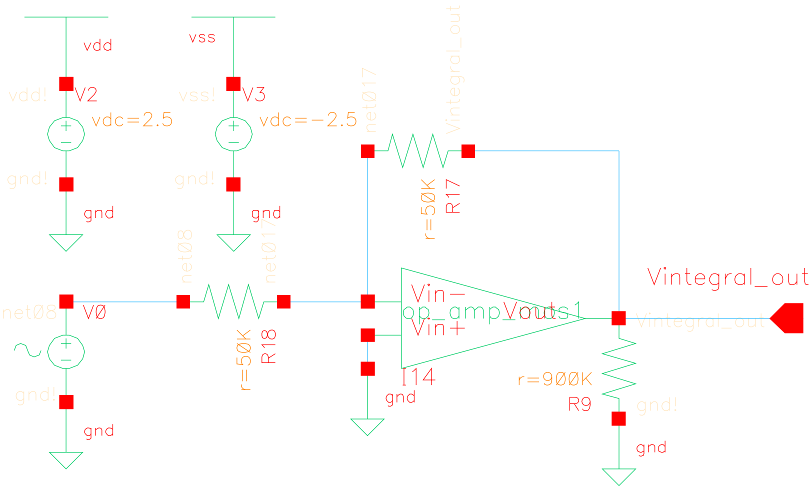


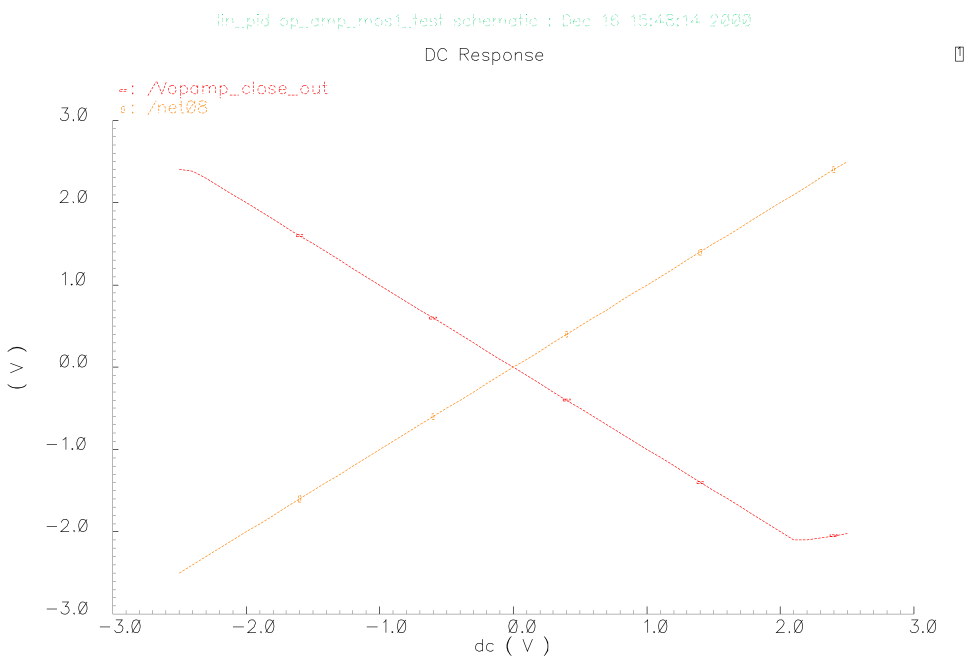
PID_Chip lin_vol_control_resistor_test schematic : Dec 16 16:36:34 2000
DC Response
/Vbias
bias voltage changing from -2.5v to +2.5v
3.0
1.0
-1.0
-3.0
(V)
/Vin
input voltage is fixed at 1v
1.0010
1.0005
1.0000
999.50m
999.00m
(V)
/I0/Vres--
flowing current through the variable resistor is linearly changed with the bias input
300u
200u
100u
0.00
-3.0
-2.0
-1.0
0.0
1.0
2.0
3.0
dc (V)

3.10Simulation for an operational amplifier:

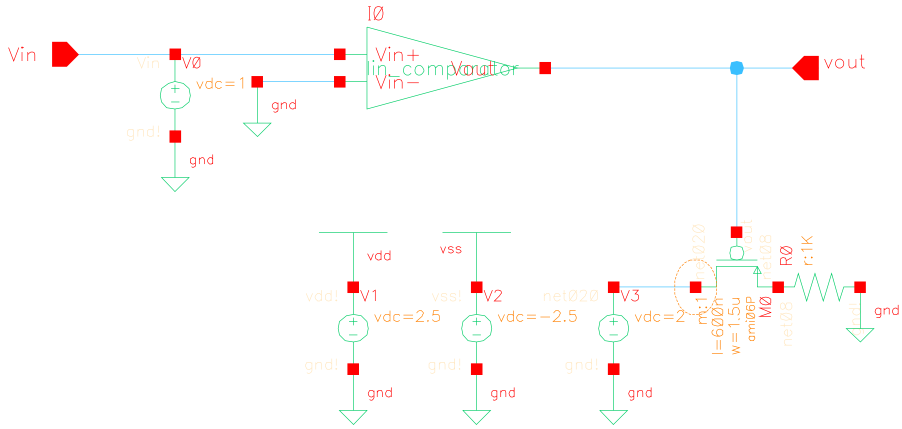


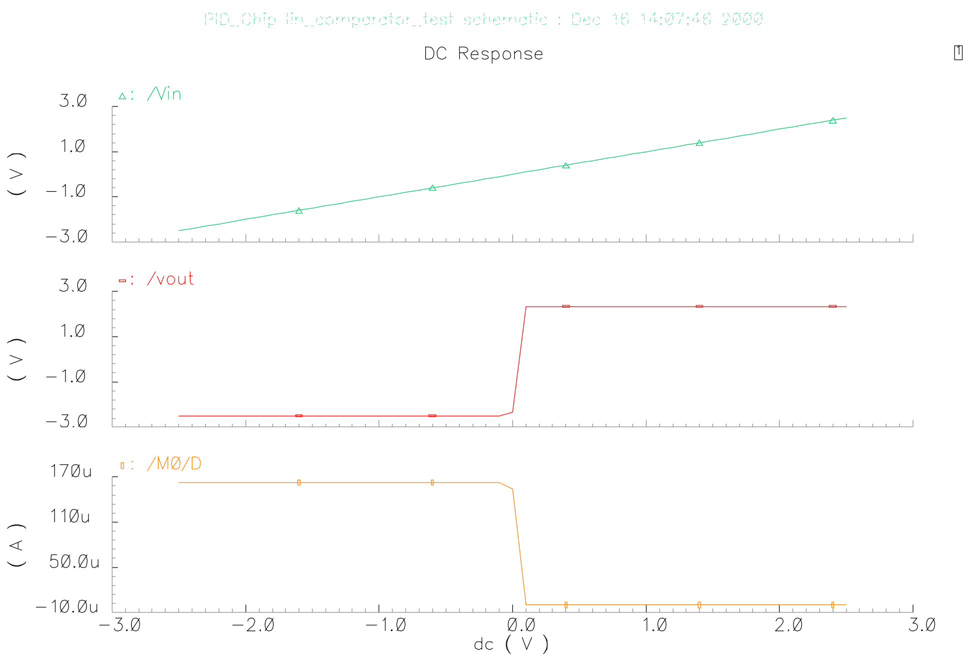



vdd
vss
vdd!
V2
vss!
V3
vdc=2.5
vdc=-2.5
net017
Vintegral_out
gnd!
gnd
r=50K
R17
net08
Vintegral_out
V0
Vin−
op_ampVouts1
Vin+
r=50K
R18
I14
gnd
r=900K
R9
gnd!
gnd

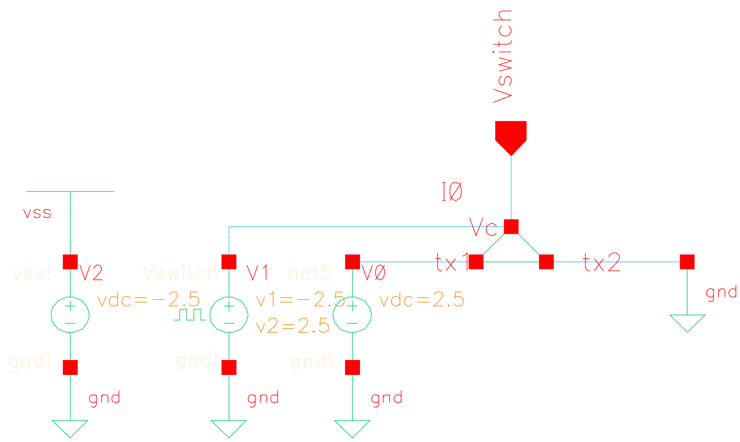

lin_pid op_amp_mos1_test schematic : Dec 16 15:48:14 2000
DC Response
/Vopamp_close_out
/net08
3.0
2.0
1.0
0.0
−1.0
−2.0
−3.0
(V)
−3.0
−2.0
−1.0
0.0
1.0
2.0
3.0
dc (V)

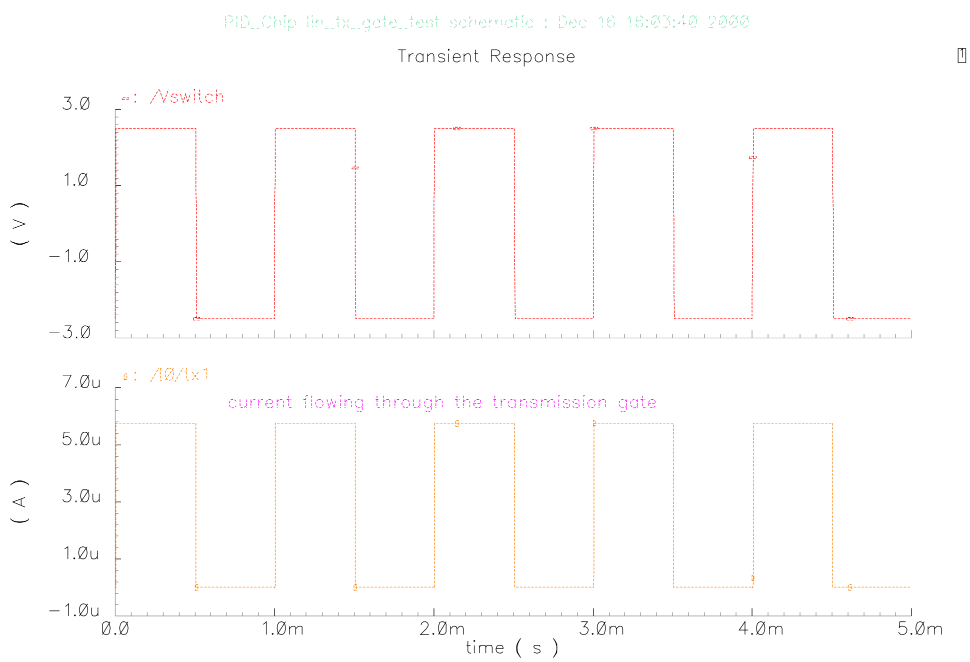
3.11Simulation for a voltage comparator:



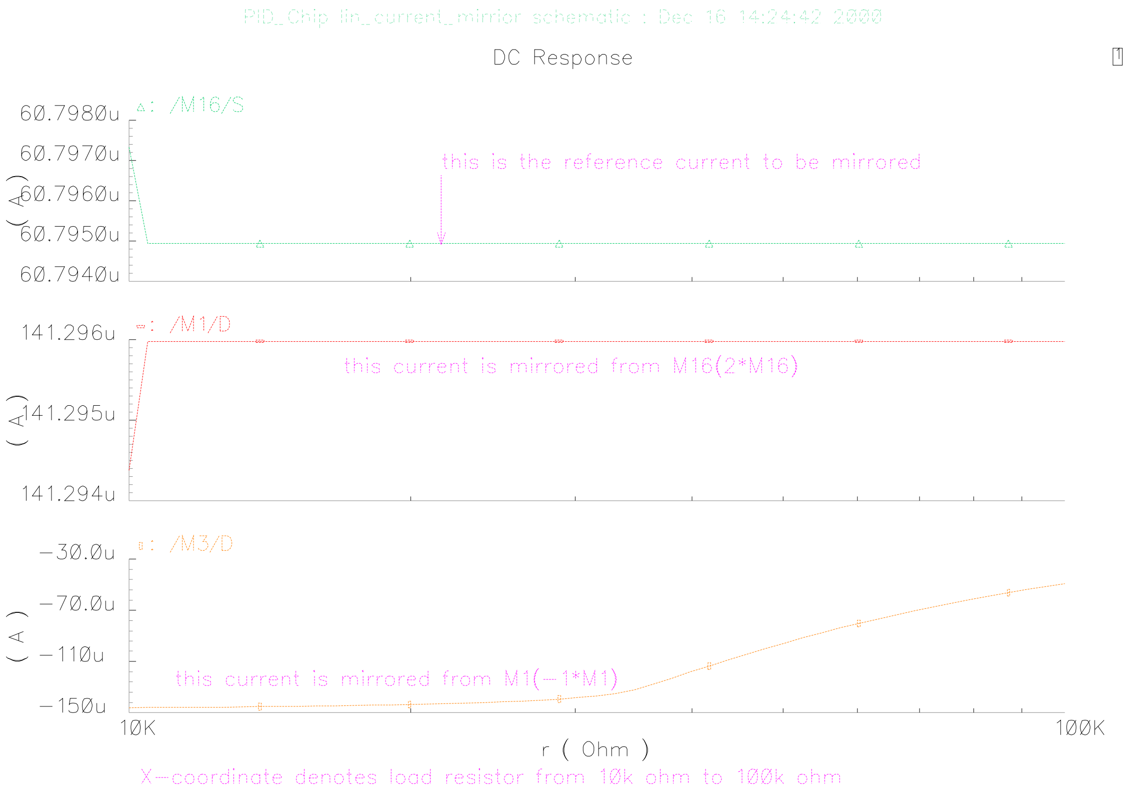


3.12Simulation for a transmission gate:

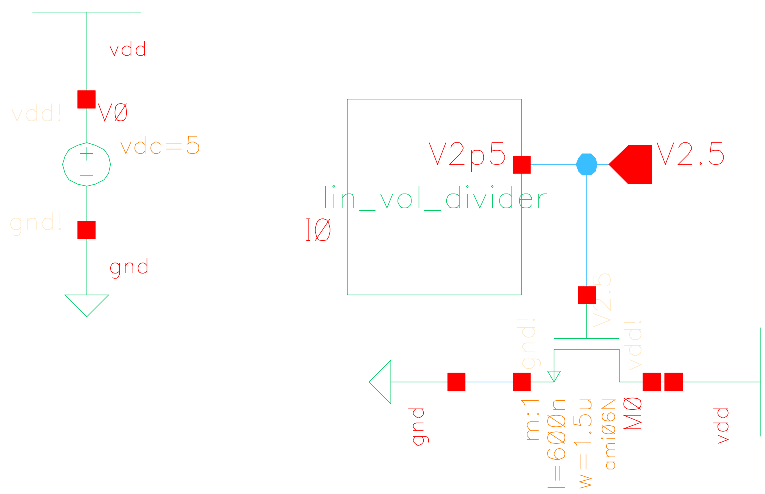


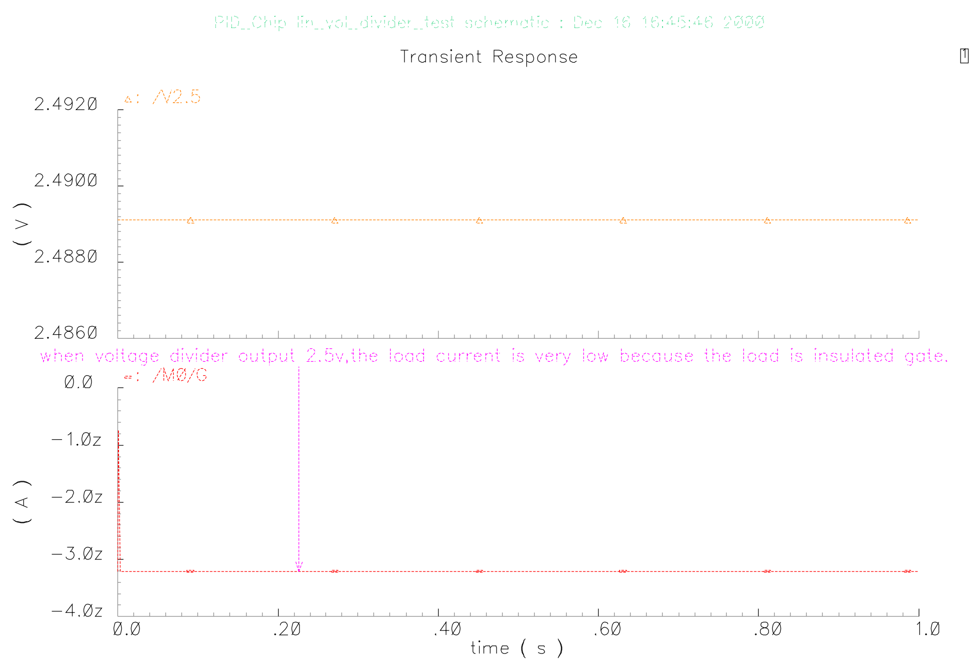


3.13Simulation for a current mirror:



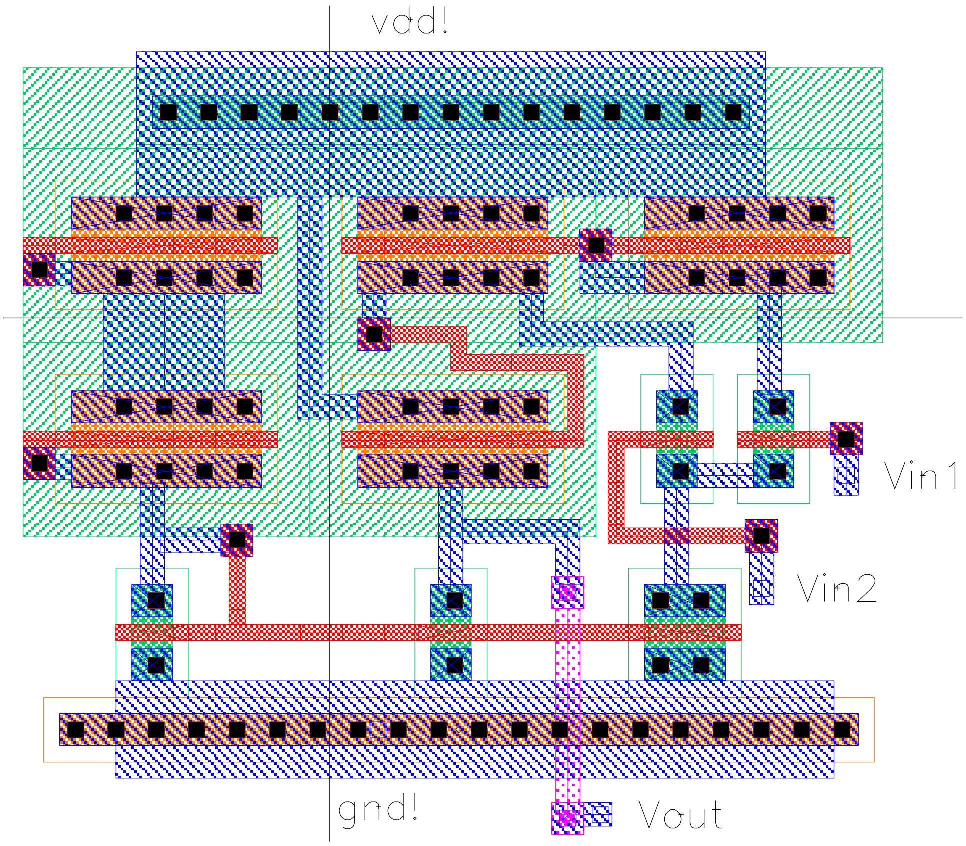
3.14Simulation for a voltage divider:




PID_Chip lin_vol_divider_test schematic : Dec 16 16:45:46 2000
Transient Response
▵: /V2.5
2.4920
2.4900
(V)
2.4880
2.4860
when voltage divider output 2.5v,the load current is very low because the load is insulated gate.
∗: /M0/G
0.0
−1.0z
(A)
−2.0z
−3.0z
−4.0z
0.0
.20
.40
.60
.80
1.0
time (s)

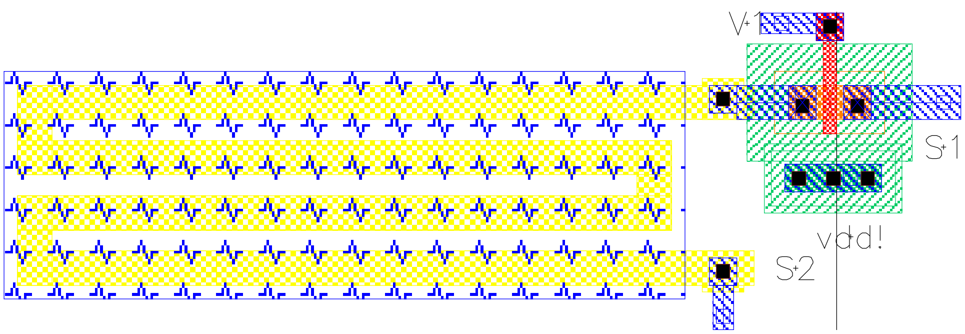
Chapter 4 Layout

4.1 Comparator layout



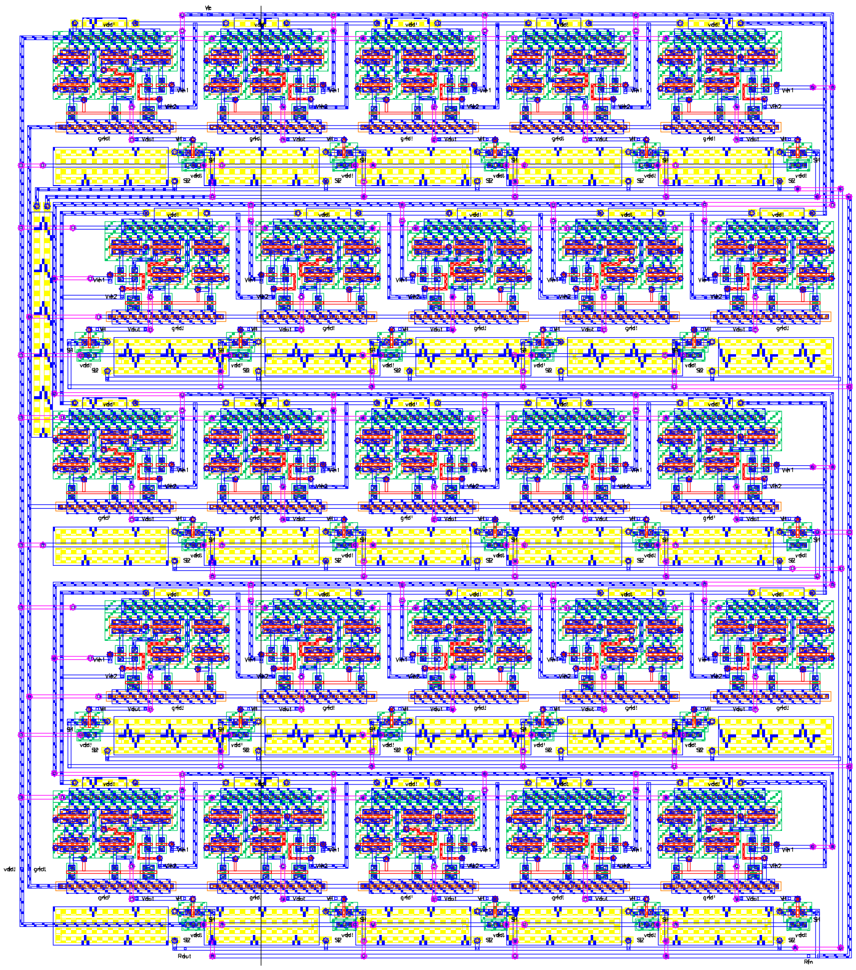
There are 5 pmos and 5 nmos in this comparetor and the size of each one is listed blew: pmos 7.05x0.6um; nmos one of them is 3x0.6 with anothers 1.5x0.6um. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole comparator is 35.7x31.05um. There are 5 pins in it, vdd!, gnd!, Vout, Vin1 and Vin2.

4.2 Transgate layout



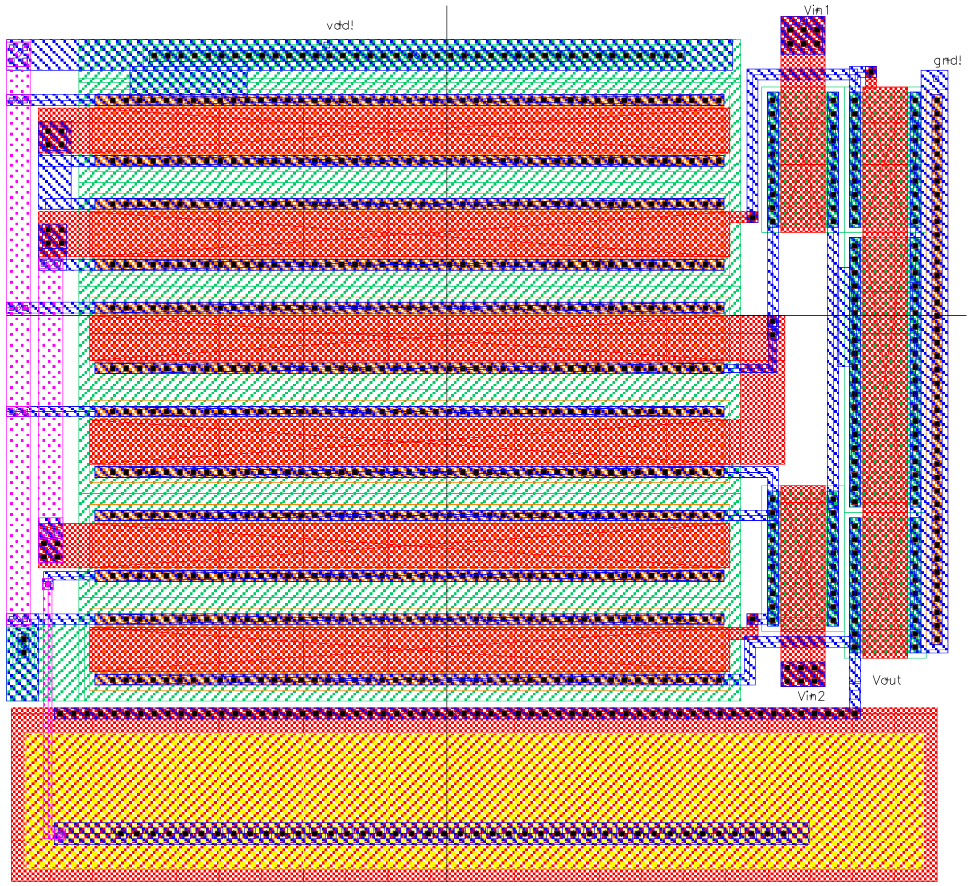
There one pmos with size of 1.5x0.6um and one 100K ohms resistorin this transgate.By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole transgate is 39x13.95um. There are 5 pins in it, vdd!, gnd!, V1, S1 and S2.

4.3 Virable resistor layout



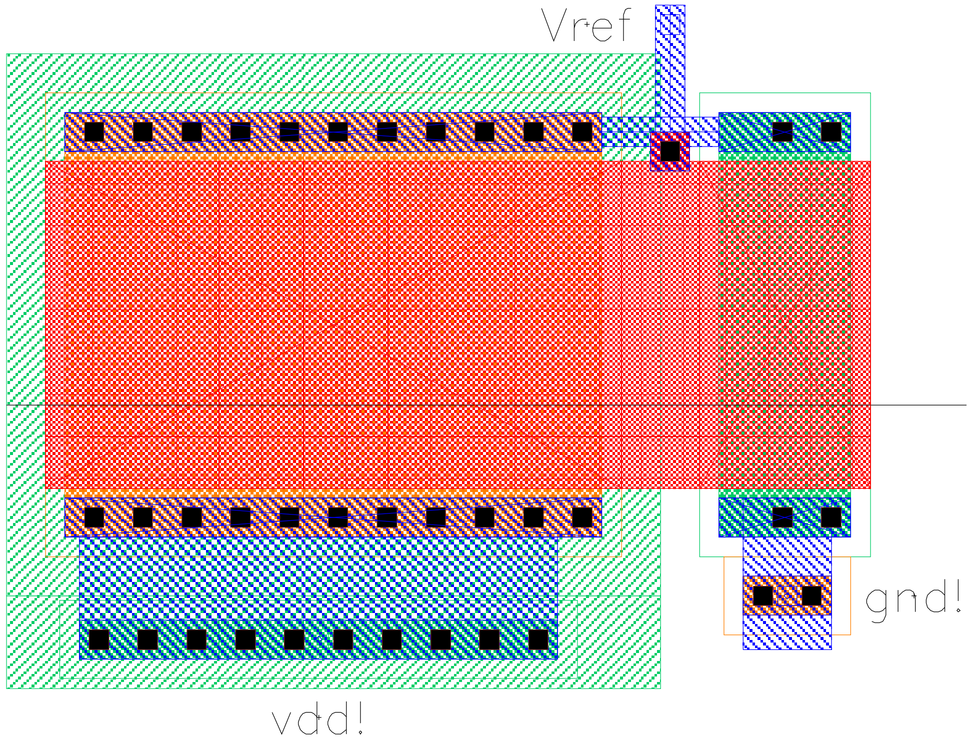
There are 25 comparators, 25 transgates, 25 10K ohms resistors and 0ne 100K ohms resistor in this vriable resistor. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole virable resistor is 216.45x247.5um. There are 5 pins in it, vdd!, gnd!, Vc, Rin and Rout.

4.4 Operation amplifier layout



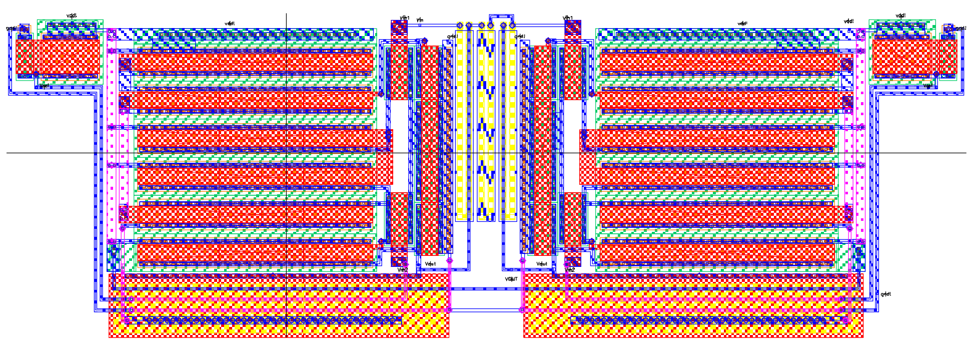
There are 6 pmos ,5 nmos and one 1.42pf capacitor in this operation amplifier and the size of each one is listed blew: pmos 70x5um; nmos one of them is 30x5 with anothers 15x5um. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole operation amplifier is 106.8x97.35um. There are 5 pins in it, vdd!, gnd!, Vout, Vin1 and Vin2.

4.5 Voltage referance layout



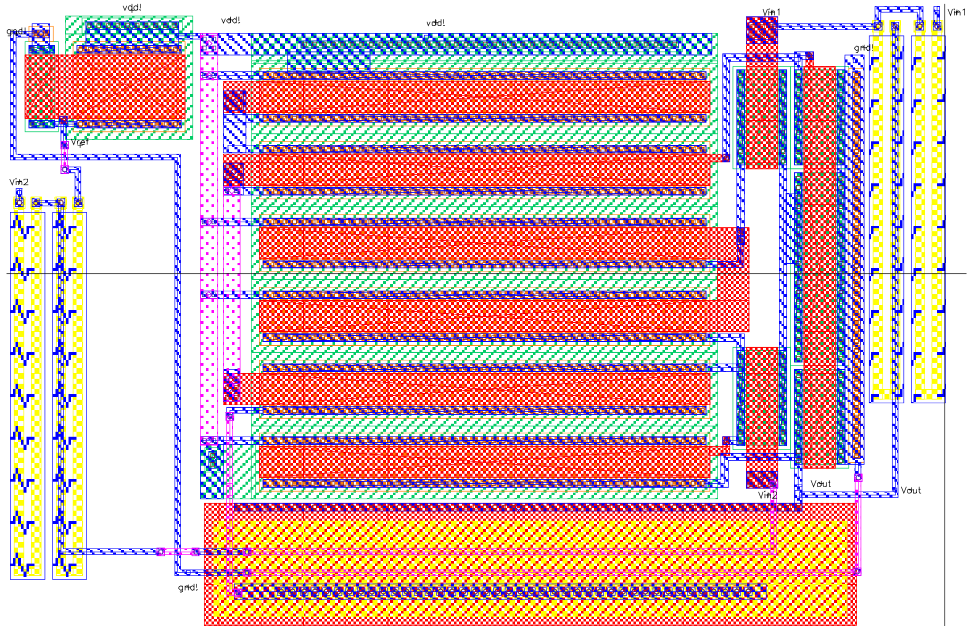
There are 1 pmos, 1 nmos this voltage referance and the size of each one is listed blew: pmos 16.5x10um; nmos 5x10um. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole voltage referance is 29.55x22.55um. There are 3 pins in it, vdd!, gnd! and Vref.

4.6 Voltage divider layout



There are 2 operation amplifier, 2 voltage referance and three 100K ohms resistors in this voltage divider. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole voltage divider is 291.6x99um. There are 4 pins in it, vdd!, gnd!, Vin and Vout.

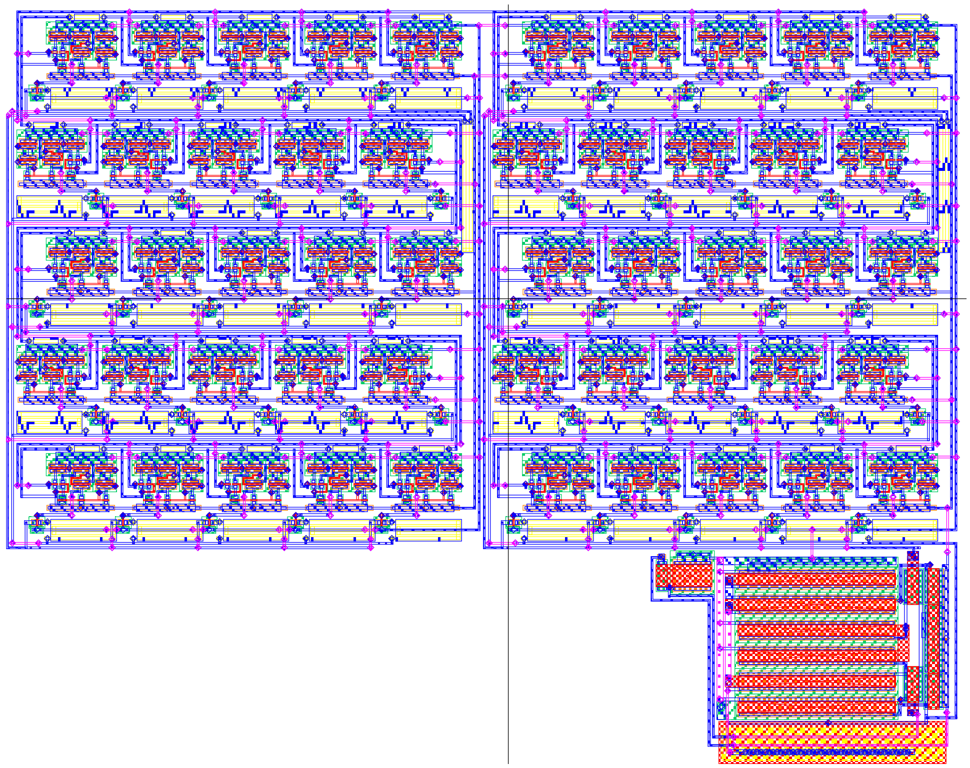
4.7 Summation block layout



There are 1 operation amplifier, 1 voltage referance and four 100K ohms resistors in this summation block. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole summation block is 152.7x97.2um. There are 5 pins in it, vdd!, gnd!, Vin1,Vin2 and Vout.

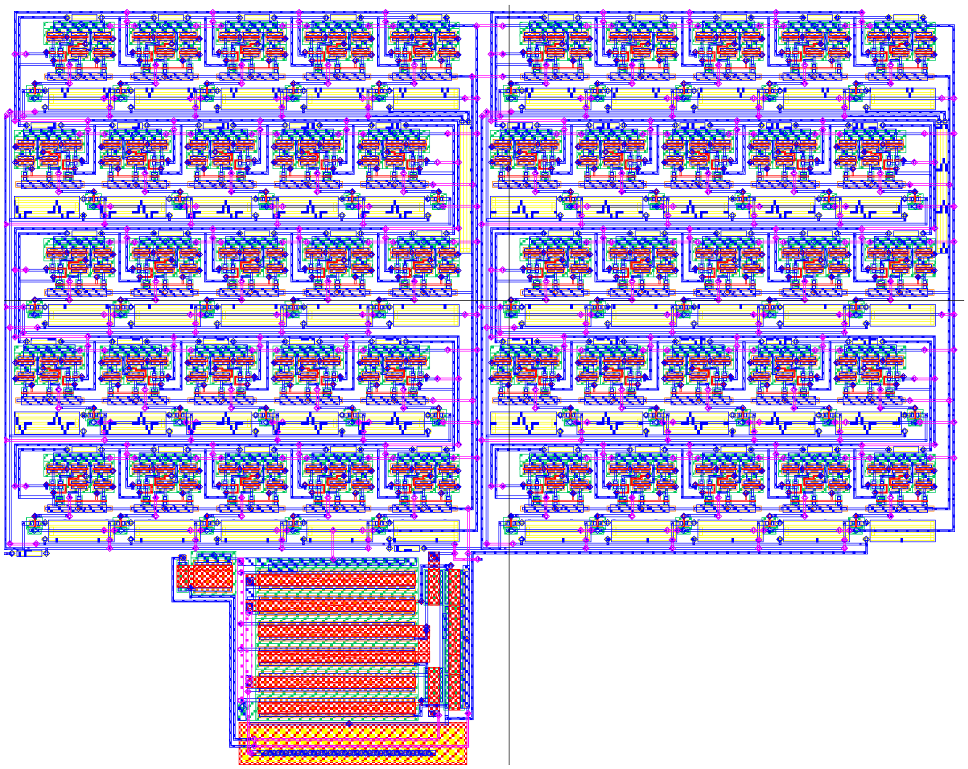
4.8 Derivative part layout

There are 1 operation amplifier, 1 voltage referance and 2 virable resistors in this derivative part. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole derivative part is 436.05x344.7um. There are 7 pins in it, vdd!, gnd!, Vi3,Vc3, Vo3 Vd11 and Vd12.



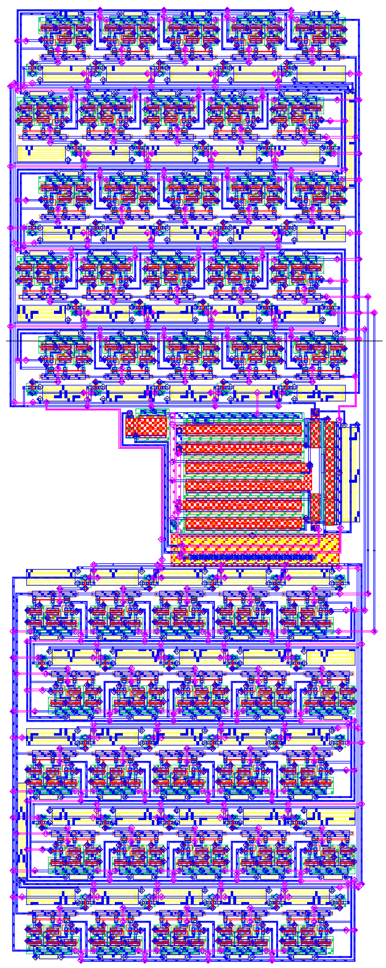
4.9 Integral part layout

There are 1 operation amplifier, 1 voltage referance, 2 virable resistors and two 10K ohms resistors in this integral part. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole integral part is 435.15x344.7um. There are 6 pins in it, vdd!, gnd!, Vi2,Vc2, Vo2 and Vi11.



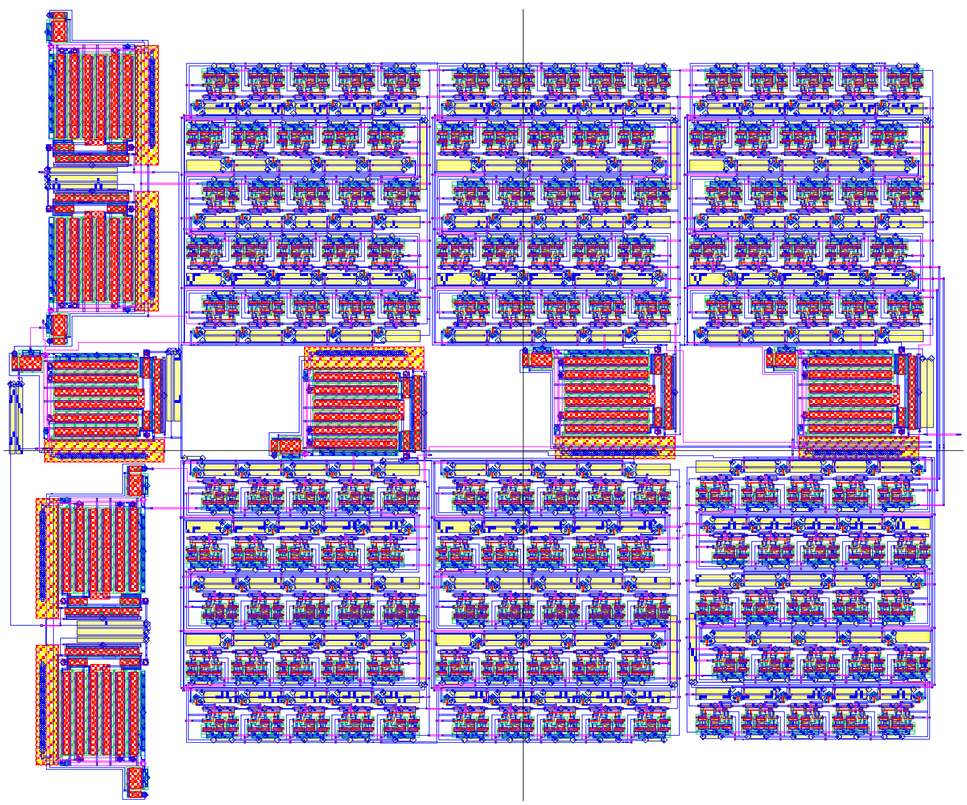
4.10 Propotional part layout

There are 1 operation amplifier, 1 voltage referance, 2 virable resistors and one 200K ohms resistor in this proportional part. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole proportional part is 227.25x587.6um. There are 6 pins in it, vdd!, gnd!, Vpin−1,Vpin−2,Vc1 and Vpout.



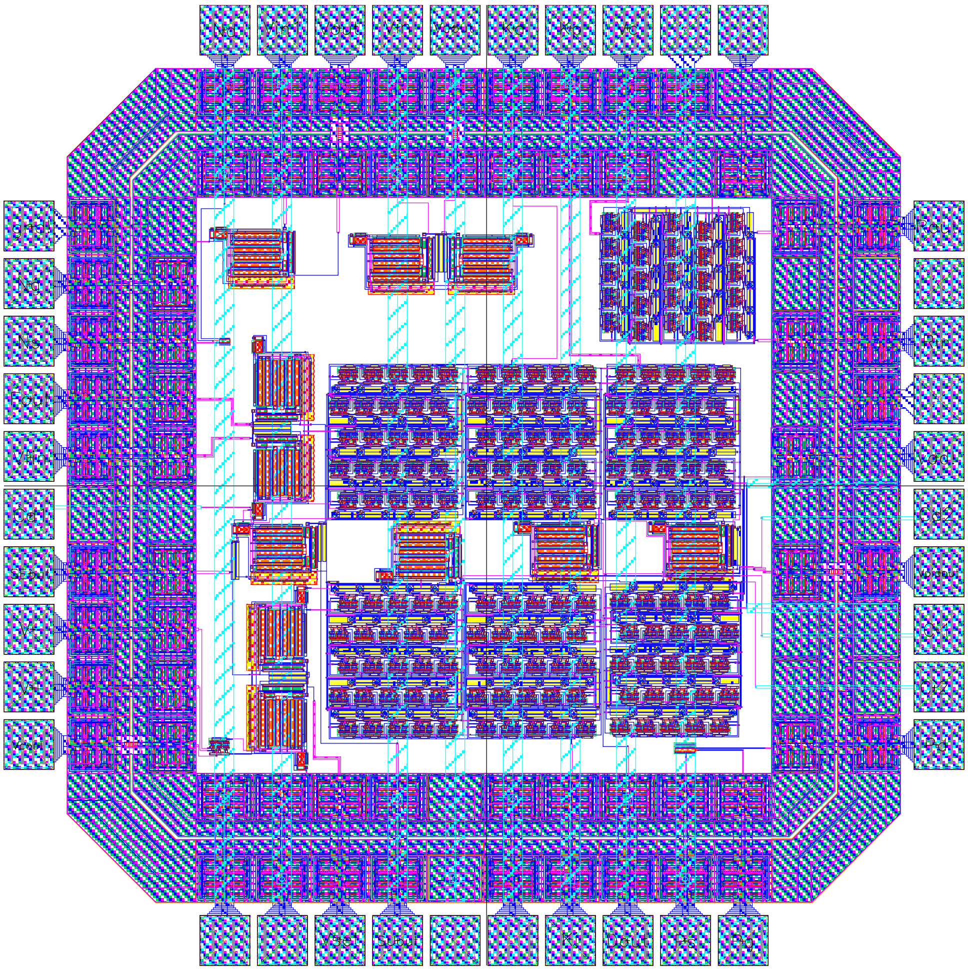
4.11 PID controller layout

There are 2 voltage dividers, 1 summation block, 1 derivative part, 1 integral part and 1 propotional part. in this pid controller. By trying to keep everything to fufill the smallest requirmet of layout rule, the size of whole pid controller is 826.05x681.6um. There are 16 pins in it, vdd!, gnd!, Vfin, Vset, Fout, Seout, Suout, Cd1, Cd2, Kd, Dout, Ki, Ci1, Ci2, Kp and Vpidout.



4.12 PID chip top layout

By trying to put more indepent devices as we can, there are 1pid controller, 1 voltage dividers, 1 operation amplifier, 1 comparetor, 1 virable resistor, 1 pmos, 1 nmos and 1 set of padset in this chip with the size of whole chip is 1.5x1.5mm. There are 32 pins in it, vdd!, gnd!, Vfin, Vset, Fout, Seout, Suout, Cd1, Cd2, Kd, Dout, Ki, Ci1, Ci2, Kp, Vpidout, Vc, Rin, Rout, Vdout, Vin, Vin1, Vout, Nd, Ng, Ns, V−, V+, Vcout, Pd, Pg and Ps.



Chapter 5 Verification

Each component of this chip has passed the DRC verification without any errors except the 45 degree parts of padset. Each component of this chip up to the top level has passed the LVS verification, everything is matched between schematic and extracted. The LVS report of the whole chip please refer to appendix C.

Chapter 7 Conclusion

Under the instrction of Professor David Kotecki, we utilized Cadence build the PID controller and tested it in first and second controlled object. It passed the DRC and LVS verification. The performance of this controller can be tesitified through the simulation results. This chip will be tested as an temperature controller in ECE 548.

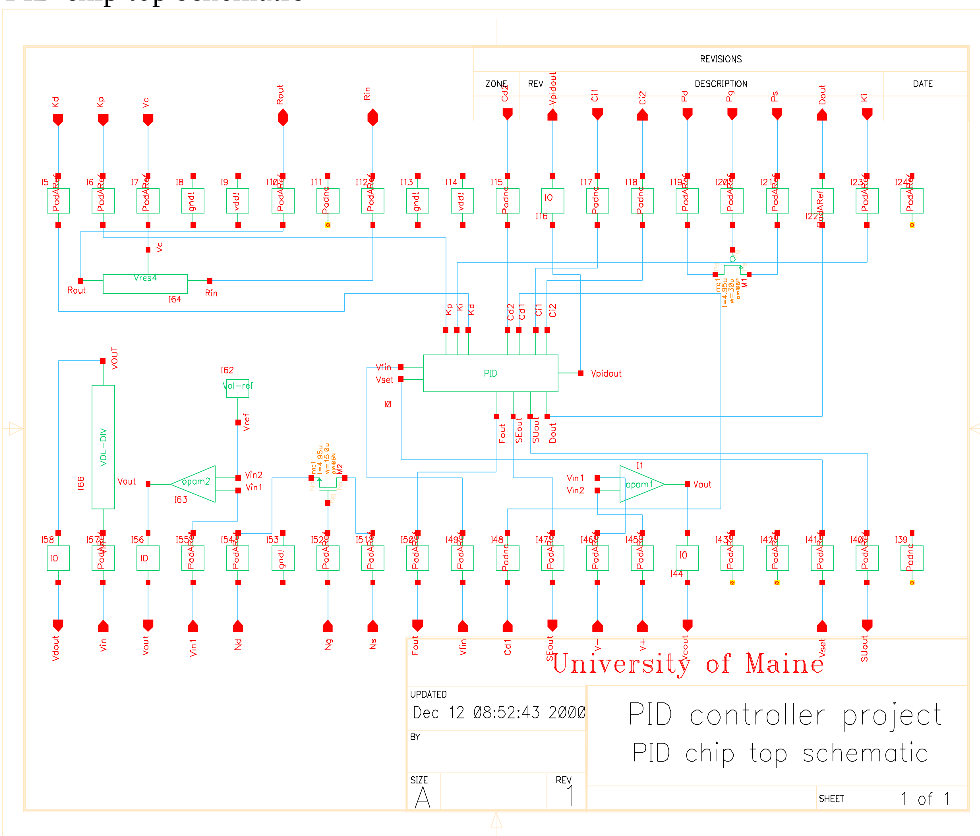
Appendix A: Schematics

Introduction

In this appendix, we briefly include each schematic of this PID controller. It will be divided into two parts, one is schematics break down parts of PID chip, another is schematics for testing circuits.

A.1 PID chip

A1.1 PID chip top schematic



PID: The PID controller.

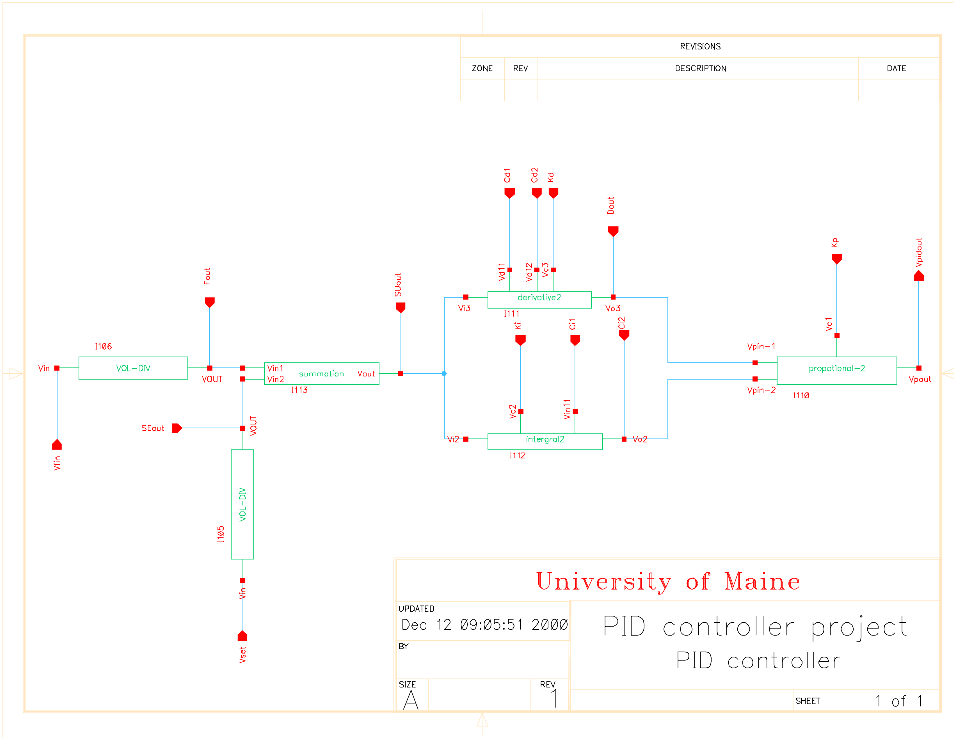
Opam1: Comparator which is used for virable resistor.

Opam2: Operation amplifier which is used for each part.

Vres4: Virable resistor.

Vol−div: Input voltage divider which is used to transform the 0~5volts input voltage into 2.4~2.5volts.

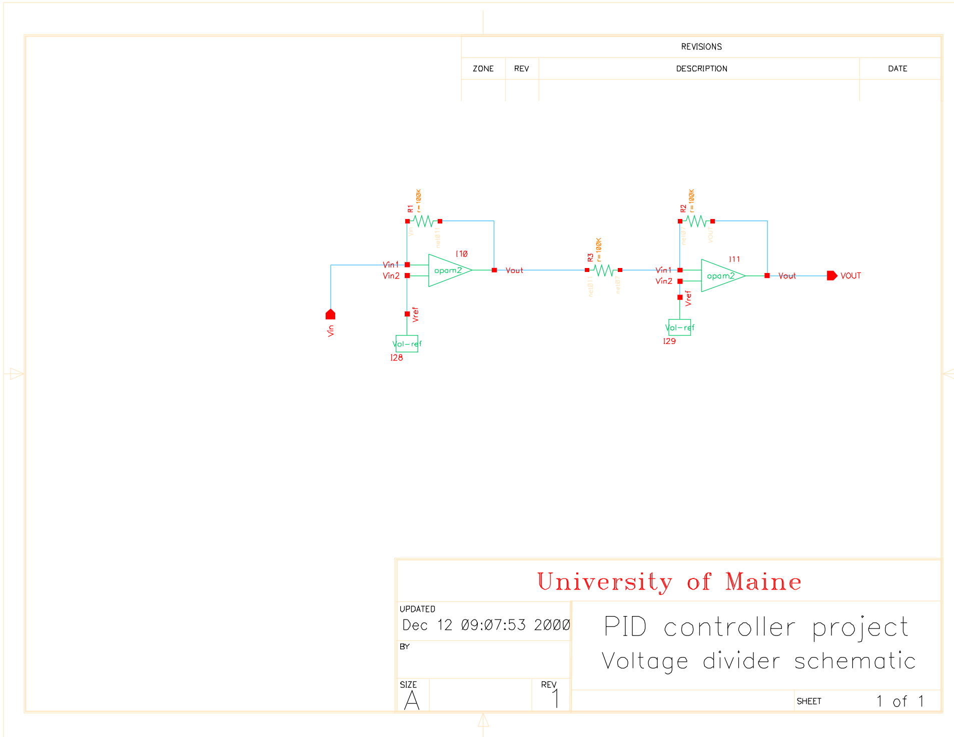
A1.2 PID controller schematic



Vol−div: Input voltage divider which is used to transform the 0~5volts input voltage into 2.4~2.5volts.
Summation: Which is used as an subtractor for process feedback signal and setpoint signal.
Derivative2: The derivative part of PID controller.
Integral2: The integral part of PID controller.
Proportional−2: The proportional part of PID controlle.

Analog inputs and outputs:
Vfin: Input signal of process mearument signal(eg. RTD, Thermal Couple).
Vset: Input signal of setpoint.
Kd: Adjusting coefficient of derivative part.
Ki: Adjusting coefficient of integral part.
Kp:Adjusting coefficient of proportional part.
Ci1,Ci2: External capacitor of integral part.
Cd1,Cd2: External capacitor of derivative part.
Vpidout: Output signal of PID controller.
Fout,SEout,Suout,Dout:Testing point of relative parts.

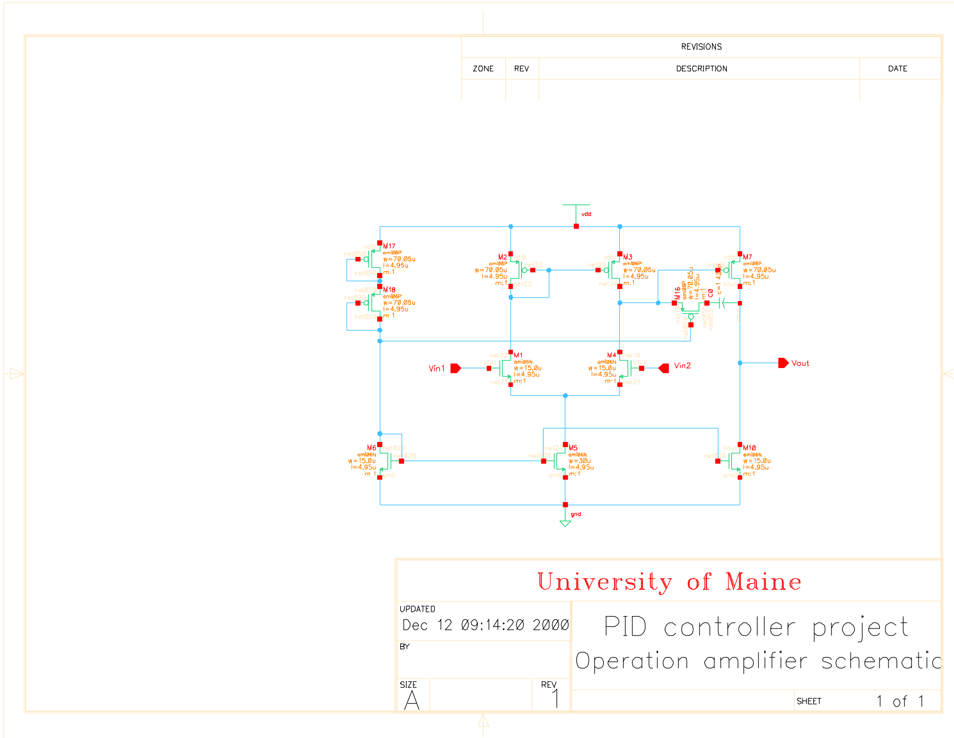
A1.3 Voltage divider



Input voltage divider which is used to transform the 0~5volts input voltage into 2.4~2.5volts.
Opam2: Operation amplifier.
Vol−ref: 2.5 voltage reference for operation amplifier.

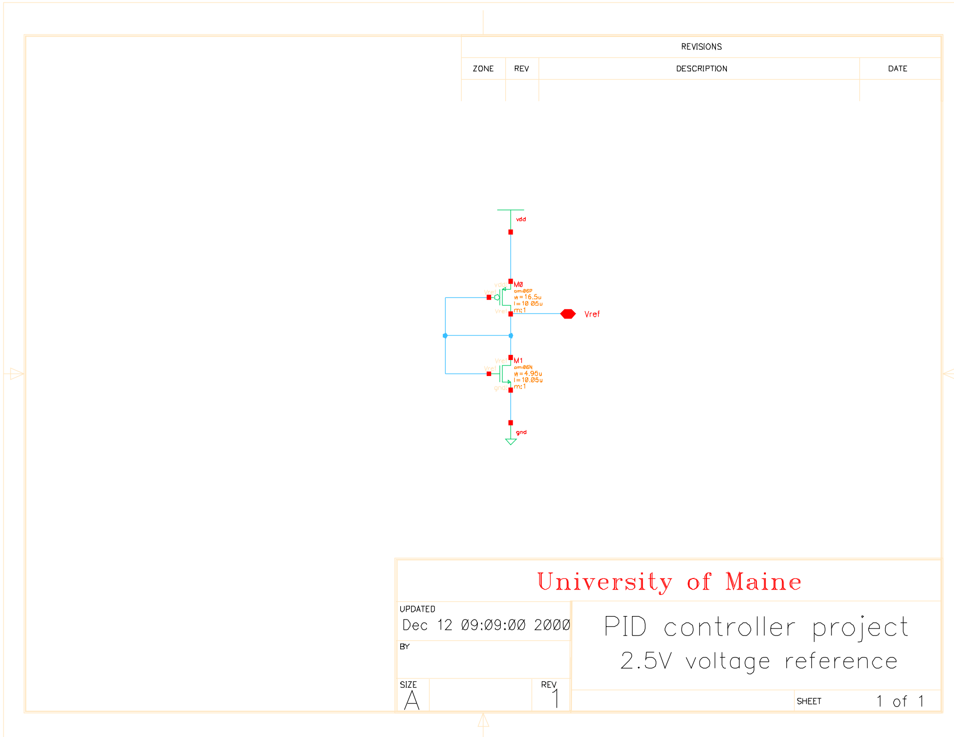
Vin: Input of voltage divider which should be connected one 2.5M ohm resistor.
VOUT: Output of voltage divider.

A1.4 Operation amplifier



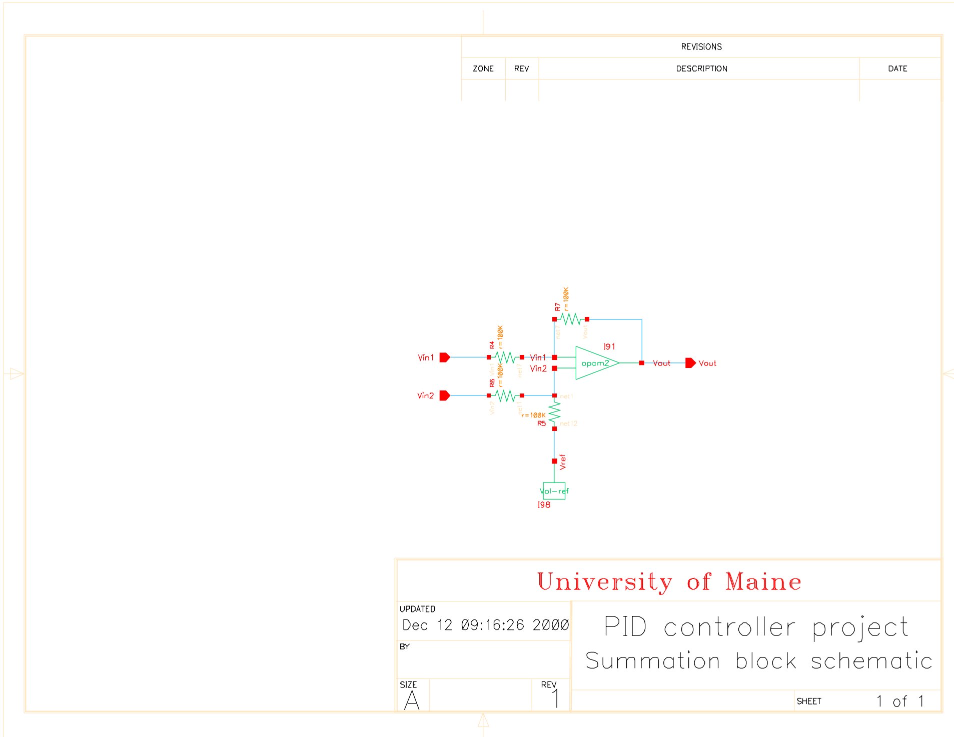
Vin1: Negative input of operation amplifier.
Vin2: Positive input of operation amplifier.
Vout: Output of operation amplifier.

A1.5 Voltage referance



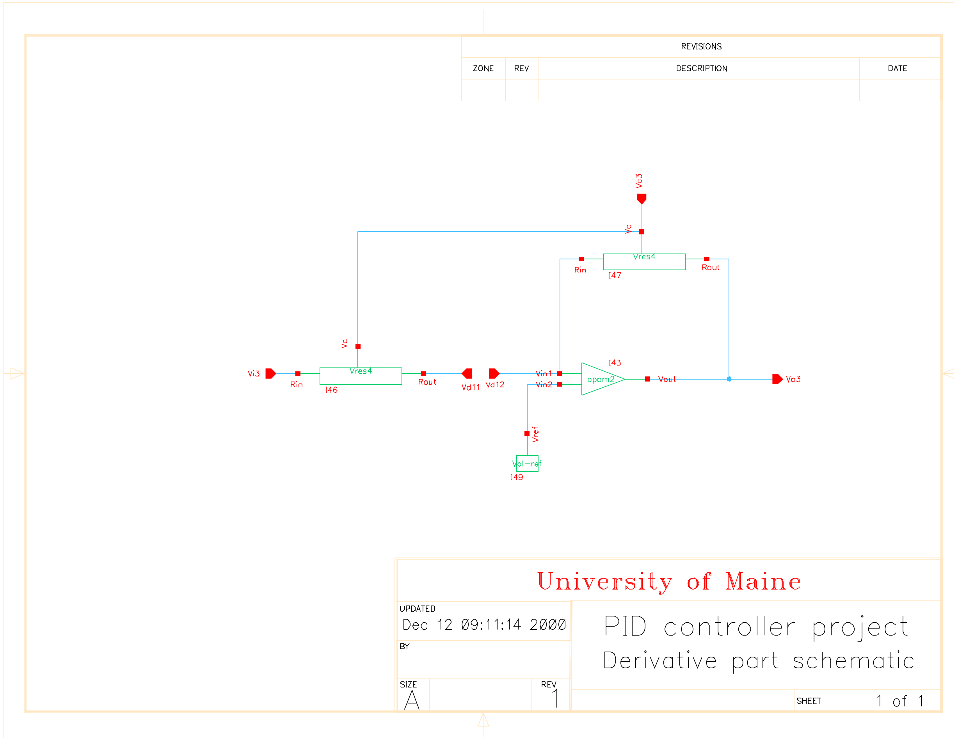
Vref: Supply 2.5volts as the referance voltage for operation amplifier.

A1.6 Summation block:



Vin1: Output of voltage divider for process feedback signal.
Vin2: Output of voltage divider for setpoint.
Vout: Output of the summation block which is a subtractor.

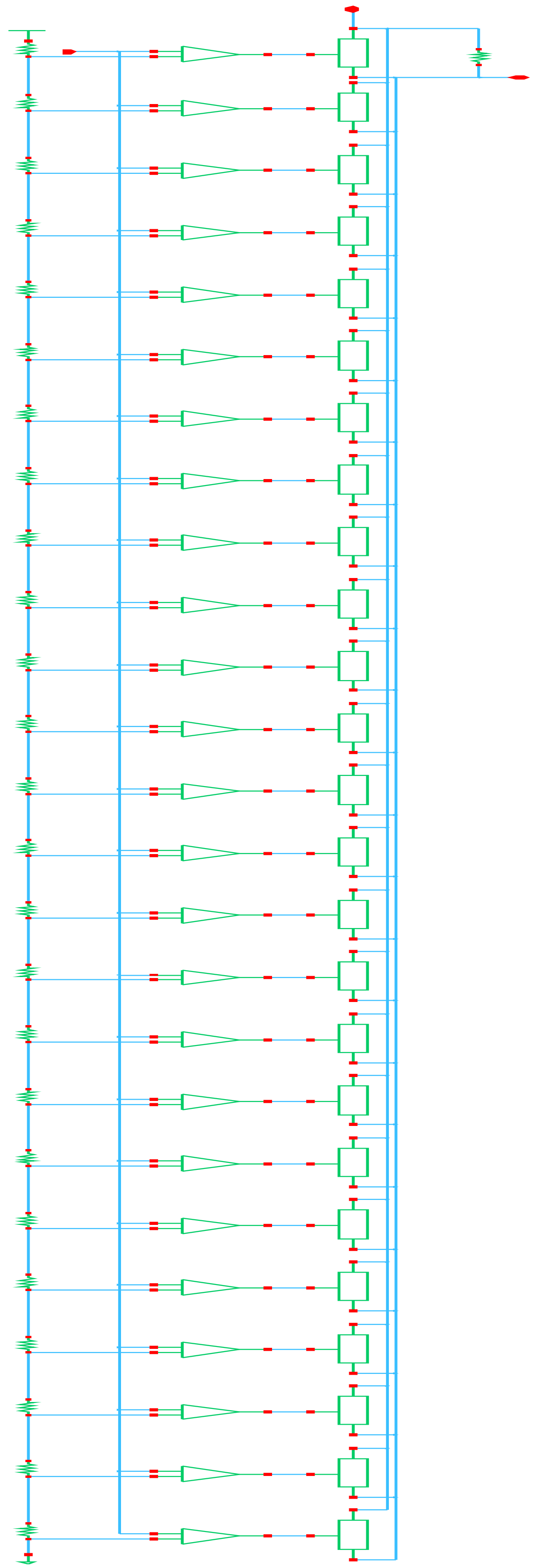
A1.7 Derivativ part



Vres4: Virable resistor
Opam2: Operation amplifier.
Vol−ref: 2.5 voltage reference for operation amplifier.

Vi3:Input signal of derivative part.
Vc3: Coefficient of Voltage control resistor.
Vo3: Output of derivative part.
Vd11,Vd12: External capacitor (4uf).

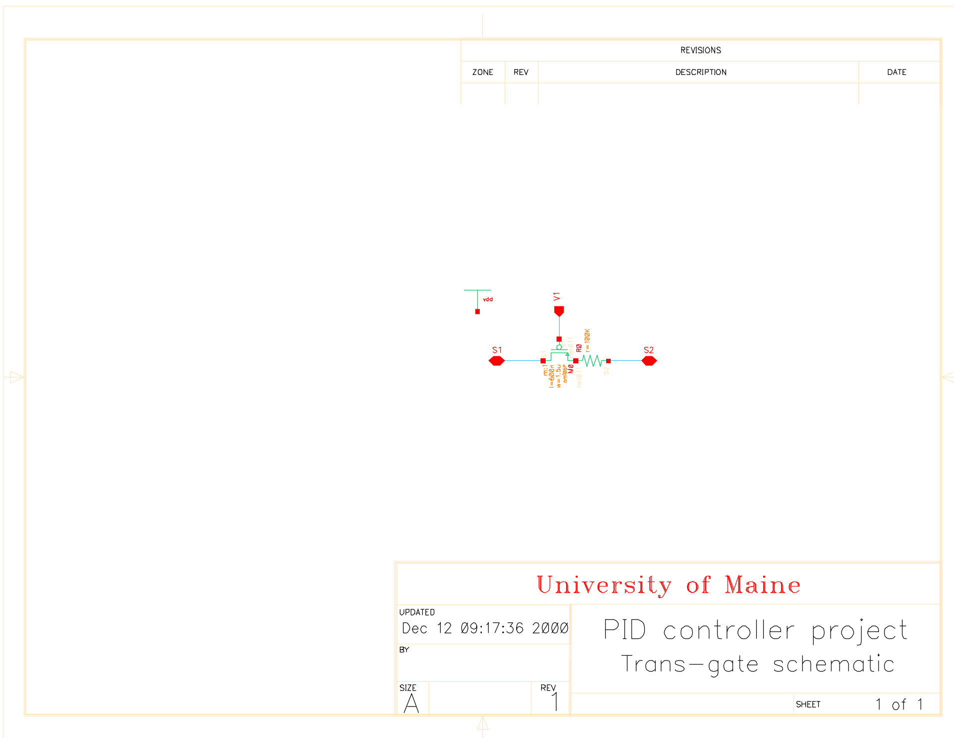
A1.8 Vriable resistor



Opam1: Comparator
Transgate: Working as a switch to connect or disconnect each 100K ohm resistor.

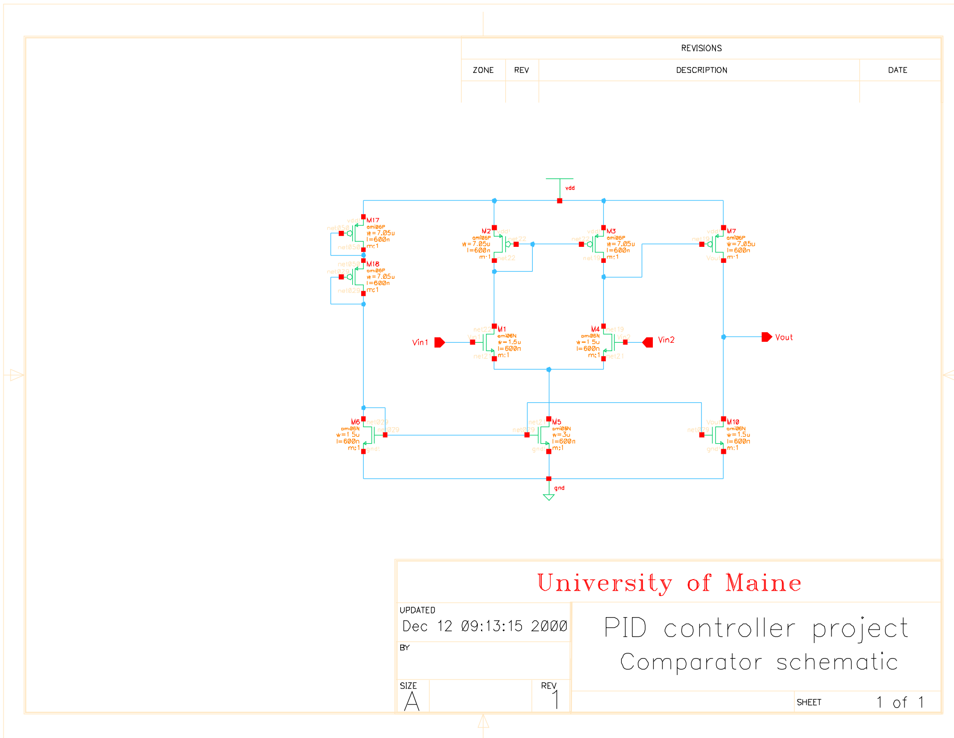
Rin: One terminal of virable resistor.
Rout: Another terminal of virable resistor.
Vc: Input bias voltage (0~5v) signal.

A1.9 Trans gate



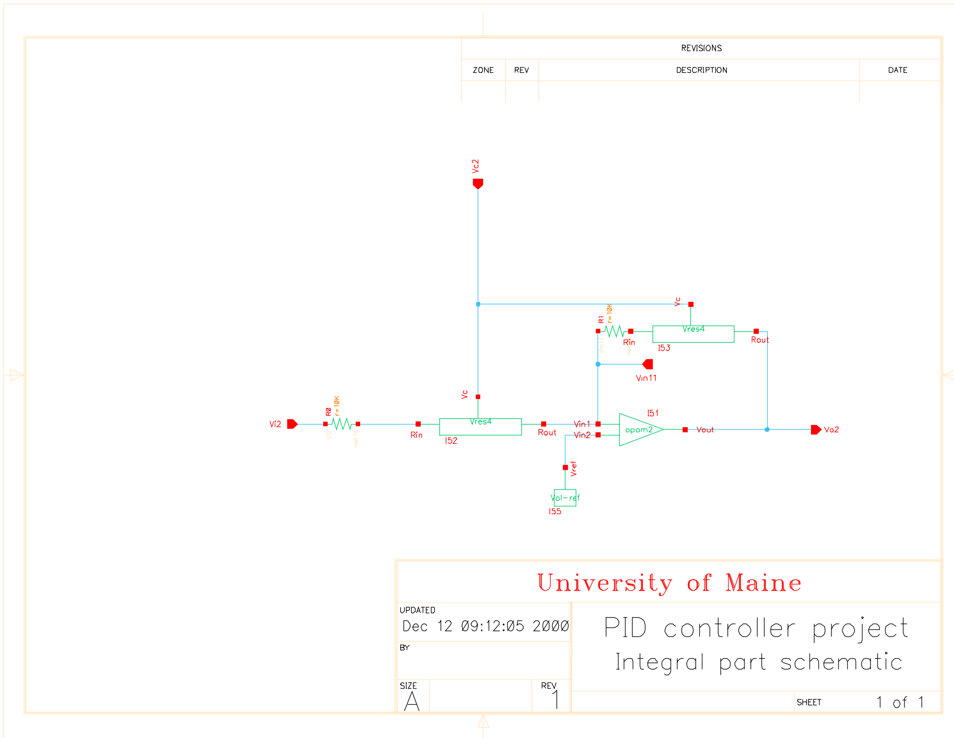
S1: One terminal of transgate.
S2: Another terminal of transgate.
Vc: Output of the comparator.

A1.10 Comparator



Vin1: Negative input of comparator.
Vin2: Positive input of comparator.
Vout: Output of comparator.

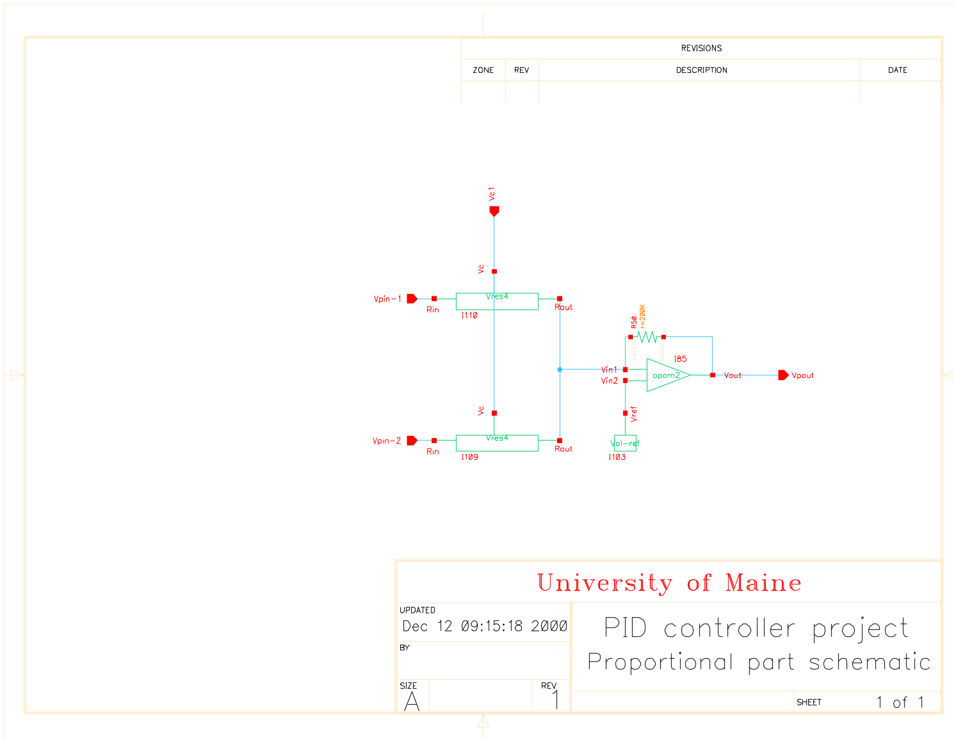
A1.11 Integral part



Vres4: Virable resistor
Opam2: Operation amplifier.
Vol−ref: 2.5 voltage reference for operation amplifier.

Vi3:Input signal of integral part.
Vc3: Coefficient of Voltage control resistor.
Vo3: Output of integral part.

A1.12 Proportional part

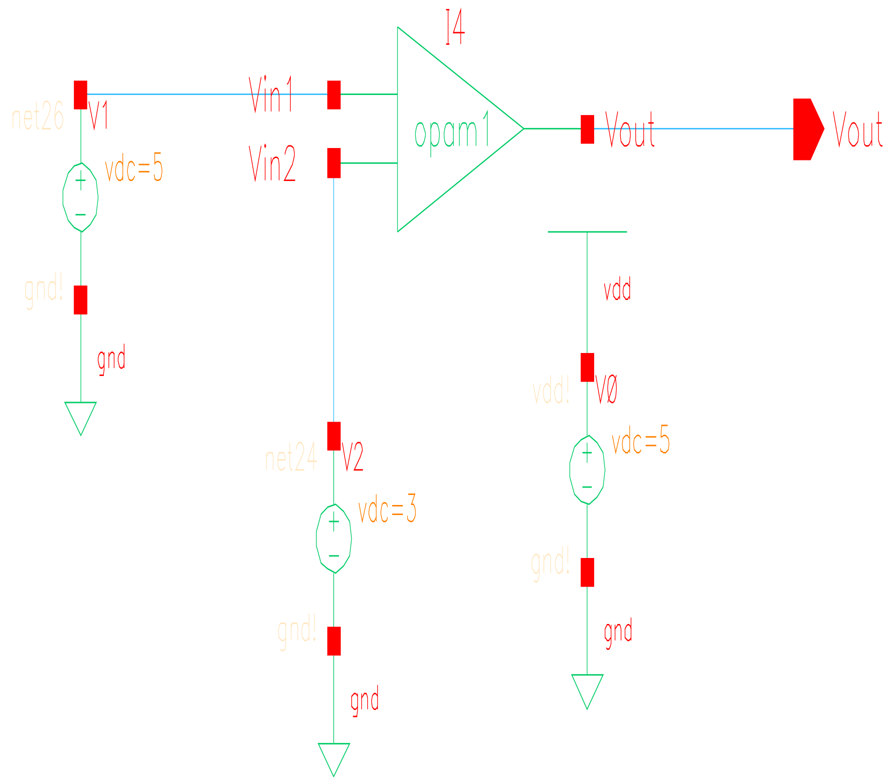


Vres4: Virable resistor
Opam2: Operation amplifier.
Vol−ref: 2.5 voltage reference for operation amplifier.

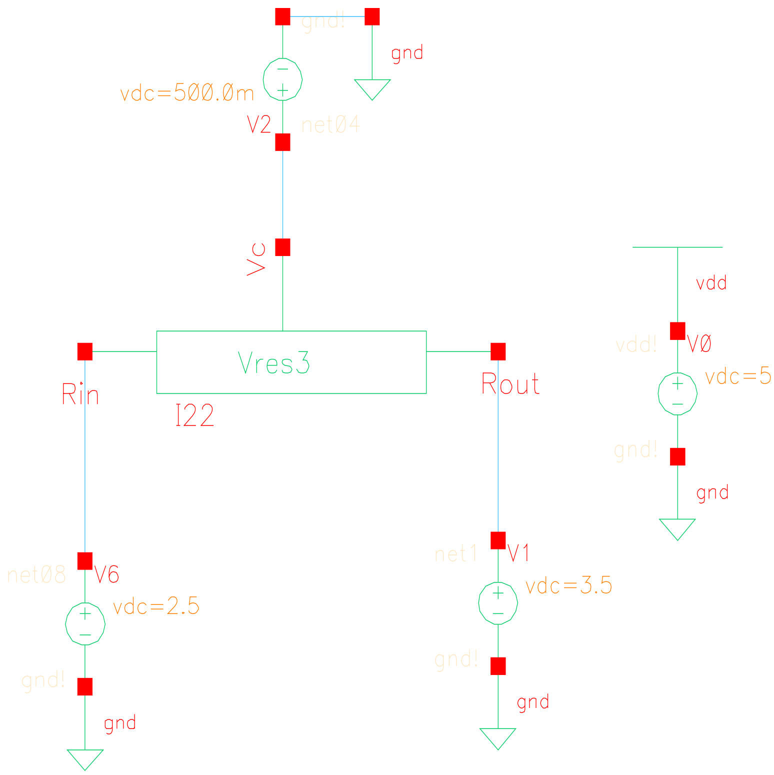
Vpin−1:Output signal of derivative part.
Vpin−2:Output signal of integral part.
Vc1: Coefficient of Voltage control resistor.
Vpout: Output of Proportional part.

A2 Testing circuit schematic

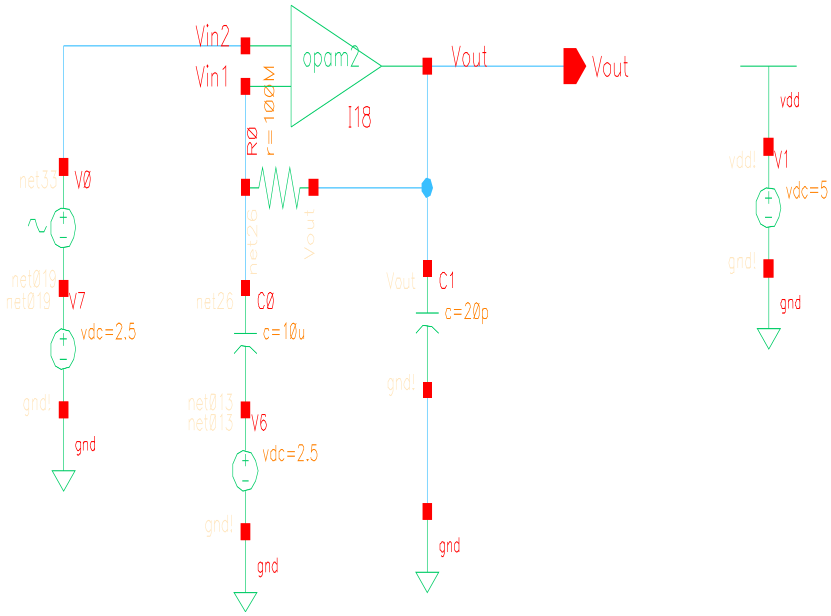
A2.1 Comparator test



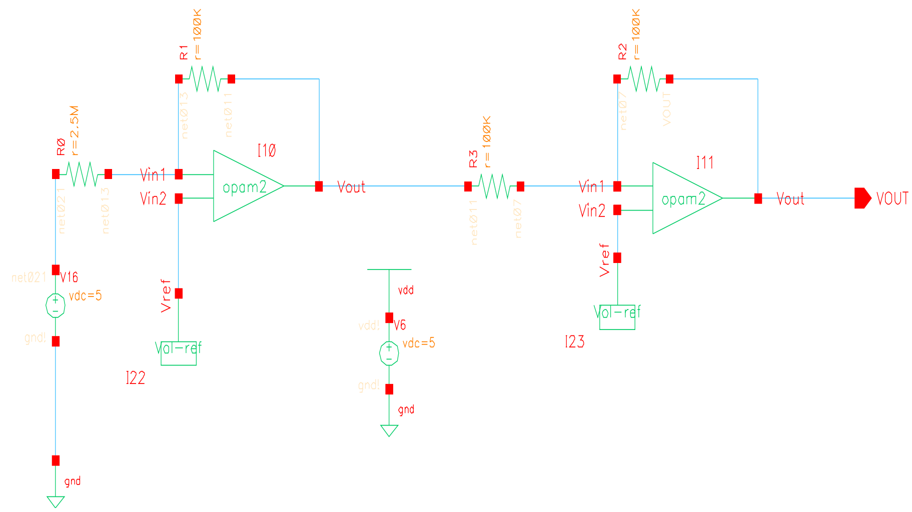
A2.2 Virable resistor test



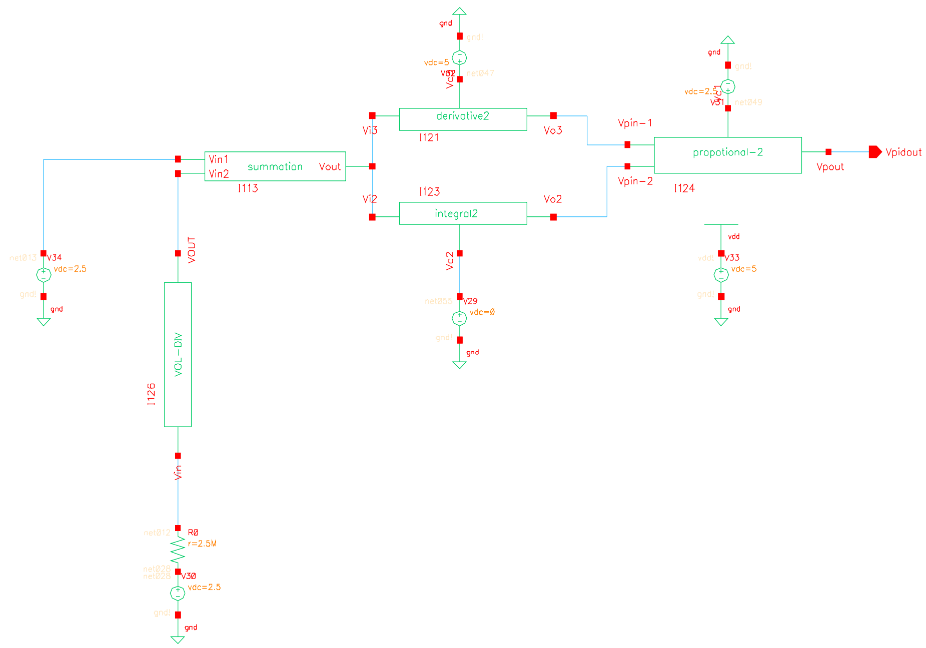
A2.3 Operational amplifier test



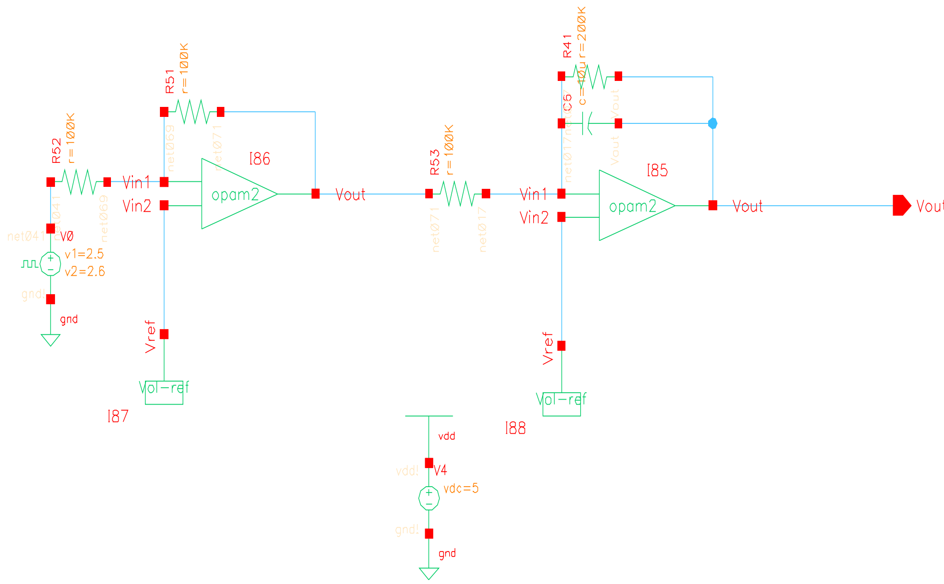
A2.4 Voltage divider test



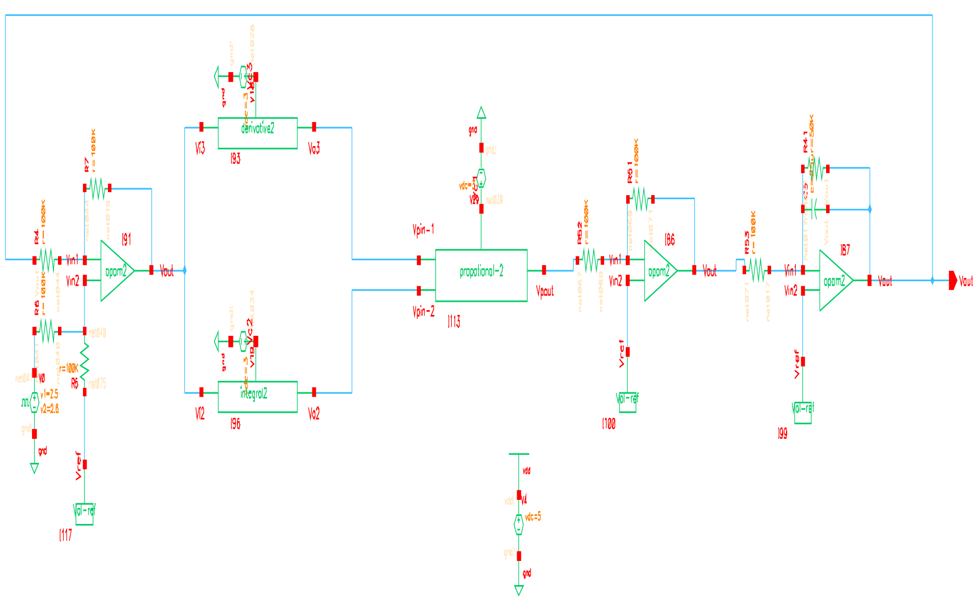
A2.5 PID output range test



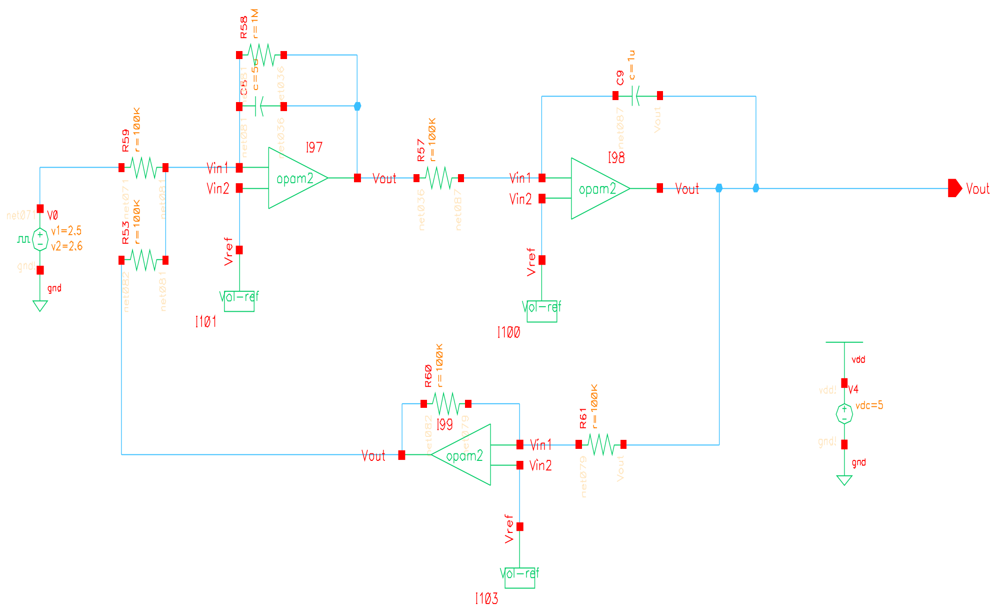
A2.6 First order controlled object open loop test



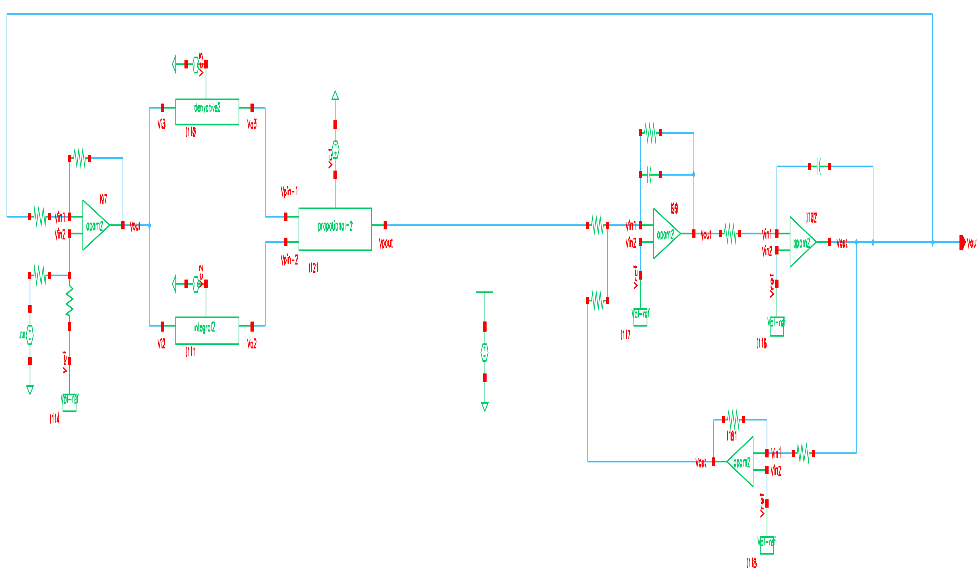
A2.7 First order controlled object close loop test



A2.8 Second order controlled object open loop test



A2.9 Second order controlled object close loop test

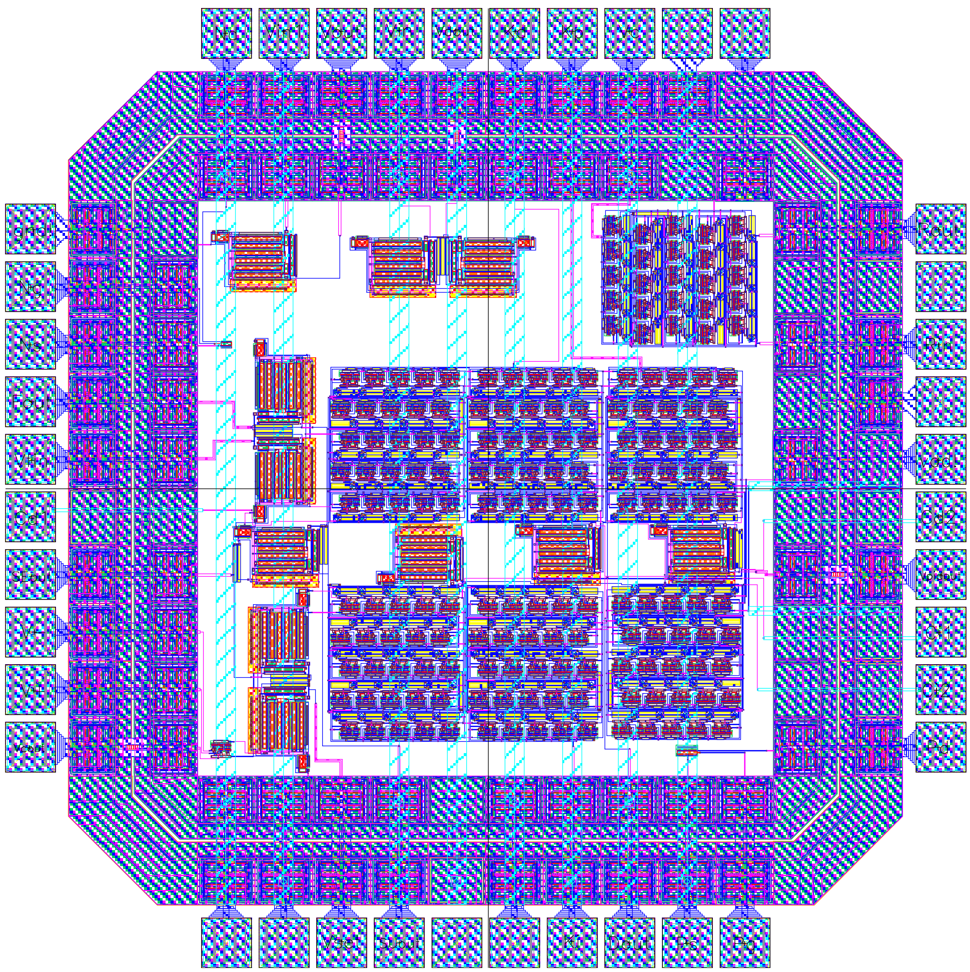


Appendix B: Layout Hieraarchy

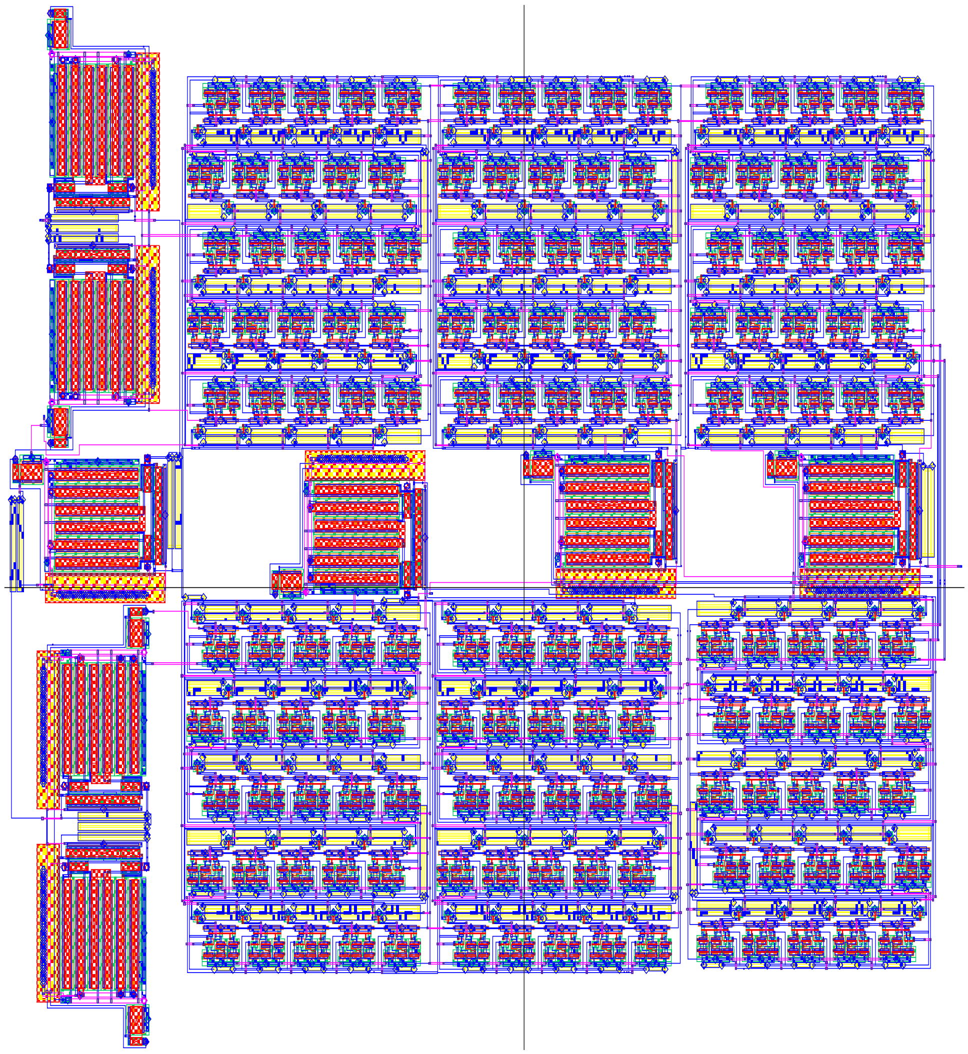
Introduction

In this appendix, we briefly include each layout of this PID controller.

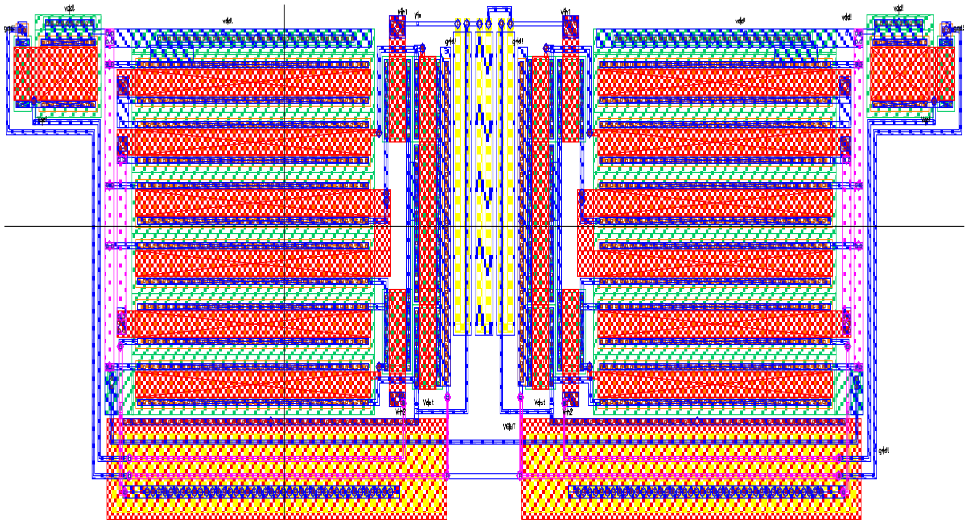
B.1 PID chip top layout



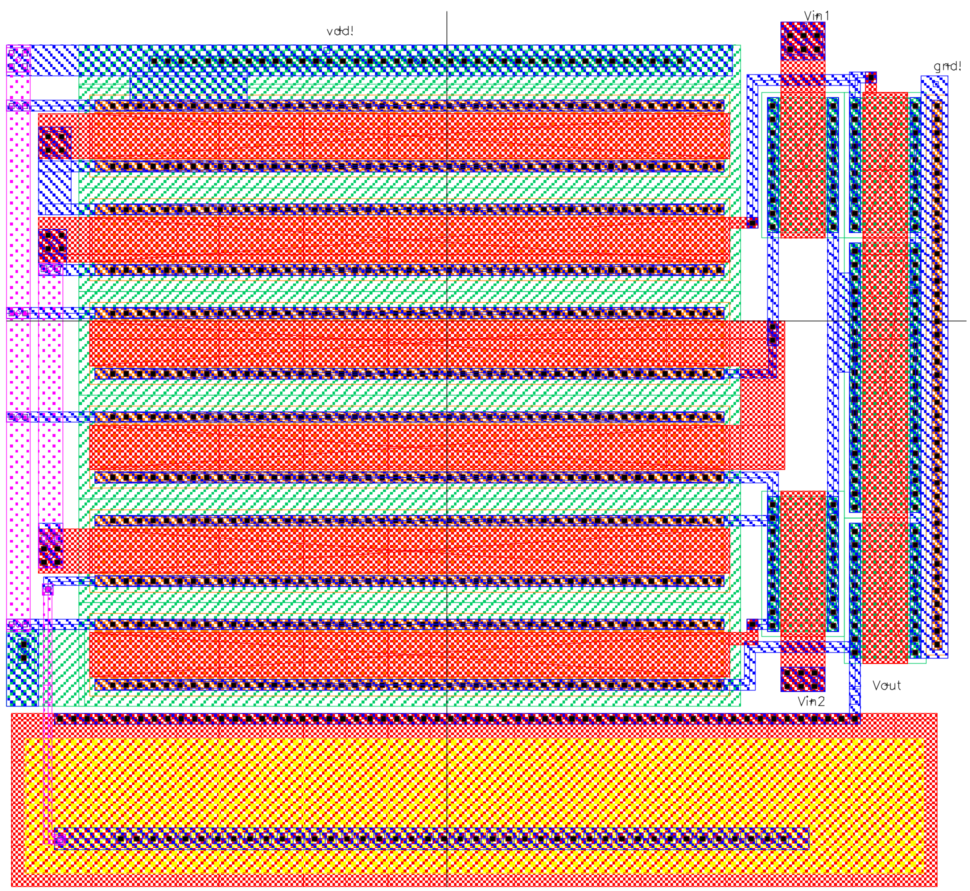
B2. PID controller Layout



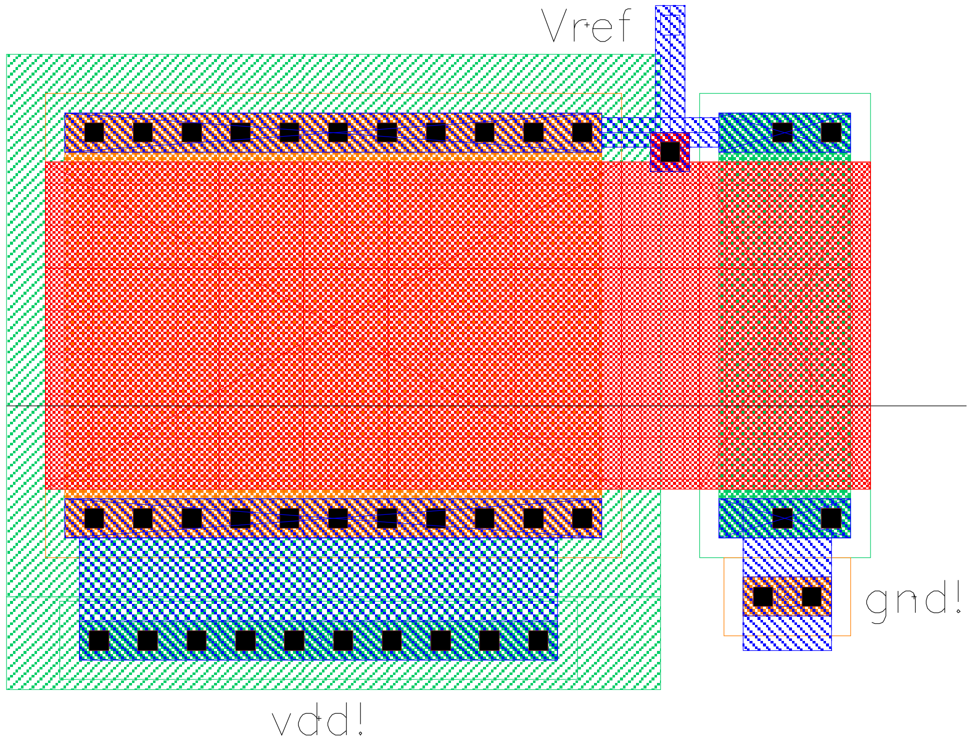
B3 Voltage divider layout



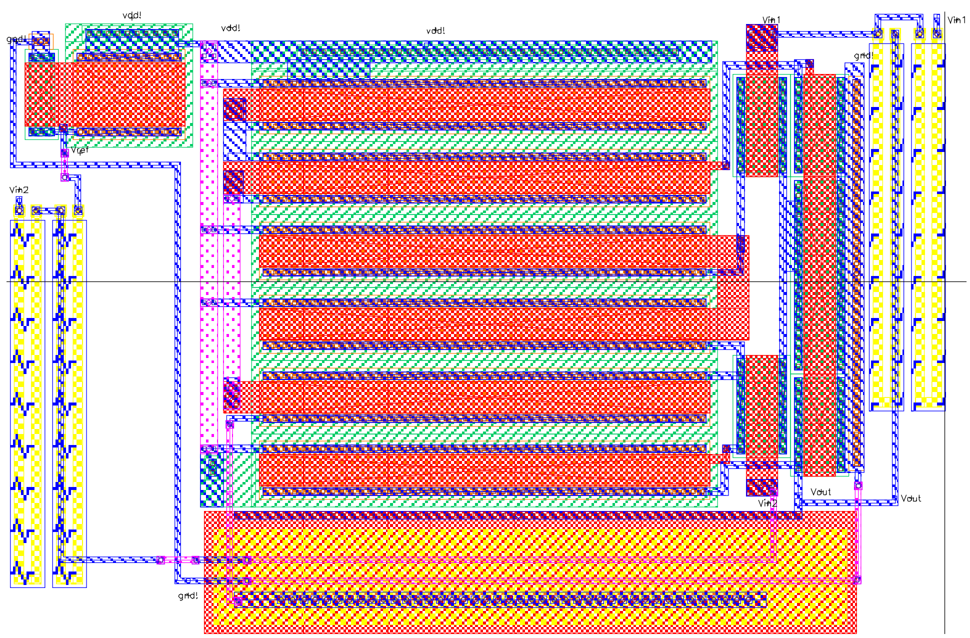
B4 Operation amplifier layout



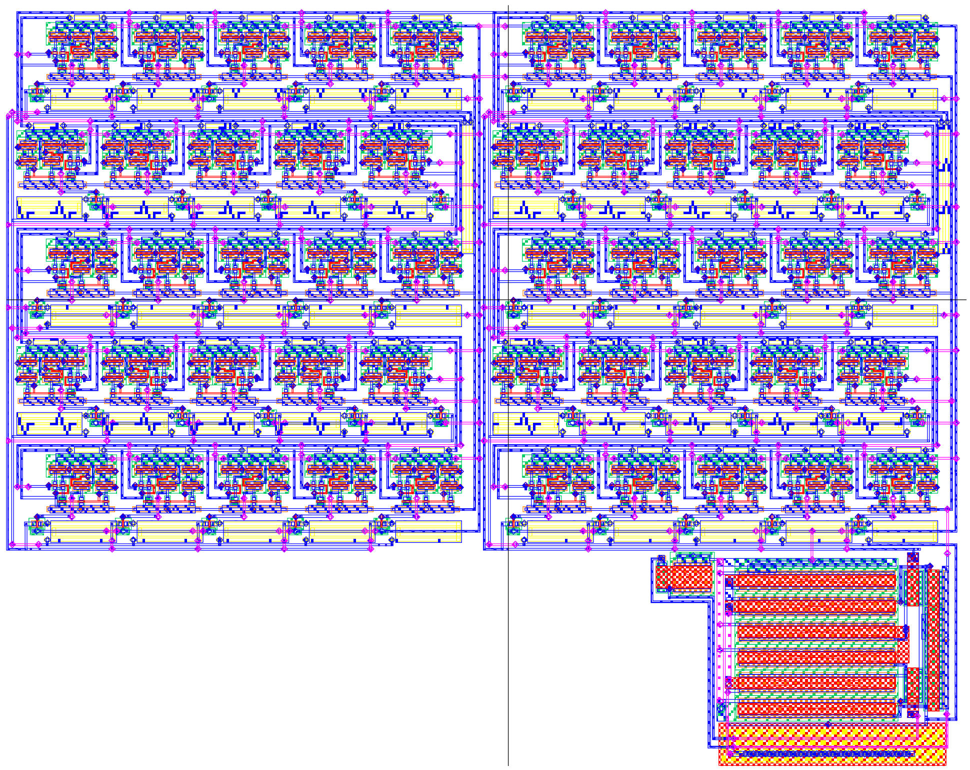
B5 Voltage referance layout



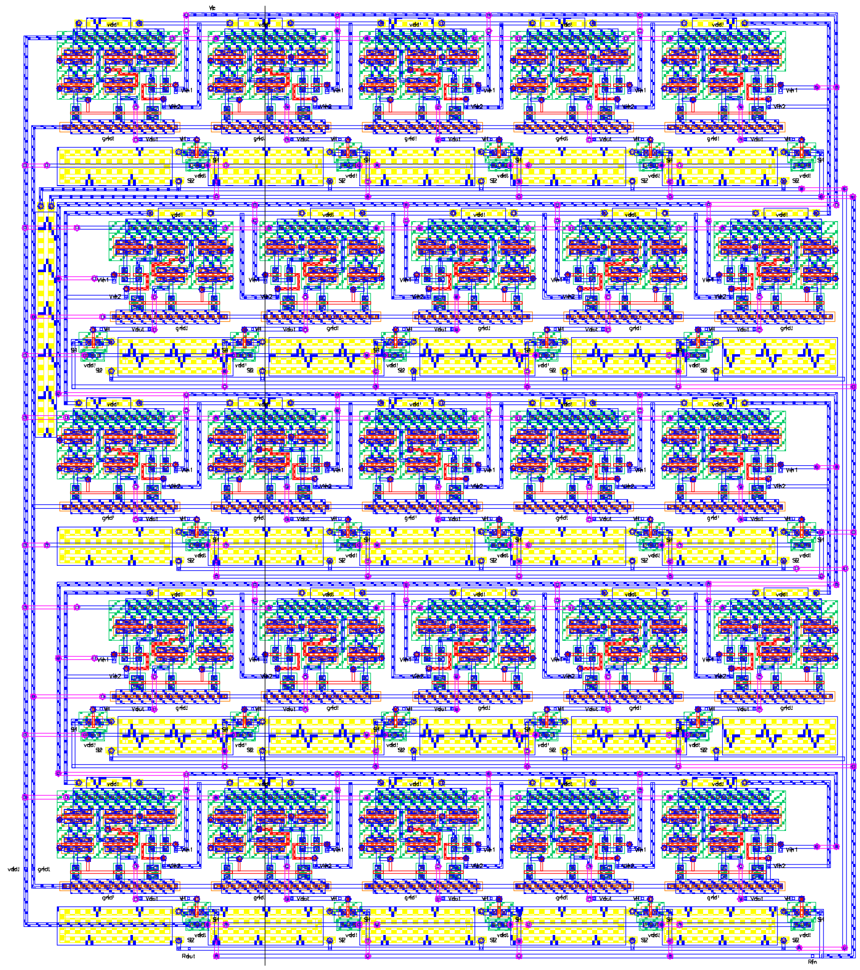
B6 Summation block layout



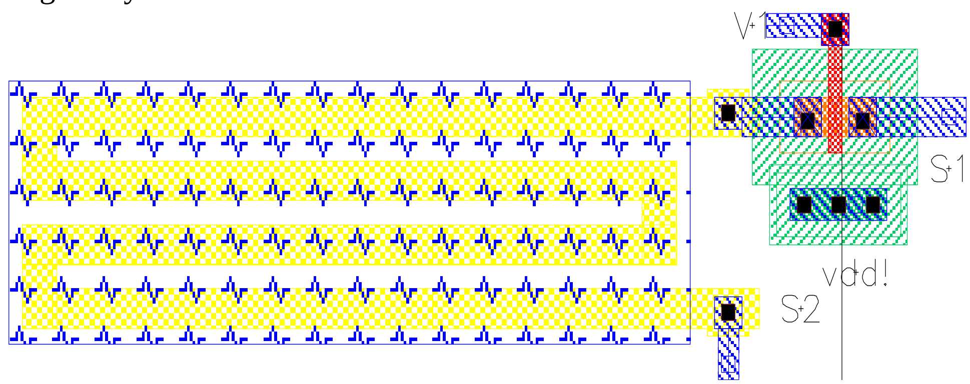
B7 Derivative part layout



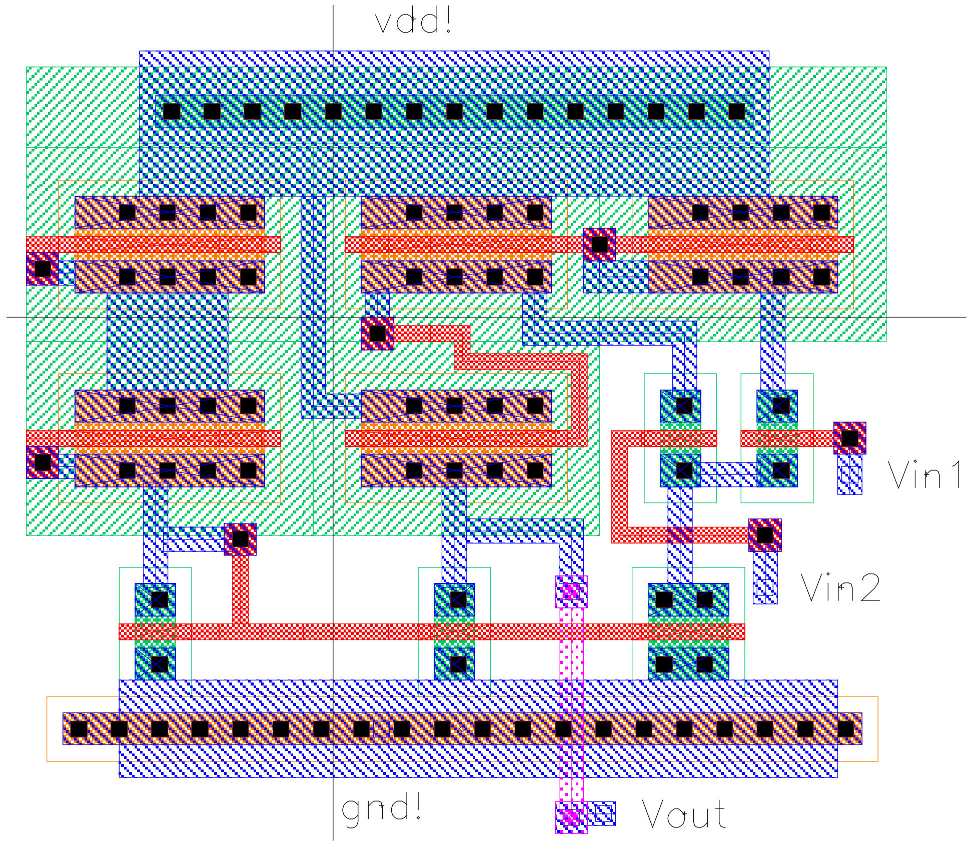
B8 Verivable resistor layout



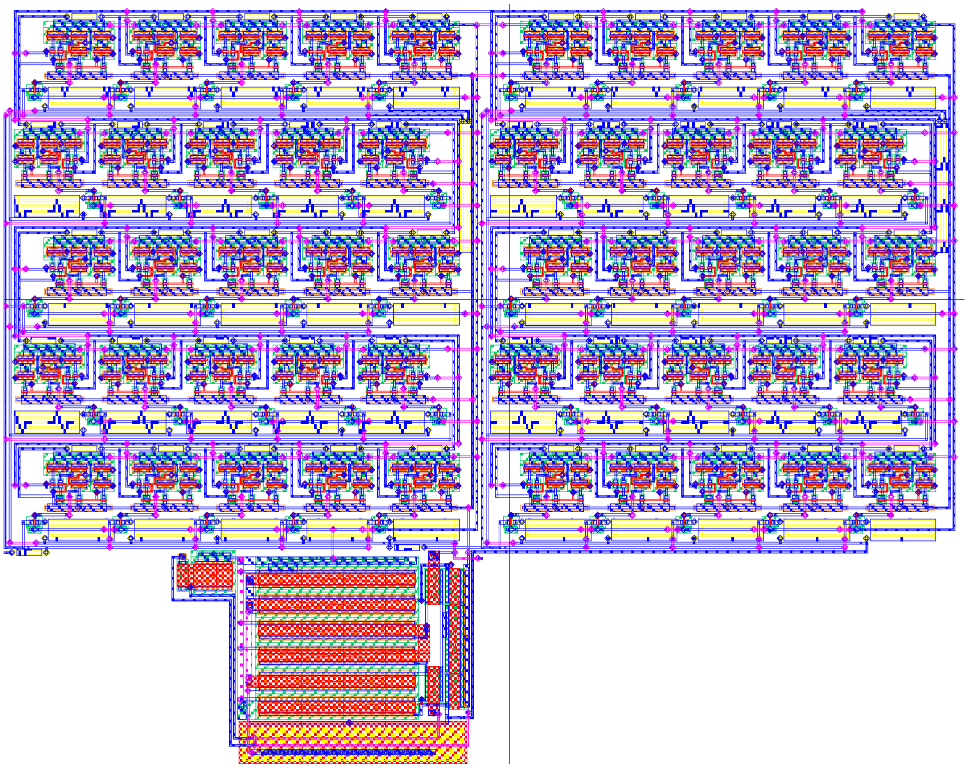
B9 Transgate layout



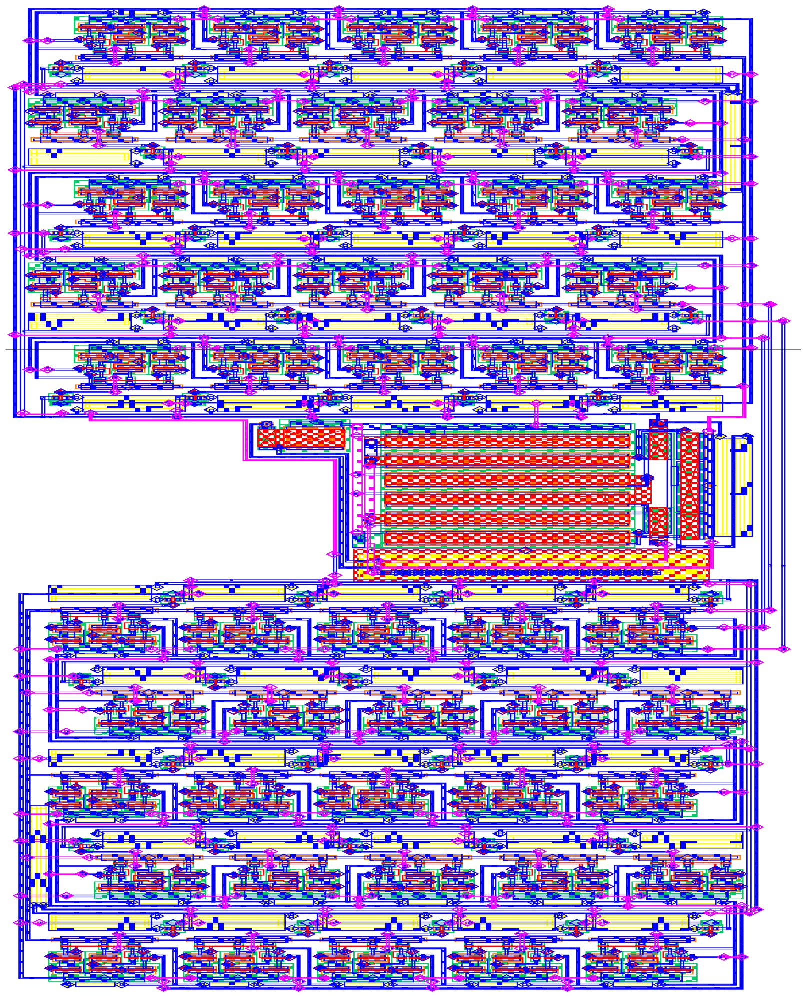
B10 Comparator layout



B11 Integral part layout



B12 Proportional part layout



Appendix C: Top Level Verification

Top level verification includes DRC report of the top level lauout and LVS report for top level schematic and extracted.

C1. DRC report

Passed without error.

C2 . LVS report

@(#)$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $

Like matching is enabled.
Net swapping is enabled.
Creating /usr/grads/guchen/ECE547_Cadence/LVS/xref.out file.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net−list summary for /usr/grads/guchen/ECE547_Cadence/LVS/layout/netlist

count	
1521	nets
32	terminals
373	res
11	cap
1517	pmos
1319	nmos

Net−list summary for /usr/grads/guchen/ECE547_Cadence/LVS/schematic/netlist

count	
1521	nets
32	terminals
373	res
11	cap
1165	pmos
978	nmos

Terminal correspondence points

1	Cd1
2	Cd2
3	Ci1
4	Ci2
5	Dout

6	Fout
7	Kd
8	Ki
9	Kp
10	Nd
11	Ng
12	Ns
13	Pd
14	Pg
15	Ps
16	Rin
17	Rout
18	SEout
19	SUout
20	V+
21	V−
22	Vc
23	Vcout
24	Vdout
25	Vfin
26	Vin
27	Vin1
28	Vout
29	Vpidout
30	Vset
31	gnd!
32	vdd!

The net−lists match.

	layout	schematic	
	instances		
un−matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	3220	2527	
total	3220	2527	
	nets		
un−matched	0	0	
merged		0	0
pruned	0	0	
active	1521	1521	
total	1521	1521	
	terminals		
un−matched	0	0	

matched but different type	0	0
total	32	32

Probe files from /usr/grads/guchen/ECE547_Cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/grads/guchen/ECE547_Cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Appendix D: Biography of Authors

D1 Guang Chen

1988 Bachelor degree of North China Electrical University, Process instrumentation and control.
1988~1998 Engineer and project manager of Shandong Electric Power Engineering and consulting Institute.
1999 Sales and marketing manager of Siemens China Ltd.
2000~ Master candidate of Electrical Engineering in University of Maine.

D2 Zhiqiang Lin
1994 Bachelor degree of Beijing University of Aeronautics and Astronautics, Aircraft Control and Navigation.
1994~1997 Master degree of SiChuan University,Modern electric drive.
1997~1999 Hardware engineer of Huawei Technologies Co.,Ltd. SDH optical transmission system.
2000~ Master candidate of Electrical Engineering in University of Maine.

D3 Jie Zhou
1993 Bachelor degree of Harbin Engineering University, ECE Dept.
1993~1999 Electrical Engineer, Wuhan Marine Propulsion Plant Research Institute.
1999~ Master candidate of Electrical Engineering in University of Maine.