Class-D Audio Amplifier Front-End Circuit

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Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Project Overview

Class-D amplifiers are becoming key components of low power modern consumer devices. Their high efficiency makes them ideal audio amplifiers in laptops, cell-phones, subwoofers, and other mobile audio devices. This VLSI project implements the signal processing 'front end' component of a class-D amplifier. The inputs to the circuit are stereo line-in audio, and the outputs are designed to drive an H-bridge for each audio channel. Volume control has been implemented as a five-bit digital number input. An output mute function is also available as a digital input.

1.2 Objective of Project

The objective of the *Class-D Front-End* design is to integrate all of the signal processing neccessary to drive two different H-bridges from two distinct input channels. Having two inputs and two output drives allows us to utilize the *Class-D Front-End* for stereo operation. The *Class-D Front-End* has been designed to drive the National Semiconductor LMD18201 Monolithic H-Bridge.

Table 1.1: Specifications

- Operates at Vdd=+2.5 volt, Vss=-2.5 volt
- Stereo signal input, +/- 1.5 volt swing
- 5 bit volume control, zero to -31 dB
- Audio bandwidth, 20 Hz to 20 kHz
- Chip output will drive National LMD18201 H-Bridge IC's

1.3 Specifications

Since this was our first analog VLSI design, specifications were relaxed. Most circuit operation was in the audio frequency band, making many circuits relatively easy to design. Listed in Table 1.1 are the specifications for the *Class-D Front-End* design.

1.4 Design Macros

A table listing all design macros used in the *Class-D Front-End* design is provided in Table 1.2.

Table 1.2: Macros Listing

Macro Name	Description
AnalogBuffer	analog buffer
OpAmp_FINAL (1)	opamp
OpAmp_FINAL	wide swing opamp
OpAmp_FINAL_bias (1)	bias ckt
pmos (6)	standard cell
nmos (6)	standard cell
OpAmp_FINAL_amp	amp ckt
pmos (6)	standard cell
nmos (6)	standard cell

Continued...

Table 1.2: Macros Listing

Macro Name	Description
Comparator	comparator
Mux_2to1	2 to 1 mux
Mux_2to1_lay2 Mux_2to1 (1)	alternate layout for 2 to 1 mux
Mux_4to1 Mux_2to1 (3)	4 to 1 mux
Mux_8to1 Mux_2to1 (1) Mux_4to1 (2)	8 to 1 mux
volctrl	volume control ckt
VC_ROM (1)	ROM
Bit0 (21)	bit zero
Bit1 (11)	bit one
S2G_1p12 (4)	stage 2 gain of 1.12 bit pattern
S2G_1p25 (4)	stage 2 gain of 1.25 bit pattern
S2G_1p4 (5)	stage 2 gain of 1.4 bit pattern
S2G_1p58 (5)	stage 2 gain of 1.58 bit pattern
S2G_1p77 (5)	stage 2 gain of 1.77 bit pattern
S2G_1p99 (5)	stage 2 gain of 1.99 bit pattern
S2G_1p23 (2)	stage 2 gain of 1.23 bit pattern
S2G_1 (2)	stage 2 gain of 1 bit pattern
S1G_p1 (7)	stage 1 gain of 0.1 bit pattern
S1G_p2 (10)	stage 1 gain of 0.2 bit pattern
S1G_p4 (14)	stage 1 gain of 0.4 bit pattern
S1G_1 (2)	stage 1 gain of 1 bit pattern
LineDriver (1)	ROM line driver ckt
Inv_2p7u_1p5u (5)	standard cell
OpAmp_FINAL_amp	amp ckt

Continued...

Table 1.2: Macros Listing

Macro Name	Description
pmos (6)	standard cell
nmos (6)	standard cell

1.5 Pin Out

There were no major issues with respect to the pinout of the *Class-D Front-End* design. Supply net pins were assigned to the package pins with the greatest parasitic capacitance. This parasitic is actually beneficial, since it provides additional supply bypass. Critical signals were assigned to pins with the least parasitics.

Table 1.3: PinOut

Pin	Pad Type	Name	Desc
1	padvdd	vdd	VDD pin
2	padio	sq_wave	Bistable test, square wave output
3	padaref	tri_wave	Bistable test, triangle wave output
4	padaref	20kb	$20k\Omega$ test resistor, terminal B
5	padaref	20ka	$20k\Omega$ test resistor, terminal A
6	padio	test2_out	Comparator test circuit output
7	padaref	test2_in_plus	Comparator test positive differential input
8	padaref	test2_in_minus	Comparator test negative differential input
9	padaref	in_left_plus	Left channel positive input
10	padaref	in_left_minus	Left channel negative input
11	padaref	in_right_plus	Right channel positive input
12	padaref	in_right_minus	Right channel negative input
13	padio	left_pwm	Left channel PWM output
14	padio	left_dir	Left channel DIR output
15	padio	mute	Mute input bit
16	padio	vol_5	Volume control input bit
17	padio	vol_4	Volume control input bit
18	padio	vol_3	Volume control input bit
19	padio	vol_2	Volume control input bit
20	padio	vol_1	Volume control input bit

Continued...

Table 1.3: PinOut

Pin	Pad Type	Name	Desc
21	padvss	vss	VSS pin
22	padio	logic_gnd	Logical GND for H-Bridge
23	padio	test_v5	Test circuit volume control input bit
24	padio	test_v4	Test circuit volume control input bit
25	padio	test_v3	Test circuit volume control input bit
26	padio	test_v2	Test circuit volume control input bit
27	padio	test_v1	Test circuit volume control input bit
28	padio	right_dir	Right channel DIR output
29	padio	right_pwm	Right channel PWM output
30	padgnd	gnd	GND pin
31	padaref	opamp_out	Test op-amp output
32	padaref	opamp_minus	Test op-amp minus input
33	padaref	opamp_plus	Test op-amp plus input
34	padio	osc_out	Test ring oscillator output
35	padaref	test_in_plus	Test circuit positive input
36	padaref	test_in_minus	Test circuit negative input
37	padaref	10kb	$10k\Omega$ test resistor, terminal B
38	padaref	10ka	$10k\Omega$ test resistor, terminal A
39	padaref	test_amped	Test circuit preamp output
40	padio	test_pwm	Test circuit PWM output

1.6 Limitations of Current Design

This design would benefit greatly from fully-differential internal circuitry. According to Baker [1] p742, differential topology would give us a doubling in all of our signal swings, which would increase the dynamic range of all our signals. This would obviously enhance the audio signal quality. Differential design would also reduce harmonic distortion throughout the system, as well as increase rejection of substrate coupled noise.

Chapter 2

Circuit Design

2.1 Description of Schematics

Refer to Table 1.2 for a list of all macros used in this design.

Refer to Appendix A for full-size schematics of each cell.

2.1.1 Wide-Swing OpAmp

For this project, an op-amp with output swing that can approach the supply rails was needed. This allowed for enhanced dynamic range compared with designs with less output swing capability. The op-amp design is a *Wide-Swing Folded-Cascode Operational Transconductance Amplifier (OTA)* design described in Baker [1] pp657.

The op-amp is separated into two distinct components, amplification stages (Figure 2.1) and biasing (Figure 2.2). The input CMR for this op-amp extends beyond the supply rails, but the output is limited to the range of the rails. The differential amplifier is wide-swing. The biasing circuit establishes a bias current of 10 μA that is mirrored throughout the amp. A folded-cascode output buffer has been added to the OTA so that the op-amp is capable of driving resistive loads.

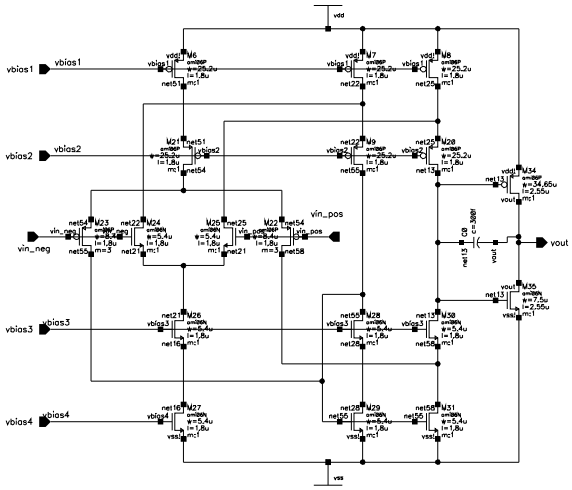

Figure 2.1: Amp Stages Schematic

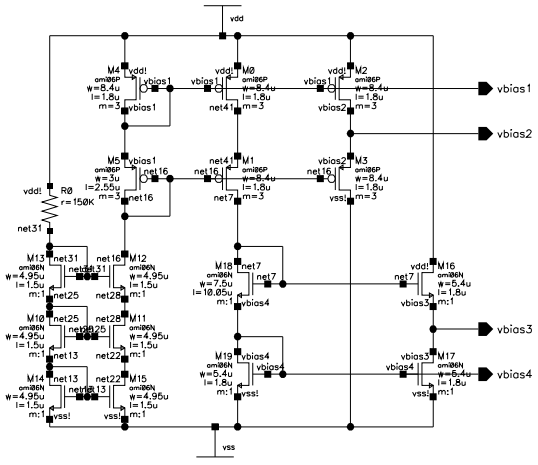

Figure 2.2: Bias Schematic

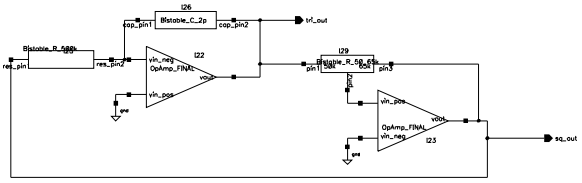

Figure 2.3: Bi-stable Schematic

2.1.2 Bi-Stable Oscillator

Bi-stable oscillators rely on positive feedback to slam the op-amp outputs back and forth between two stable states, the supply rails.

This circuit, shown in Figure 2.3, also contains an integrator, such that as the bistable cycles between states, the integrator is in essence integrating the basic square-wave output of the bistable. This circuit oscillates with a 50% duty cycle at 240 kHz. 240kHz was chosen as a operating frequency well above the Nyquist rate for the frequencies of interest in this project - audio band 20 Hz - 20 kHz See Sedra & Smith [2] p1005 for more information.

2.1.3 Comparator

This cell is used to compare the triangle wave and the input waveform to provide a pulse-width modulated signal. The design used is a resized version of the self-biased comparator shown on p699 of Baker [1]. The gate sizes were modified to match our technology. The ratios of the shorter length devices in Baker's book (70/5 and 15/5) was scaled to the meet our minimum channel length of .6 μm, so they became 8.4/.6 and 1.8/.6. The long length devices (5/50) were scaled so that their width related to our minimum channel width of 1.5 μm, making the devices 1.5/15. Two inverters were added to the output of the comparator to make the output sharper. The comparator is shown in Figure 2.4.

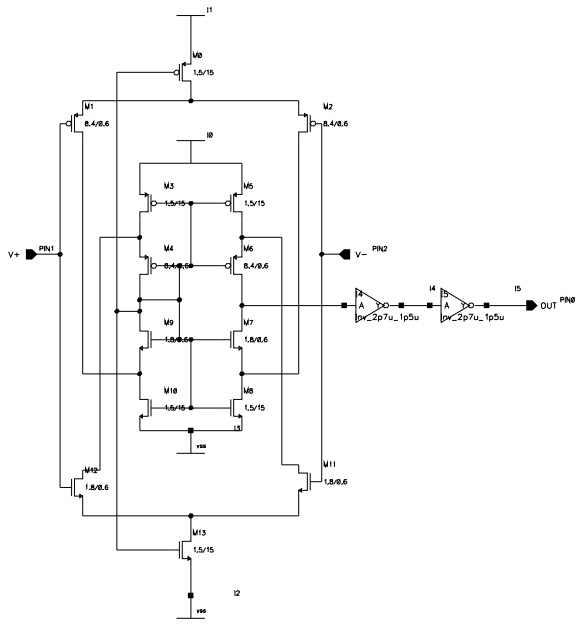

Figure 2.4: Comparator Schematic

2.1.4 Multiplexors (Mux_2to1, Mux_4to1, Mux_8to1)

Mux_2to1

This is a 2 to 1 mux/demux for analog signals. It uses the TX_Gate cell in the configuration shown in Figure 13.8 on p261 of Baker [1]. When the select (S) is low, B is output. When S is high, A is output.

Mux_4to1

This is a 4 to 1 mux/demux for analog signals. It uses two Mux_2to1 cells fed into a single Mux_2to1 cell to implement the 4 to 1 mux/demux. The selection lines S[1], S[0] are configured so that the binary value of S[1], S[0] determines which input is passed. For example, if $S[1] = high$ and $S[0] = low$, then IN[2] is passed.

Mux_8to1

This is an 8 to 1 mux/demux for analog signals. It uses two Mux_4to1 cells fed into a single Mux_2to1 cell to implement the 8 to 1 mux/demux. The selection lines S[2], S[1], S[0] are configured so that the binary value of S[2], S[1], S[0] determines which input is passed. For example, if $S[2] = high$, $S[1] = high$, and $S[0] = low$, then IN[6] is passed.

TX_Gate

This is a transmission gate designed to pass or not pass our analog signals based on a digital signal input. It is a standard transmission gate of the type that uses both P and N type transistors.

2.1.5 Volume Control Logic

Volctl

The volctrl circuit shown in Figure 2.5 is used to drive the muxes in the VC_preamp circuit. It has 5 volume selection inputs and 6 mux driving outputs. A scheme using combinational logic was designed for this block and rejected. Instead, a ROM was used because it can be more easily changed than the combinational logic and it is easier to layout. In addition, this choice allows for more flexibility for potential changes to the design. The ROM was also an interesting exercise, since none have been implemented at UMaine. The ROM consists of the VC_ROM, which is the array of 1's and 0's, and the line_driver that selects and drives one of the 32 ROM lines from the 5 bit input.

VC_ROM

The VC_ROM shown in Figure 2.6 is driven by the Line_driver, and it drives the mux select lines in the VC_preamp circuit. The selection lines consist of a PMOS tied to GND as a weak pull-up which is connected through an offset inverter (switches around -1 volt) and a regular inverter. With this set up the line is high unless it is pulled low before the inverters. To pull the line low, an NMOS is connected to the line. A single row of 6 bits can drive all 6 selection lines. Note that the line_driver ensures that only one row is driven at a time. The bits are either not connected for a high signal, or have an

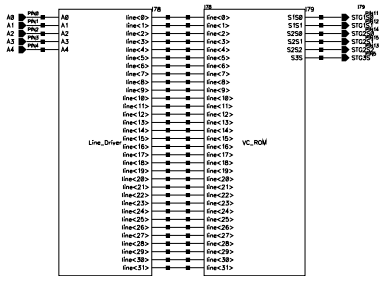

Figure 2.5: Volctrl Schematic

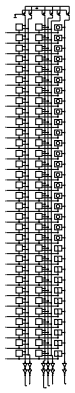

Figure 2.6: VC_ROM Schematic

enabled NMOS pull-down for a low bit. Since the weak pull-up is connected to GND the ROM bits use less power than if the pull-up were connected to VDD. To make the circuit easier to understand and modify the bit pattern for each gain of each stage was encapsulated in a schematic macro.

Line_driver

The line_driver selects and drives only one line on the VC_ROM. It uses the tree decoder method described on pp341-3 of Baker [1]. On the output side of the selection lines, the line is tied to a pull-down NMOS and an offset inverter (switches around -1 volt) connected to a regular inverter. The gate of the pull-down NMOS is tied to the signal line so any 'high' floating lines are sufficiently pulled down. The offset inverter allows the real high signal to

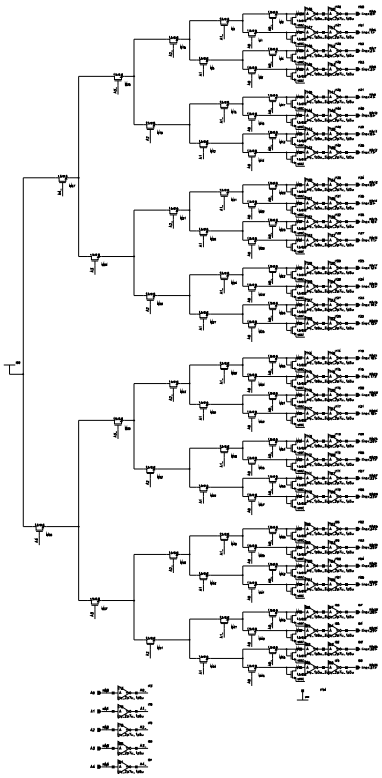

Figure 2.7: Line Driver Schematic

be accepted, since the NMOS will be trying to pull it low. The tree consists of NMOS pass gates, with the common end tied to VDD. The configuration of the tree is an expansion of the tree on page 342 to allow for 5 inputs and 32 outputs. The line driver is shown in Figure 2.7.

Bit0

This cell represents a zero bit in the ROM. It contains an NMOS that pulls the line low when it is active.

Bit1

This cell represents a one bit in the ROM. Since the ROM lines are pulled high, this cell only contains wires to continue the ROM line.

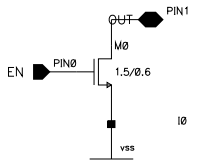

Figure 2.8: Bit Zero Schematic

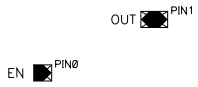

Figure 2.9: Bit One Schematic

2.1.6 Volume Control PreAmplifier

The VC_preamp shown in Figure 2.10 is intended to provide volume control for the input signal before it is fed into the comparator. It has an input signal, 5 volume selection bits, and a conditioned output signal. It provides 32 levels of attenuation in 1 dB increments from 0dB to -31 dB. A scheme was used that uses 3 gain stages, as opposed to 32 separate gain stages. This not only saves on chip space, but it also minimizes differences from process variations. Table 2.1 demonstrates the scheme used to obtain the desired gain with 3 stages:

Table 2.1: Volume Control Amplifier Stage Gains

input	desired gain (dB)	stage 1 gain (V/V)	stage 2 gain (V/V)	stage 3 gain (V/V)	actual gain (dB)
00000	0	-1	1	-1	0
00001	-1	-0.4	2.23	-1	-0.9927
00010	-2	-0.4	1.99	-1	-1.98174
00011	-3	-0.4	1.77	-1	-2.99933
00100	-4	-0.4	1.58	-1	-3.98566
00101	-5	-0.4	1.4	-1	-5.03624
00110	-6	-0.4	1.25	-1	-6.0206

Continued...

Table 2.1: Volume Control Amplifier Stage Gains

input	desired gain (dB)	stage 1 gain (V/V)	stage 2 gain (V/V)	stage 3 gain (V/V)	actual gain (dB)
00111	-7	-0.4	1.12	-1	-6.97444
01000	-8	-0.2	1.99	-1	-8.00234
01001	-9	-0.2	1.77	-1	-9.01993
01010	-10	-0.2	1.58	-1	-10.0063
01011	-11	-0.2	1.4	-1	-11.0568
01100	-12	-0.2	1.25	-1	-12.0412
01101	-13	-0.2	1.12	-1	-12.995
01110	-14	-0.1	1.99	-1	-14.0229
01111	-15	-0.1	1.77	-1	-15.0405
10000	-16	-0.1	1.58	-1	-16.0269
10001	-17	-0.1	1.4	-1	-17.0774
10010	-18	-0.1	1.25	-1	-18.0618
10011	-19	-0.1	1.12	-1	-19.0156
10100	-20	-0.1	1	-1	-20
10101	-21	-0.4	2.23	-0.1	-20.9927
10110	-22	-0.4	1.99	-0.1	-21.9817
10111	-23	-0.4	1.77	-0.1	-22.9993
11000	-24	-0.4	1.58	-0.1	-23.9857
11001	-25	-0.4	1.4	-0.1	-25.0362
11010	-26	-0.4	1.25	-0.1	-26.0206
11011	-27	-0.4	1.12	-0.1	-26.9744
11100	-28	-0.2	1.99	-0.1	-28.0023
11101	-29	-0.2	1.77	-0.1	-29.0199
11110	-30	-0.2	1.58	-0.1	-30.0063
11111	-31	-0.2	1.4	-0.1	-31.0568

The gains in each stage are achieved by selecting the signal path through resistors in the gain stages which are connected to op amps. The resistors are configured in a 'ladder' so that the number used is kept smaller, and the resistors are more closely matched. The selection of the path is done through muxes that are selected by signals from the volctl circuit. Stage 1 is an inverting op amp with 4 separate gains and 5 total resistors. Stage 2 is

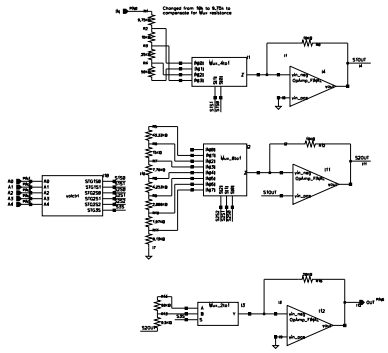

Figure 2.10: Volume Control Preamp Schematic

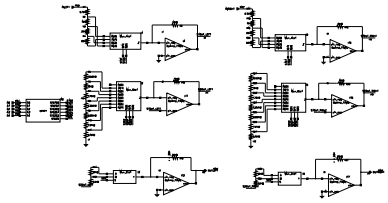

Figure 2.11: Stereo Volume Control Preamp Schematic

a non-inverting op amp with 8 separate gains and 8 resistors. Stage 3 is an inverting op amp with 2 gains and 3 resistors.

2.1.7 Stereo Volume Control PreAmplifier (VC_preamp_stereo)

This is a stereo implementation of the VC_preamp. It uses one Volctl circuit to drive the drive identical sets of gain stages for two channels. This circuit is shown in Figure 2.11.

2.1.8 Buffers (AnalogBuffer, big_buff, out_buffer, diff_in_buffer)

big_buff

This cell is designed as an output buffer for the RingRing cell. It was designed to handle at least a 120MHz signal. The ratios used are continued from the out_buffer cell, so that the first inverter has a PMOS width of 243 μm (3^5) and the second inverter has a PMOS width of 729u (3^6). For each inverter the associated NMOS is half the width of the PMOS, and all the channel lengths are 0.6 μm.

Chapter 3

Circuit Performance

3.1 Simulation Results

3.1.1 Wide-Swing OpAmp (OpAmp_FINAL)

Figure 3.1 shows the circuits used for testing the op-amp. Three primary tests were run on the operational amplifier in order to characterize its AC and DC response. The circuit containing instance I28 (described in Baker [1] p623) was used for open-loop characterization. Plots of the open-loop AC response of this amplifier are shown in Figure 3.2. DC input voltage was swept from -3 volt to +3 volt for an amplifier in the unity gain configuration. Output voltage for this test exhibits good linearity and reaches the +/-2.5 volt supply rails, as can be seen in Figure 3.3. One final test was to test the transient response of the op-amp. A step function was applied to the input, and the output rise time driving a load capacitance ($C_L = 20pF$) was observed. Step response is shown in Figure 3.4.

3.1.2 Comparator

The following simulation shows (Figure 3.5) the comparator with the V+ terminal driven by a 11 kHz sine wave (representing an audio input) and the V- terminal driven by a 200 kHz sine wave (approximately representing an input triangle wave). The resulting output seems to be a reasonable representation of pulse width modulation.

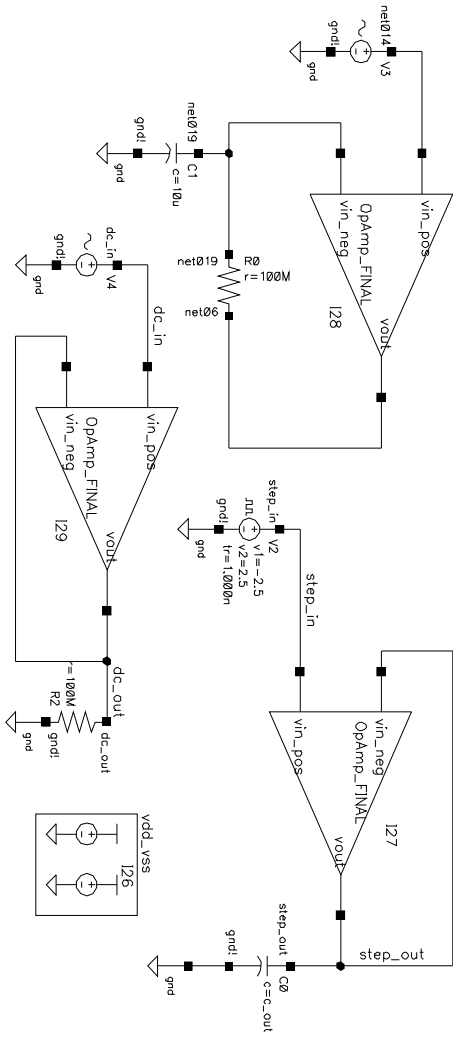

Figure 3.1: OpAmp Test Circuits

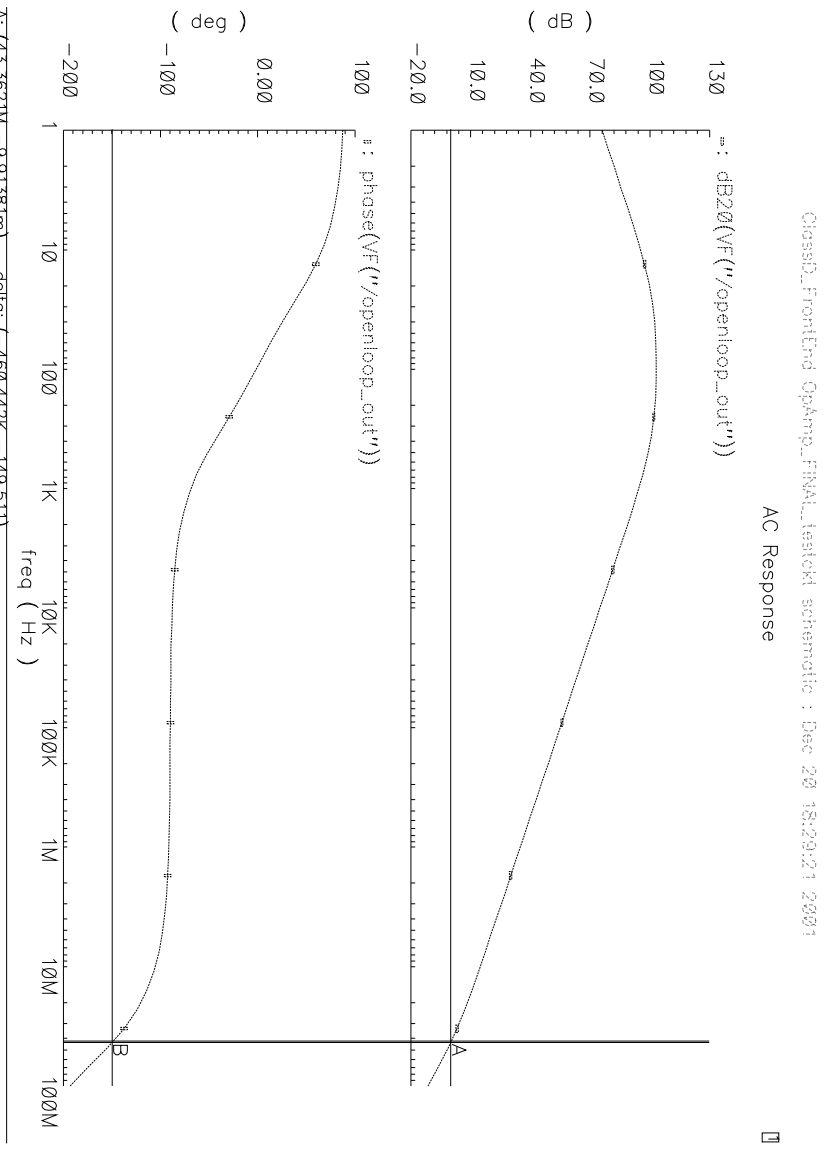

Figure 3.2: OpAmp Open Loop Simulation

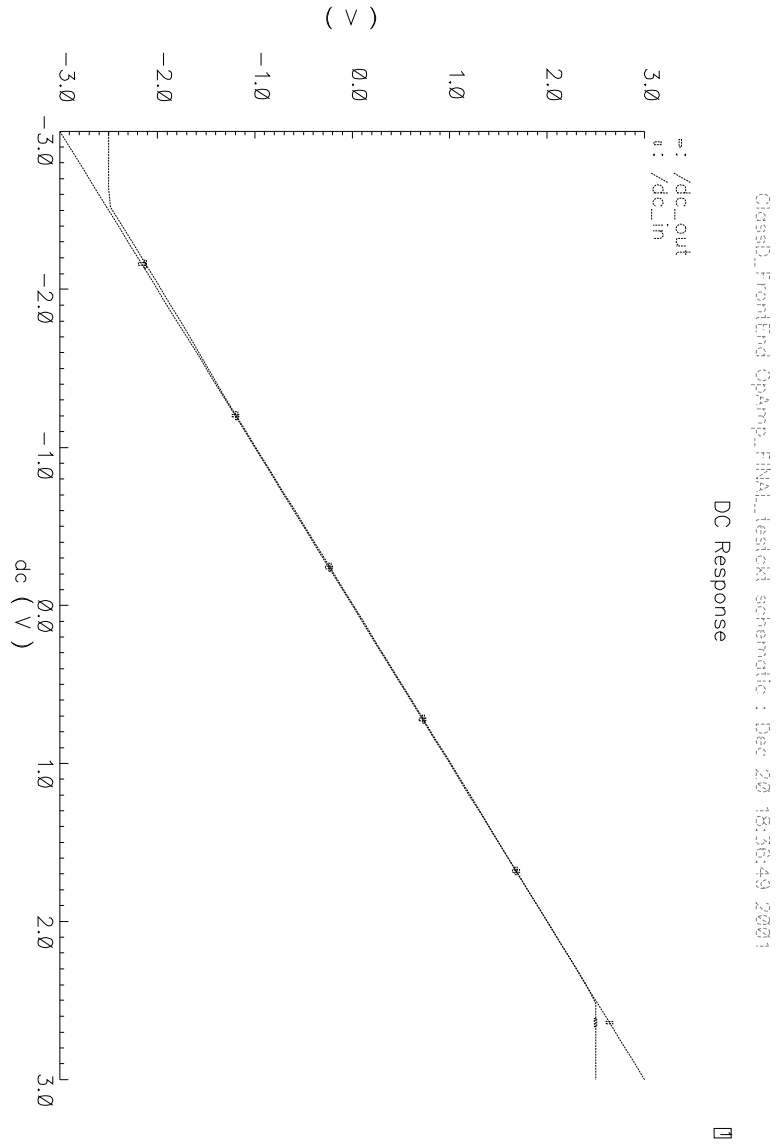

Figure 3.3: OpAmp DC Simulation

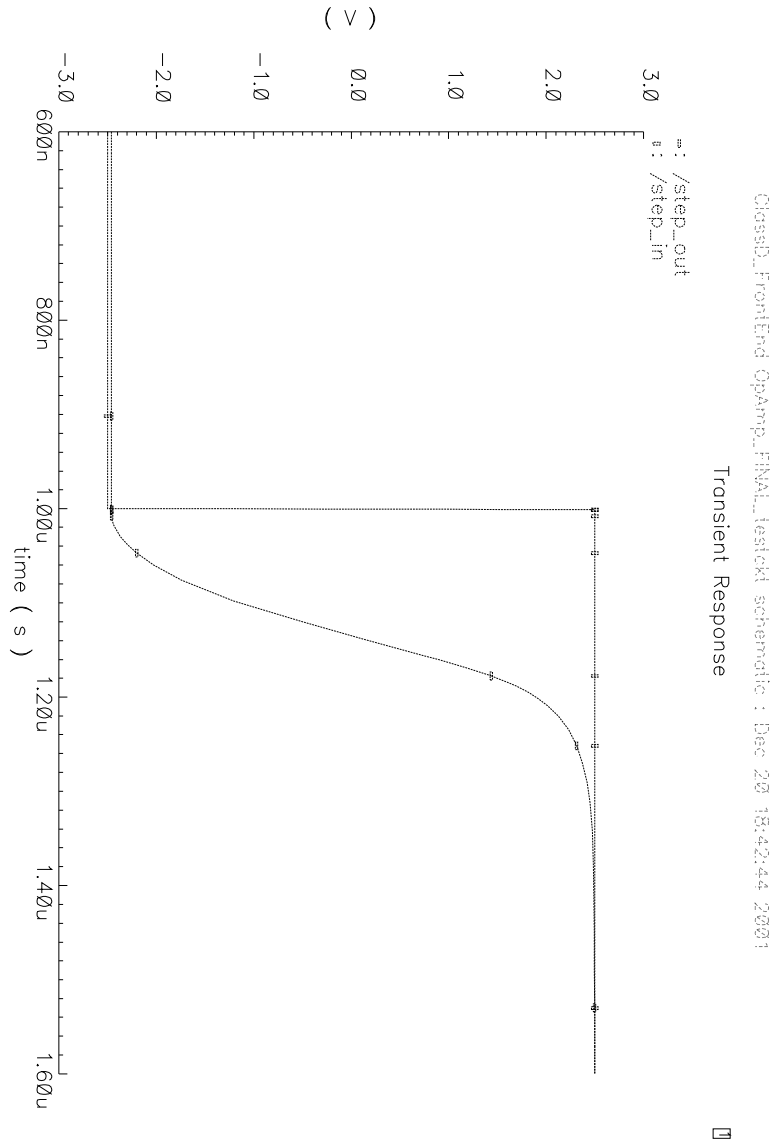

Figure 3.4: OpAmp Transient Step Simulation ($C_L = 20pF$)

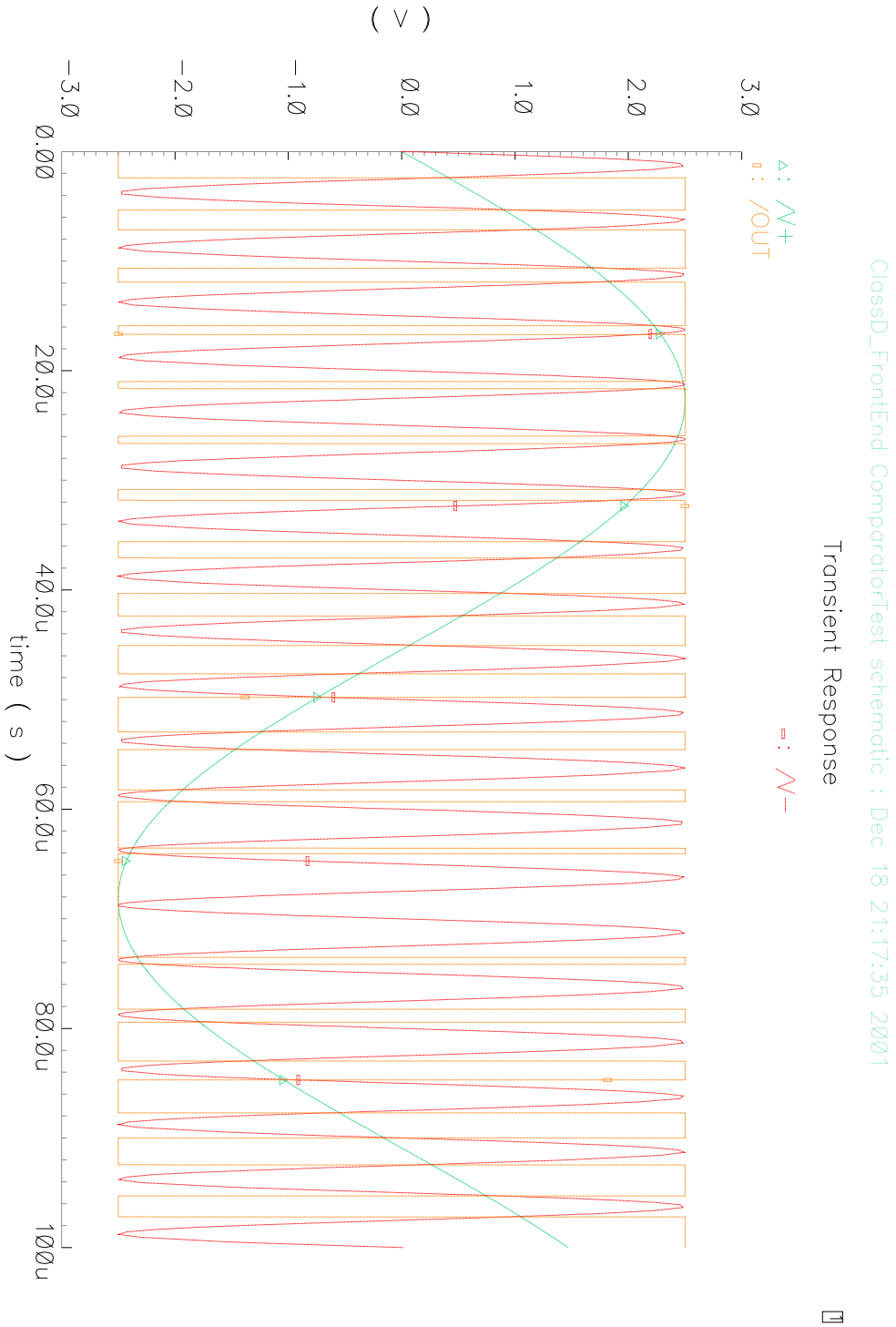

Figure 3.5: Comparator Simulation

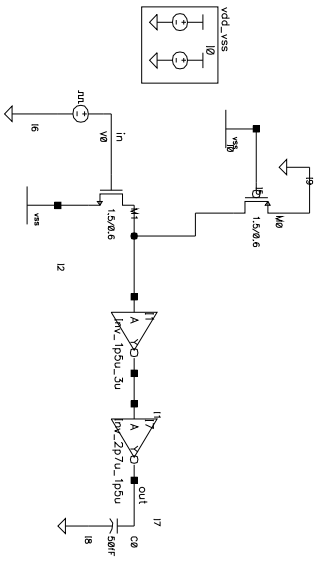

Figure 3.6: ROM Simulation Schematic

3.1.3 Volume Control Logic (volctrl)

VC_ROM

The test circuit in Figure 3.6 is used to illustrate the theory behind the ROM. A pull up, pull down, and the output drivers are included to illustrate the workings of one ROM line. As can be seen in Figure 3.7 from the simulation, the ROM works as expected. It is high when the pull down is inactive, and low when the pull down is active.

Line Driver

This simulation shows the line driver being cycled so that the outputs go active in reverse order from line 31 to line 0, and back to line 31. The selection lines are not shown for the sake of simplicity. It is important to note that lines only go high when they are supposed to, and go back to -2.5 volt when not selected. This shows that the extra pull down fixes the problem of floating lines. The simulation results are shown in Figure 3.8.

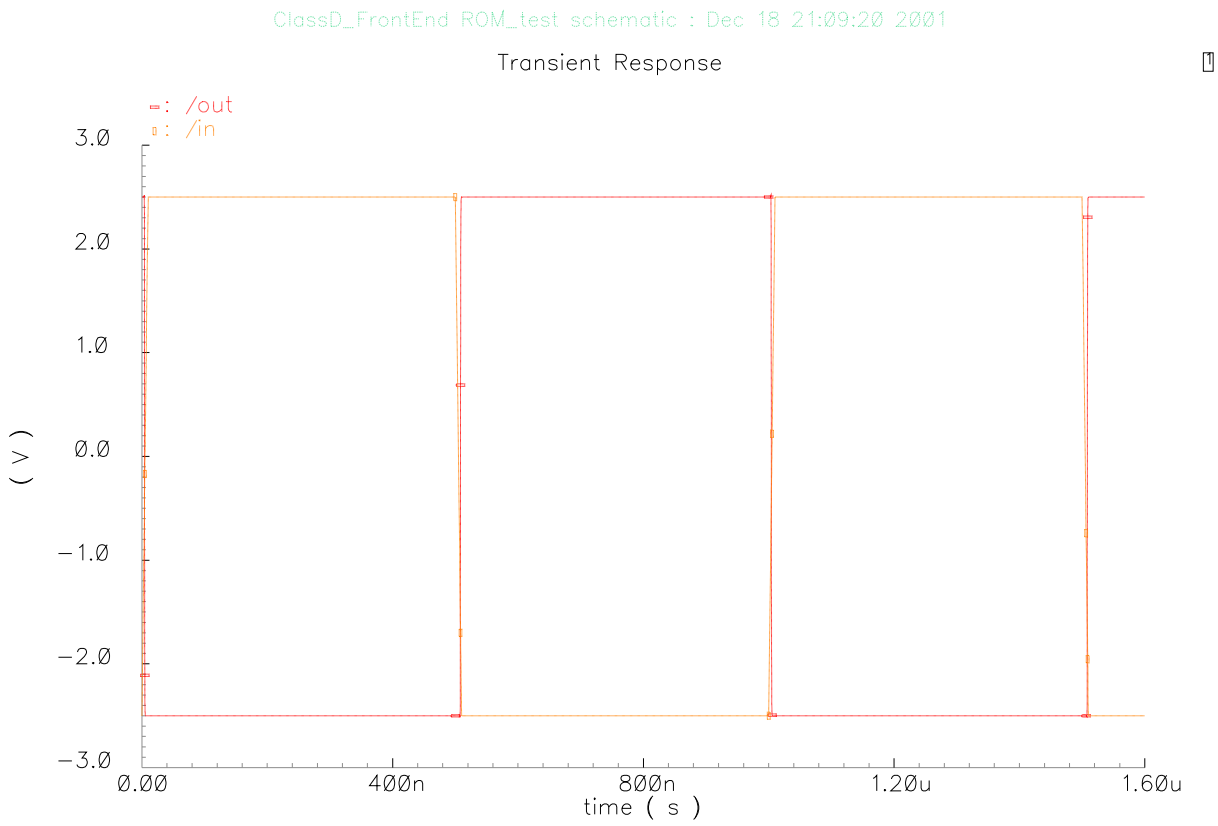

Figure 3.7: ROM Simulation Result

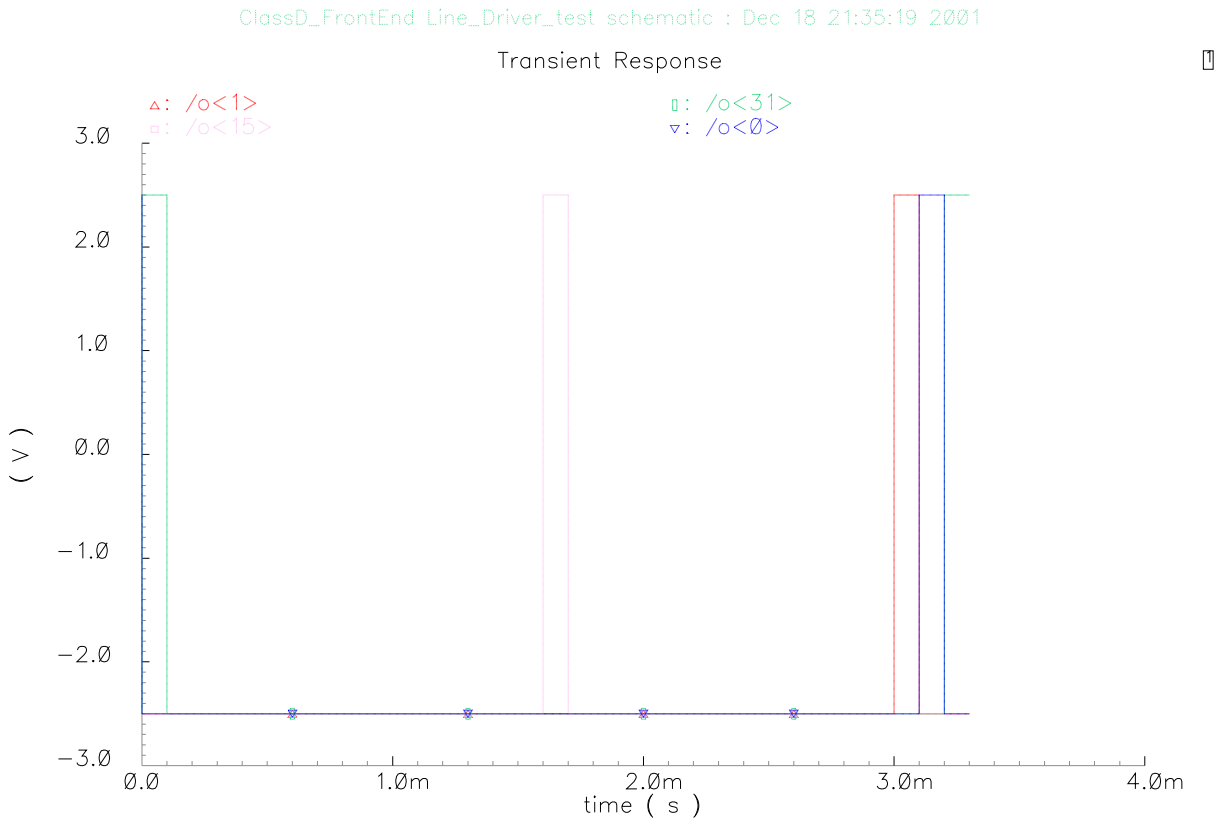

Figure 3.8: Line Driver Simulation

3.1.4 Muxes (Mux_8to1)

Figure 3.9 shows a test of the 8 to 1 mux/demux. Since this mux contains the 4 to 1 and 2 to 1 muxes, this should be sufficient to show that all of the muxes work. This simulation has two different frequency sine waves (20 kHz and 2 kHz) on inputs 6 and 7. The low bit of the select logic is changed from high to low so that first input 7 is active, then input 6 is active. Simulation results are in Figure 3.10.

3.1.5 Transmission Gate (TX_Gate)

The simulation in Figure 3.11 shows the transmission gate going from enable to disabled with a 20 kHz input sine wave. The graph demonstrates that the output is the same as the input when the transmission gate is enable and that it is floating when it is disabled. A 20 kHz input is used to show that the gate will work for the upper end of the audio spectrum.

3.1.6 Volume Control PreAmplifier (VC_preamp, VC_preamp_stereo)

The preamp test circuit (Figure 3.12) is a parametric simulation of all the possible inputs of the VC_Preamp cell. Showing that this test works should be sufficient to show that the volctrl cell works, since the volctrl cell selects drives the preamp muxes from the inputs. It should also be sufficient to show that the stereo preamp works, since the volctrl outputs should be able to drive at least two muxes. The simulation in Figure 3.13 shows the desired output with the the range of +6 dB down to -25 dB.

3.1.7 Buffers (AnalogBuffer, big_buff, out_buffer, diff_in_buffer)

This simulation is the big_buff cell being driven by the out_buffer cell and an input square wave with a frequency of 120 MHz. The big_buff is driving a 30pf load to simulate an output pin. The output is high for a sufficient time, so the buffer should be able to be driven by at least a 120MHz source.

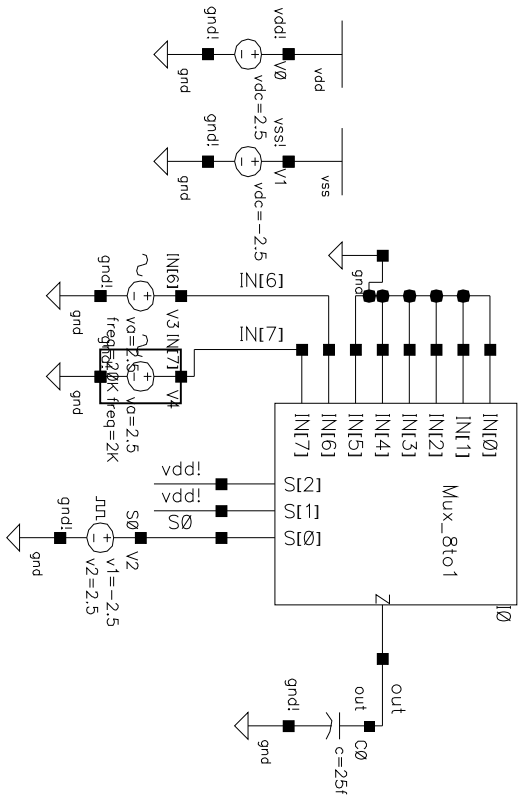

Figure 3.9: Mux Simulation Schematic

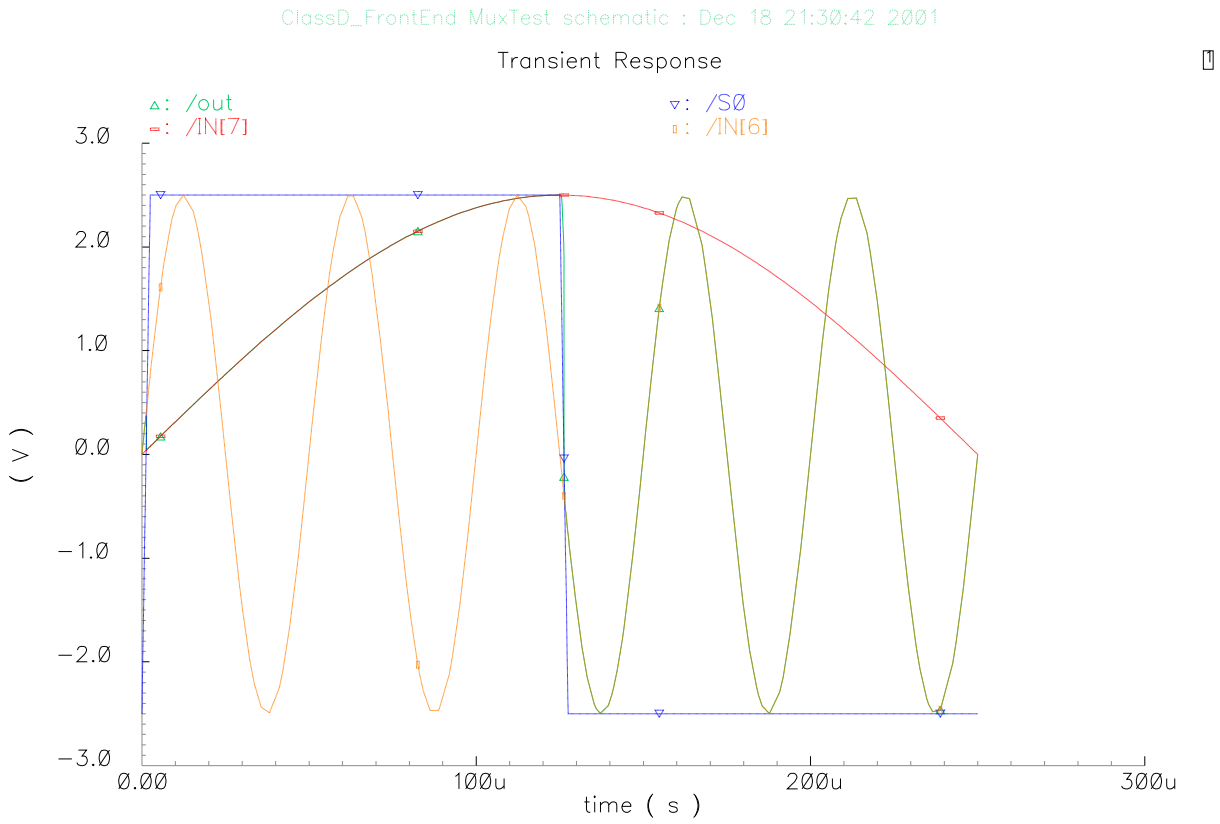

Figure 3.10: Mux Simulation Result

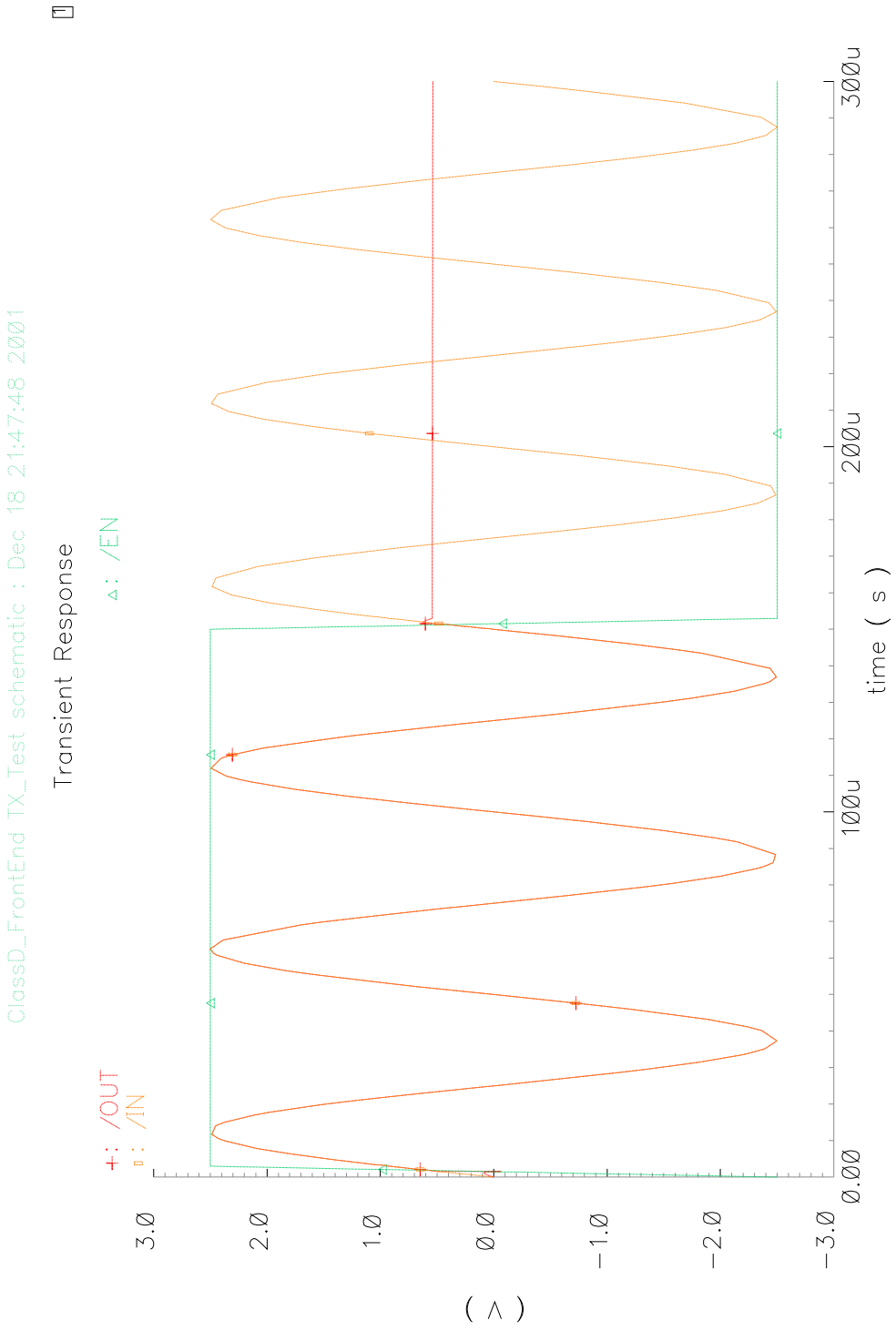

Figure 3.11: Transmission Gate Simulation Results

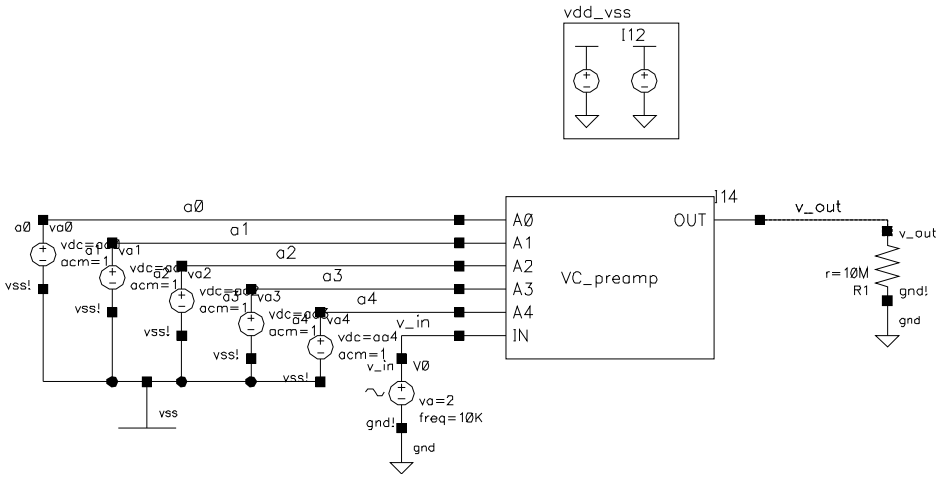

Figure 3.12: Preamp Simulation Circuit

3.1.8 Bi-Stable Oscillator (Bistable_FINAL)

The bi-stable oscillator must be characterized in terms of operating frequency and linearity of triangle wave output. A test circuit for characterization of the bi-stable is shown in Figure 3.14. Simulation results follow in Figure 3.15. The triangle wave appears reasonably linear, the frequency of operation is approximately 240 kHz, and duty cycle is approximately 50%.

3.1.9 Entire Circuit

The following circuit (Figure 3.16) was used to simulate the top-level functionality of the *Class-D Front-End*.

This circuit was tested using a 10 kHz sinusiodal input. The output was forced to drive a 20 pF load capacitance. Note that the input to the comparator is actually inverted from the input of che chip, do to the configuration of the input buffers. The PWM output is therefore 180 degrees out of phase from the chip input. This plot is shown in Figure 3.17. A closer view in Figure 3.18 shows the slight distortion on the low peak of the triangle wave, and that this has no apparent effect on the pulse width modulation.

Top-level performance has also been simulated from our extracted view. See Chapter 4.

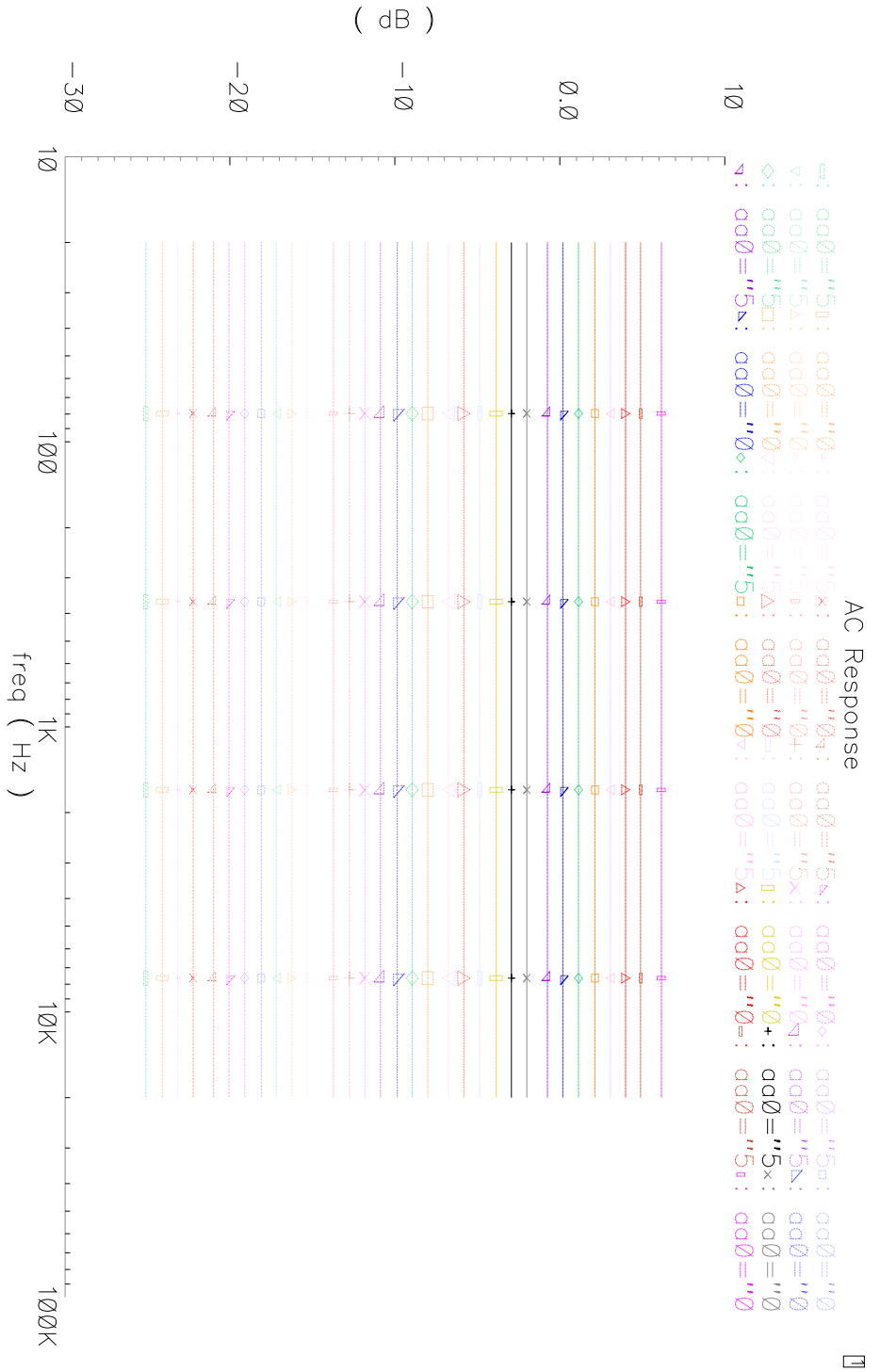

Figure 3.13: Preamp Simulation Results

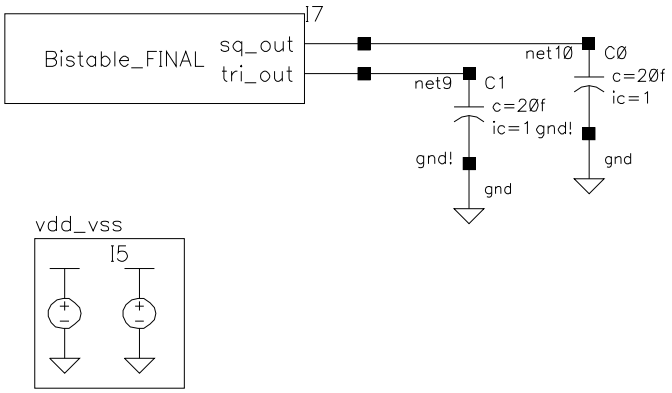

Figure 3.14: Bi-Stable Oscillator Simulation Circuit

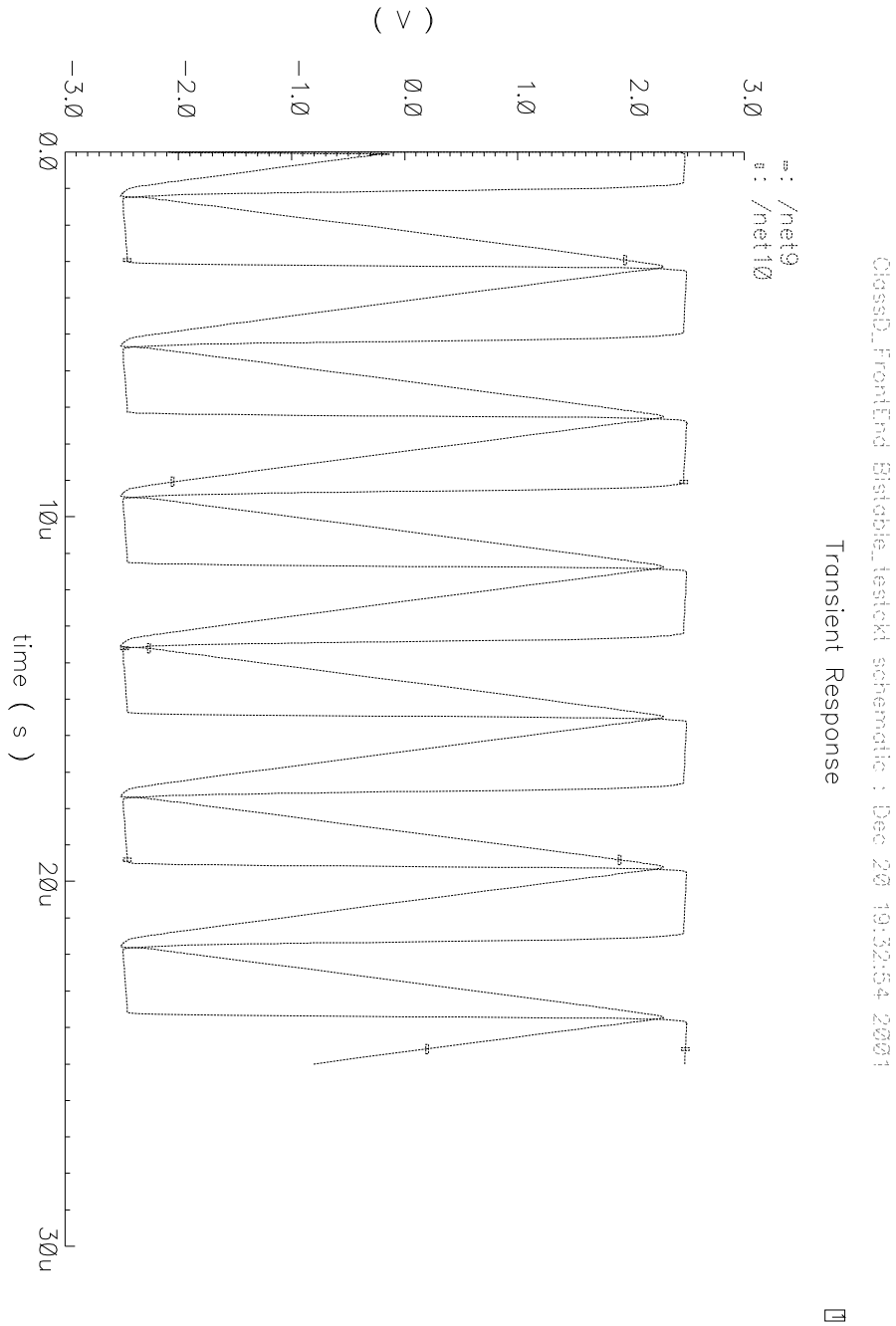

Figure 3.15: Bi-Stable Oscillator Simulation

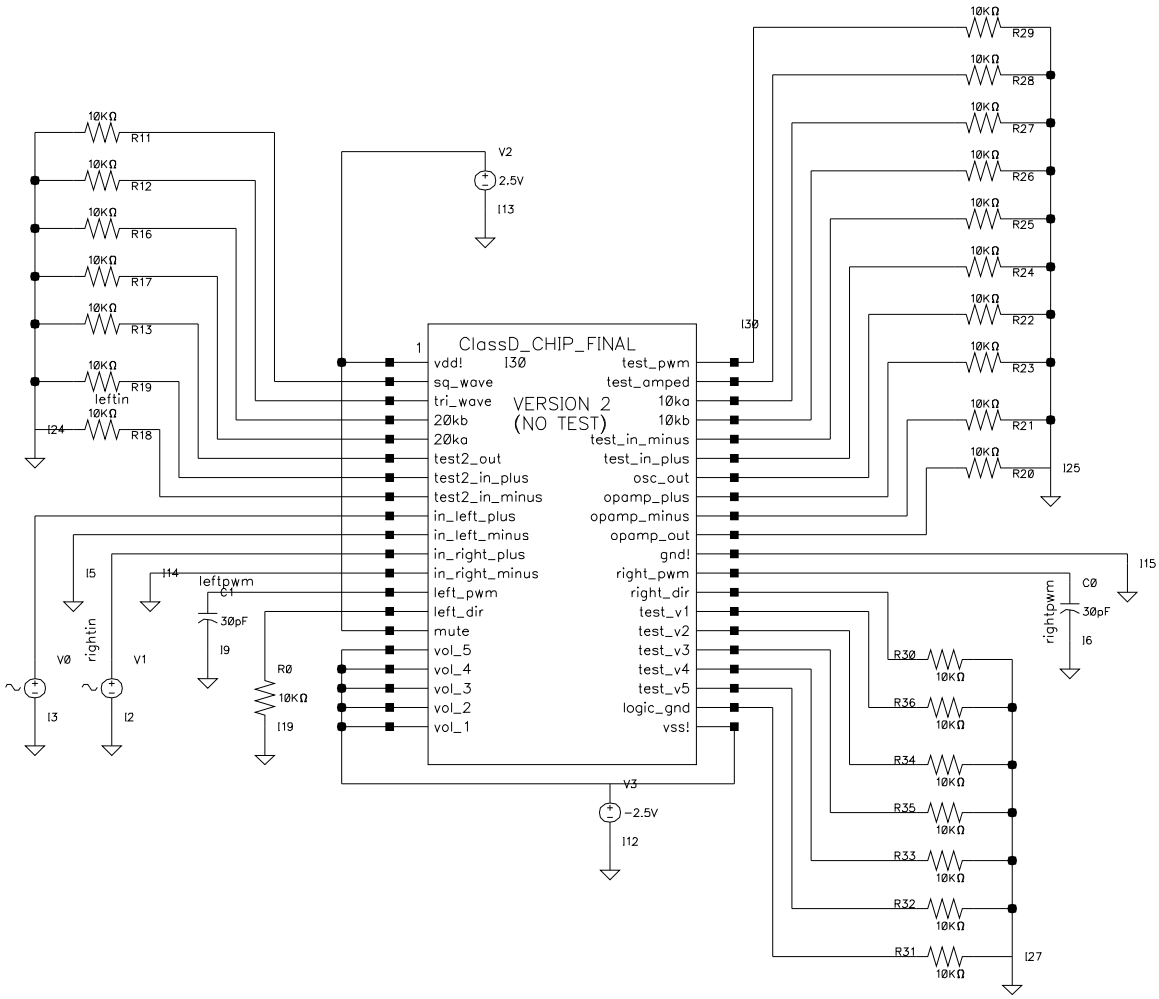

Figure 3.16: Top-Level Simulation Circuit

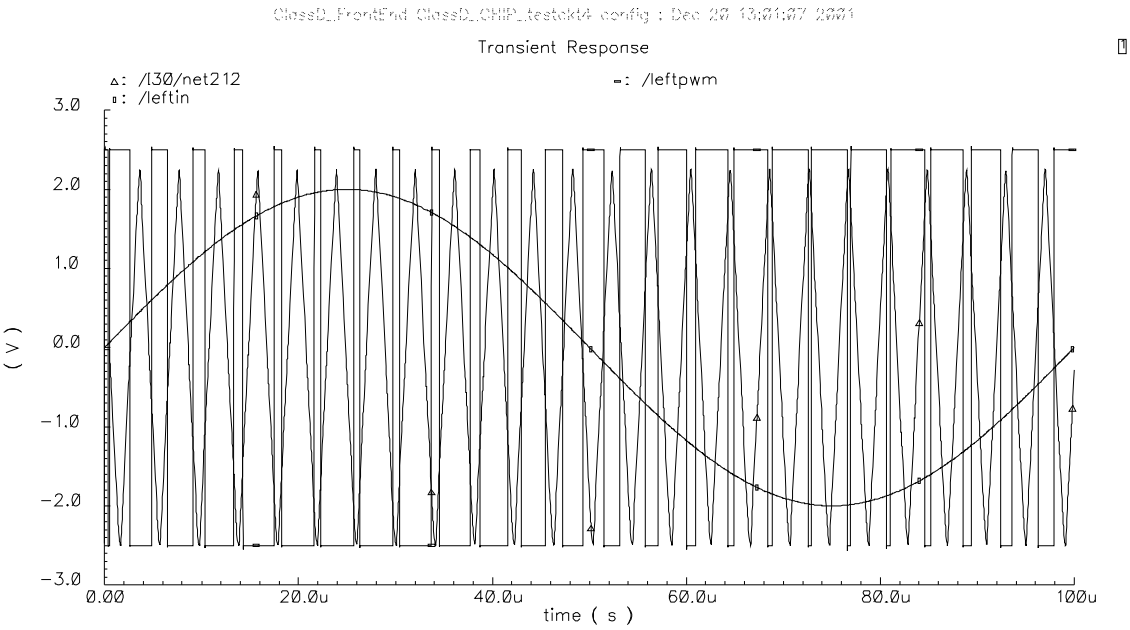

Figure 3.17: Top-Level Simulation Results

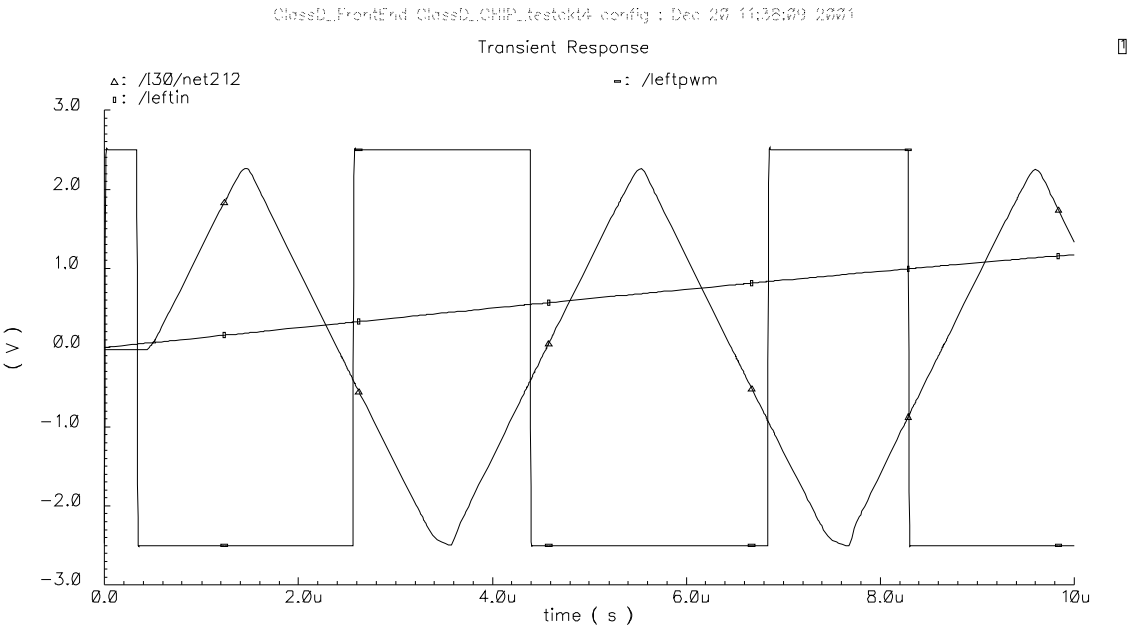

Figure 3.18: Top-Level Simulation Results

Chapter 4

Physical Design

4.1 Description of Components

For a listing of macros and layout diagrams in this project, see Table 1.2 in Chapter 1 and Appendix B, respectively.

4.1.1 Wide-Swing OpAmp (OpAmp_FINAL)

blah blah

4.1.2 Comparator

Contains a VSS guard ring around the entire structure. Drains are shared where possible.

4.1.3 Multiplexors

Mux_2to1

This cell was set up with the VSS and VDD taps next to each other. That allows the VDD and VSS sections to be isolated with full guard rings when they are instantiated in other cells.

Mux_2to1_lay2

A layout only version of the Mux_2to1 cell. This is the Mux_2to1 cell with full guard rings around the VDD and VSS sections.

Mux_4to1

This cell contains 3 instances of the Mux_2to1 cell. The instances are arranged so that the NWELLs of the instances butt together in the middle of the cell. The VSS and VDD areas have partial guard rings. The guard rings are to be completed in higher levels.

Mux_8to1

This cell contains 2 instances of the Mux_4to1 cell and one instance of the Mux_2to1 cell. The cells are arranged so that there are two NWELL areas with partial guard rings. The guard rings are to be completed in higher levels.

4.1.4 Volume Control Logic (volctr, VC_ROM)

VC_ROM

Contains the pull ups, bit patterns, and output drivers for the ROM. ROM words are isolated by guard rings in groups of two.

volctrl

A combination of VC_ROM and Line_Driver. There is a large NWELL section in the middle of the cell. The whole cell has a VSS guard ring surrounding it.

Line_Driver

The inverters for the select lines were placed on the middle part of the VSS side of the cell. Empty areas of this cell are filled with VSS taps. It was necessary to go to M3 to route some of the $\overline{A0}$ signal.

Bit0

Pull down NMOS for ROM bit value of 0.

Bit1

Represents bit value of 1 in ROM. Continues logic line and guard ring.

S1G_1

A ROM cell representing the bit pattern 11.

S1G_p1

A ROM cell representing the bit pattern 10.

S1G_p2

A ROM cell representing the bit pattern 01.

S1G_p4

A ROM cell representing the bit pattern 00.

S2G_1

A ROM cell representing the bit pattern 111.

S2G_1p4

A ROM cell representing the bit pattern 100.

S2G_1p12

A ROM cell representing the bit pattern 110.

S2G_1p25

A ROM cell representing the bit pattern 101.

S2G_1p58

A ROM cell representing the bit pattern 011.

S2G_1p77

A ROM cell representing the bit pattern 010.

S2G_1p99

A ROM cell representing the bit pattern 001.

S2G_2p23

A ROM cell representing the bit pattern 000.

4.1.5 Volume Control PreAmplifier (VC_preamp)

A combination of the cells volctrl, VC_preamp_s1_lay, VC_preamp_s2_lay, and VC_preamp_s3_lay. It has M3 on top to allow for routing of VSS and VDD.

VC_preamp_s1_lay

A layout only cell of gain stage 1 in the VC_preamp.

VC_preamp_s2_lay

A layout only cell of gain stage 2 in the VC_preamp.

VC_preamp_s3_lay

A layout only cell of gain stage 3 in the VC_preamp.

4.1.6 Stereo Volume Control PreAmplifier (VC_preamp_stereo)

A copy of VC_preamp with two instances of VC_preamp_s1_lay, VC_preamp_s2_lay, and VC_preamp_s3_lay. It has M3 on top to allow for routing of VSS and VDD.

4.1.7 Buffers (AnalogBuffer, big_buff, out_buffer, diff_in_buffer)

big_buff

Contains large output buffer inverters. Some of the routing is done in M3 to connect common drains, and to connect VSS and VDD.

4.1.8 Bi-Stable Oscillator (Bistable_FINAL)

Layout of the bi-stable consists of two op-amp cells. Reasonable aspect ratio was desired for better integration with other components. The op-amp is roughly 100 μm x μm; the large $500k\Omega$ resistor and 2 pF capacitor can conveniently be sandwiched between the two op-amps, yielding an overall aspect ratio of approximately 3:1.

4.2 Description of Physical Layout

The chip was laid out with most of the circuitry for the main circuit in the top left quadrant of the chip. A single channel test circuit was placed on the middle right side of the chip. A test op amp and a test ring oscillator were placed in the lower right portion. Much of the space not containing circuit is filled with a bypass capacitor. Top-level level layout is shown in Figure 4.1.

4.3 Floorplanning Issues

Since space was not an issue on the chip, floorplanning issues were limited. In general, it was a goal to have guard rings around cells and ample power connections. For the main circuit, the inputs come into the top part of the chip. The left PWM signal is output to the top, and the right PWM signal is output to the bottom.

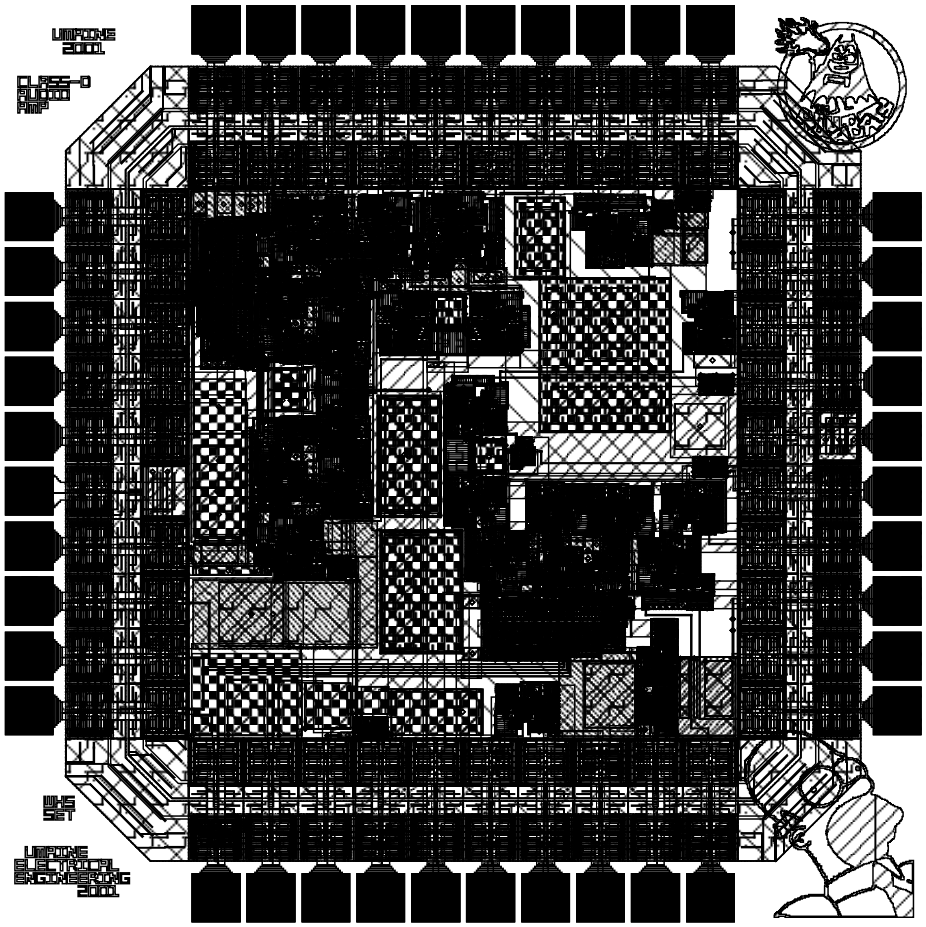

Figure 4.1: Top-Level Chip Layout

Chapter 5

Verification

5.1 Verification of Design

Several procedures were used to verify the top-level functionality of the *Class-D Front-End* project. Before layout, all components were simulated and verified functional. All higher levels cells were tied together and the output at this level was verified. During layout of the circuit, *Design Rule Checks (DRC)* were performed on individual cells. *Layout versus Schematic (LVS)* was run to verify that the circuit components generated during layout logically matched the components in the original schematic.

'The net-lists match.'

The top level layout passed DRC checking with 0 errors.

However, one problem was noted during top-level simulation. When all test circuitry that was included on chip was added to our top-level simulation, Cadence/Spectra would be unable to converge on a DC solution. If these circuits were removed from the schematic, the chip would simulate at the top level. If these circuits were removed from layout, the analog extracted top-level simulated.

5.2 Simulations with Parasitic Extractions

A simulation of the top-level design was simulated from extraction. This means that an equivalent electrical circuit (including certain parasitics) was extracted from the physical layout, and then ran through simulation. If the circuit simulates from this extracted version, there is a high likelihood that it will work upon delivery.

5.2.1 Top-Level Circuit

The following circuit (Figure 5.1) was used to simulate the top-level functionality of the parasitic *Class-D Front-End*.

The test circuit is identical to that used for the non-extracted top-level simulation.

This circuit was tested using a 10kHz sinusiodal input. The output was forced to drive a 20 pF load capacitance. Note that the input to the comparator is actually inverted from the input of che chip, do to the configuration of the input buffers. This plot of the analog extracted view is shown in Figure 5.2.

Figure 5.3 shows a close-up view of the waveforms. Little difference can be seen between the analog extracted with parasitics and the original 'ideal' design schematic, shown previously in Figure 3.18.

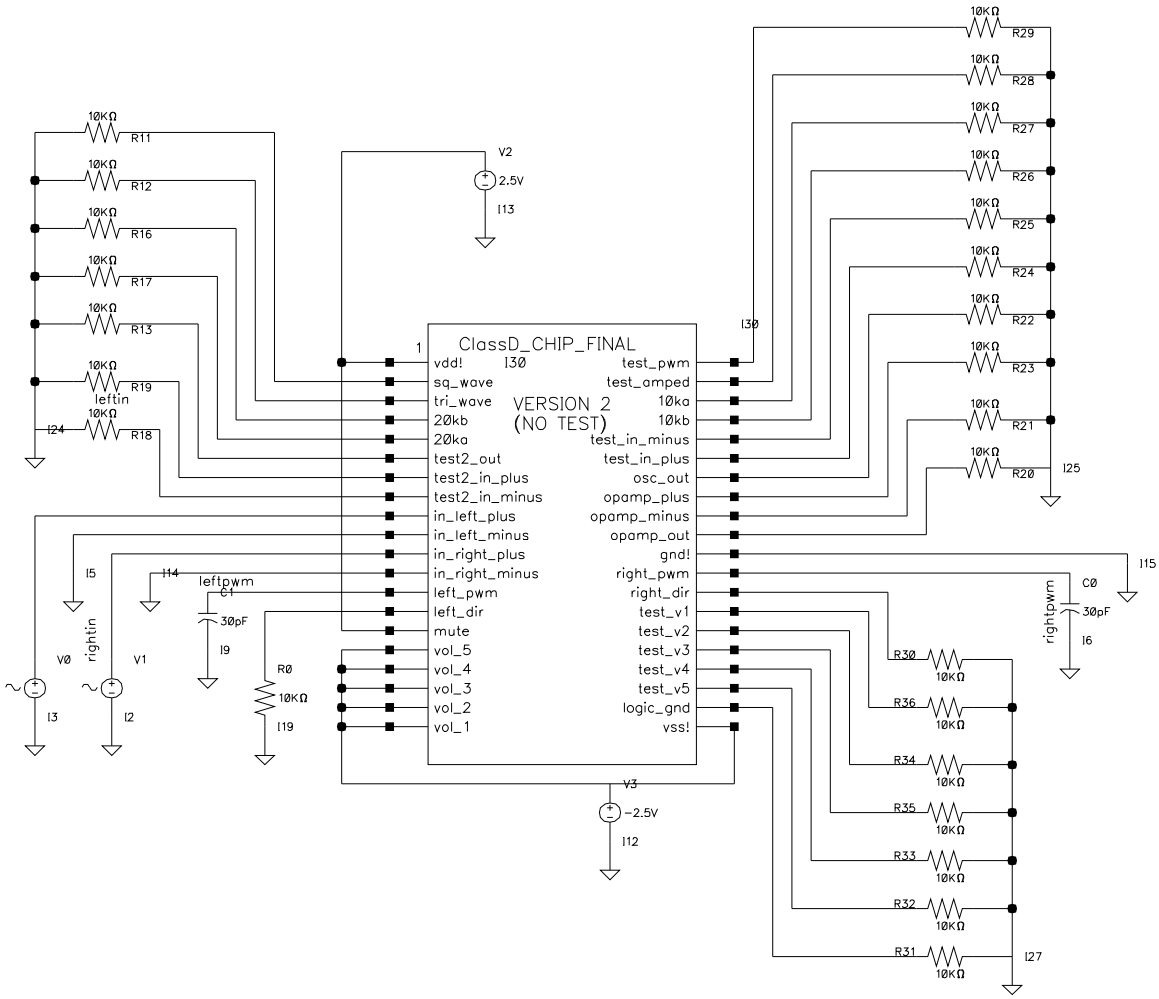

Figure 5.1: Top-Level Simulation Circuit

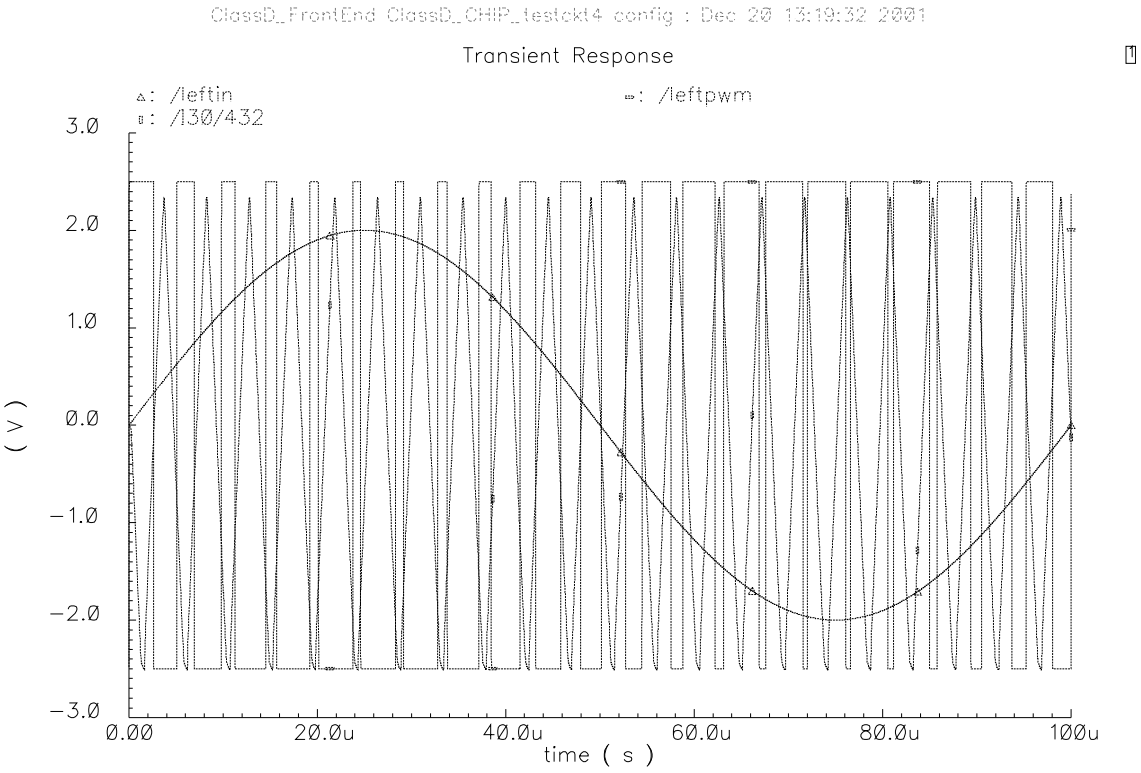

Figure 5.2: Top-Level Simulation Results (Extracted)

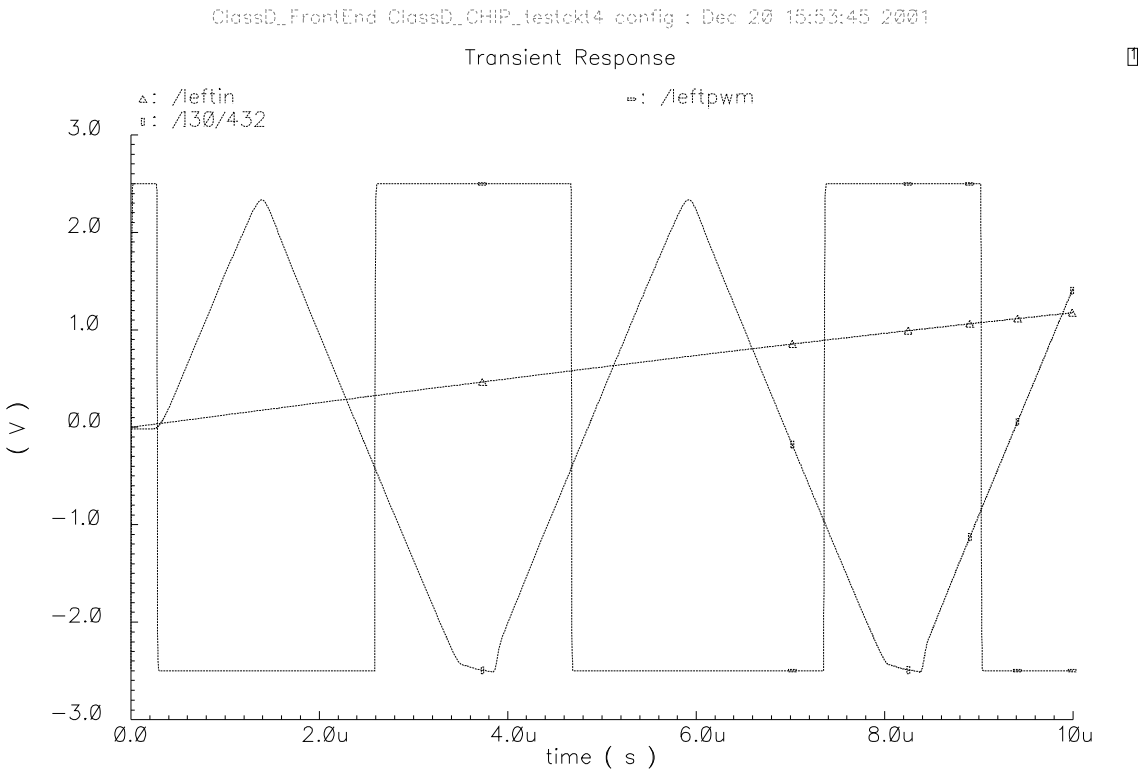

Figure 5.3: Top-Level Simulation Results Zoom (Extracted)

Chapter 6

Test

6.1 Measurement Methodology

Several components of the design were included on-chip and pinned-out for test purposes after fabrication. A complete PWM stage, op-amp, comparator, bistable, VC_Preamp, and test resistors are among the cells ready to be tested. The main circuit of this design will also be characterized to verify that it meets the specifications outlined in Table 1.1.

6.2 Test & Characterization Procedures

Seven tests are described in the following sections whichv outline a test procedure to determine the functional characteristics of the fabricated design.

6.2.1 Test 1: Static Power Dissipation

This is the simplest test of chip functionality. From the results of this test, we can determine if there are any Vdd or Vss shorts to ground, and get a rough idea if the fabricated chip compares to the simulated design.

Equipment

- (2) Agilent E3642A DC Power Supplies
- (1) Kiethley 486 Picoammeter

- (1) Kiethley 2000 Multimeter

Procedure

- Tie output pins to dummy load of 100k, input pins to ground.
- Ramp power rails Vdd=+2.5 volt, Vss=-2.5 volt up slowly, observing current draw from power suplies.
- If current draw is excessive, suspect shorts in circuit design or faulty test specimen.
- If current draw is not excessive, compare current draw from supplies and static power dissipation with simulated values.

Results

Testing scheduled for Summer 2002...

6.2.2 Test 2: Resistor Characterization

This test characterizes on-chip resistors with respect to temperature and process variation. Test resistors (Ra=10k on pins 37-38, Rb=20k on pins 4-5) were included in the final design for comparison between the fabricated and expected resistor values.
Testing scheduled for Summer 2002...

6.2.3 Test 3: Bistable Characterization

Equipment

- (2) Agilent E3642A DC Power Supplies
- (1) Kiethley 486 Picoammeter
- (1) Kiethley 2000 Multimeter
- (1) Yokogawa DL7100 Digital Oscilliscope
- LabView data capture system

Procedure

- Probe Bistable test circuit outputs (pin 2-3), no inputs needed
- Vdd=+2.5 volt, Vss=-2.5
- Capture Bistable Oscillator square and triangle waveforms.
- Characterize waveforms using time and frequency domain techniques.

Results

Preliminary captures of the Bistable Oscillator waveforms are included below in Figures 6.1 and 6.2. Both waveforms are consistent with simulated results, however there is significant nonlinearity in the triangle wave output. Further investigation is needed to determine its origin.

6.2.4 Test 4: Volume Control Characterization

Equipment

- (2) Agilent E3642A DC Power Supplies
- (1) Agilent 33250A 80MHz Function/Arbitrary Function Generator
- (1) Kiethley 2000 Multimeter
- (1) Yokogawa DL7100 Digital Oscilliscope
- Setup for 5-bit digital input
- LabView data capture system

Procedure

- Apply 1 volt test signal at volume test circuit input.
- Set 5-bit input to different values.
- Observe output voltage level.
- Calculate voltage gains for different 5-bit inputs; compare with expected gains.

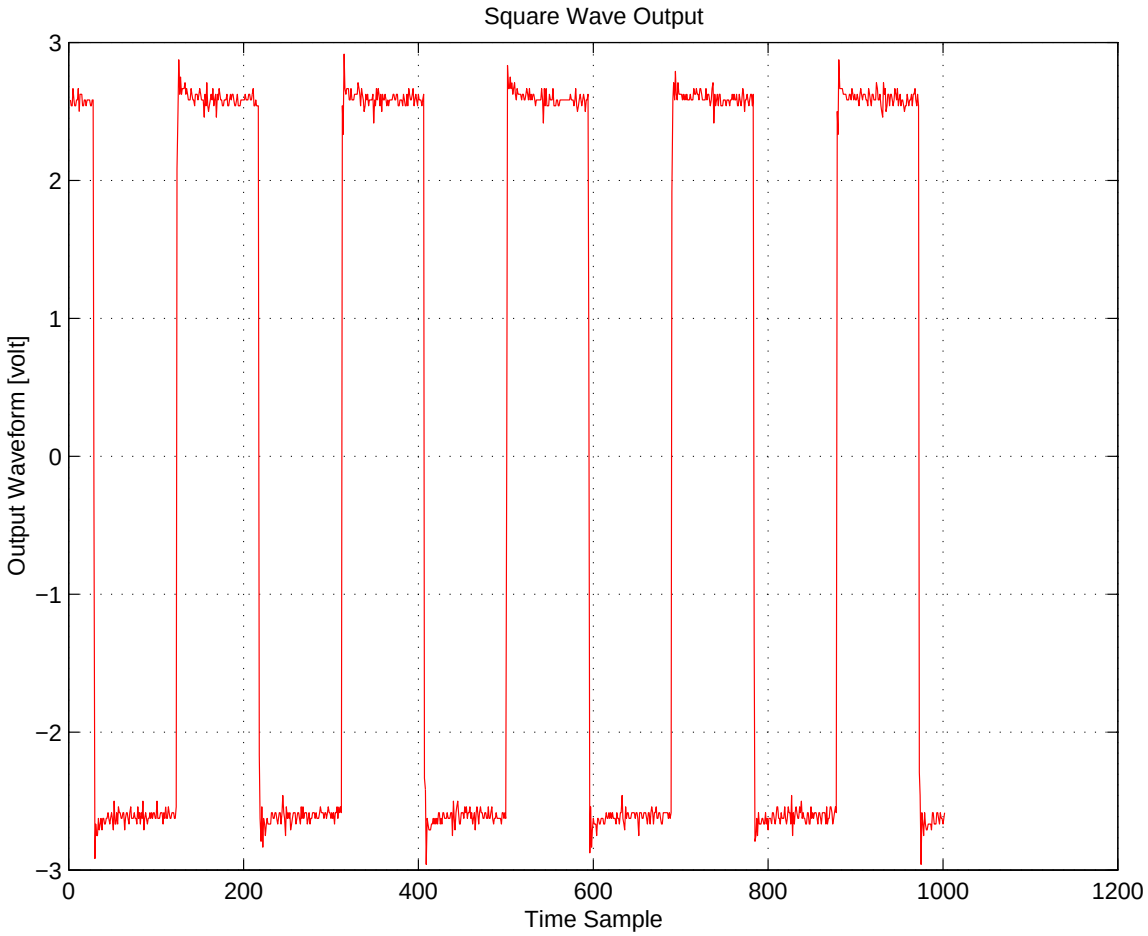

Figure 6.1: Bistable Square Wave Capture

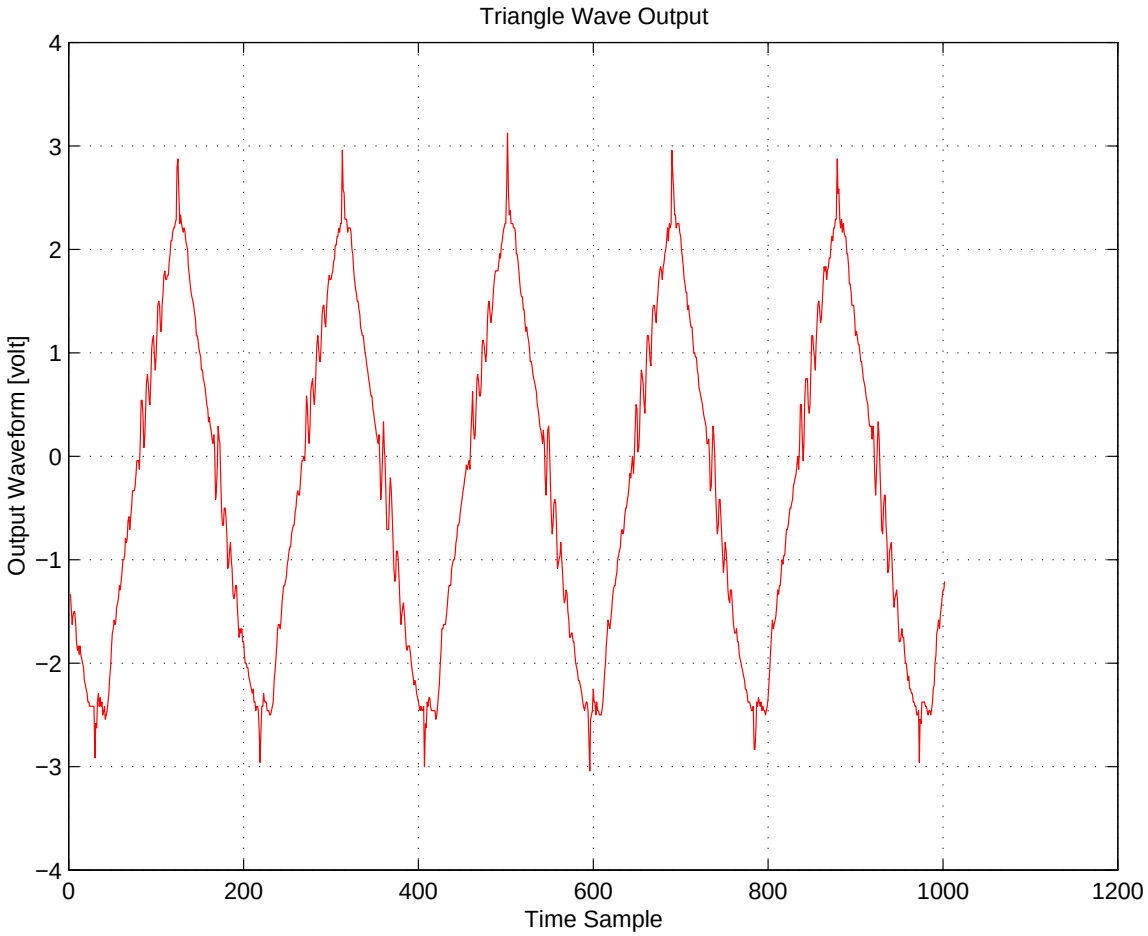

Figure 6.2: Bistable Triangle Wave Capture

Results

Testing scheduled for Summer 2002...

6.2.5 Test 5: Single Channel Frontend Circuit Test

A single channel test circuit including a complete PWM generation stage was included in the design as a test of functionality. This test will demonstrate the capabilities of the differential signal preamp and the comparator in conjunction with a bistable oscillator for PWM generation.

Equipment

- (2) Agilent E3642A DC Power Supplies
- (1) Agilent 33250A 80MHz Function/Arbitrary Function Generator
- (1) Yokogawa DL7100 Digital Oscilliscope
- LabView data capture system

Procedure

- Set input signal at pins 35-36
- Vdd=+2.5 volt, Vss=-2.5
- Capture output at pin 39 (preamped signal) and at pin 40 (PWM output).
- Characterize waveforms using time and frequency domain techniques.

Procedure

The following Figures 6.3 and 6.4 show PWM output with a test sine input of 10 kHz. These initial tests show that a PWM stage does work as expected. Further characterization is neccessary and will be performed during Summer 2002.

6.2.6 Test 6: Operational Amplifier Characterization

Testing scheduled for Summer 2002...

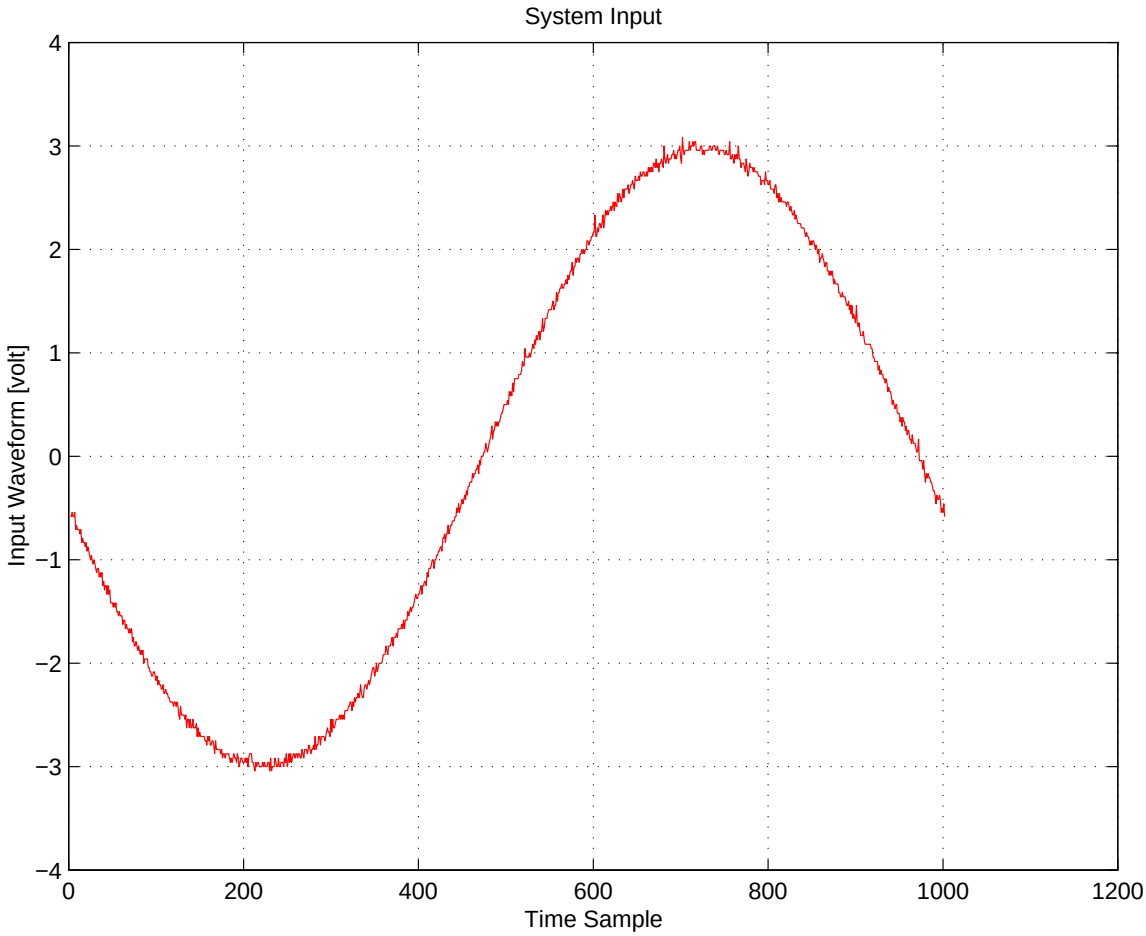

Figure 6.3: 10 kHz Sine Input to PWM Stage

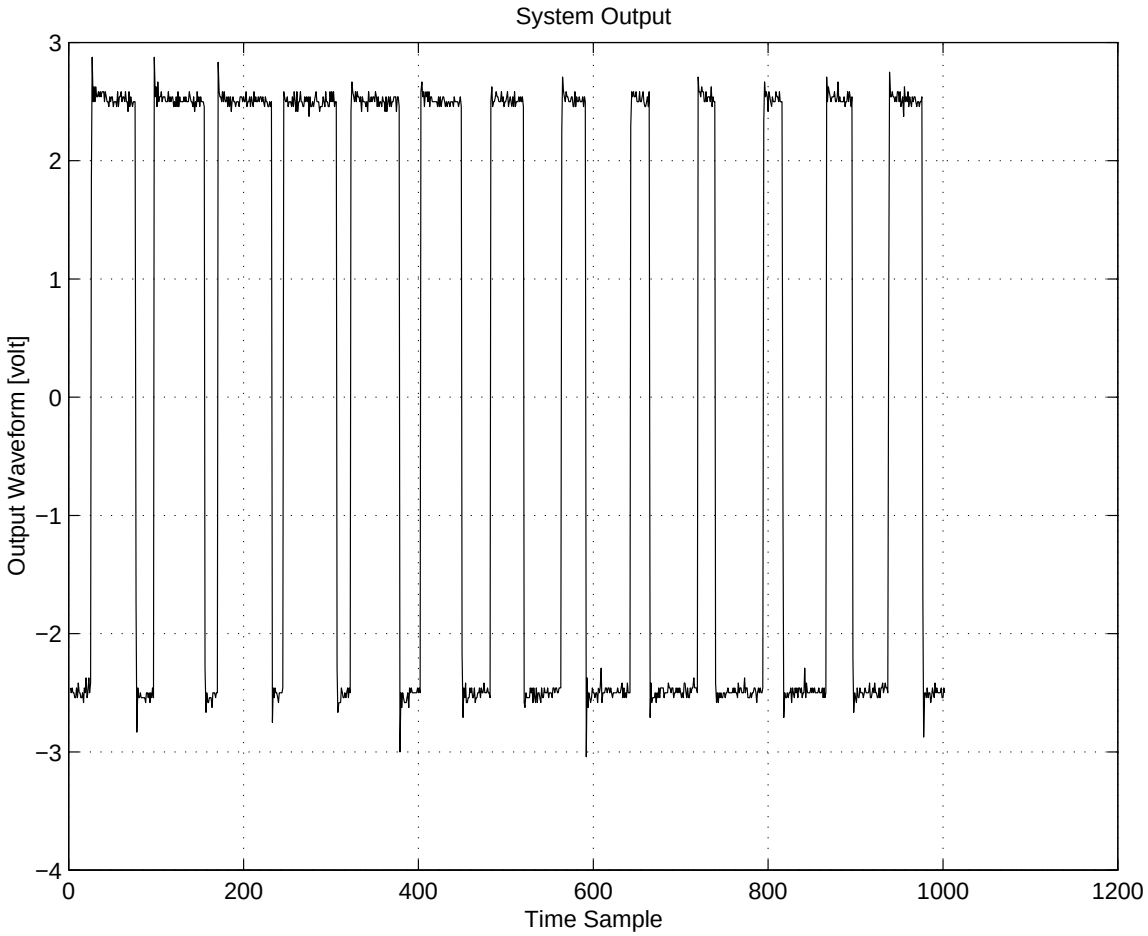

Figure 6.4: PWM Stage Output

6.2.7 Test 7: Overall System Test

As a final test the output of the stereo *Class-D Front-End*, the outputs can be used to drive high power LMD18201 H-Bridges from National Semiconductor. In theory the outputs can be used to drive any H-Bridge system, but this chip was designed around the LMD18201. A test system has been constructed and is shown below. Figure 6.5 shows the LMD18201 on a PCB with input connections for the high power voltage rails and PWM signal. Figure 6.6 shows the complete test setup, including high voltage power suply.

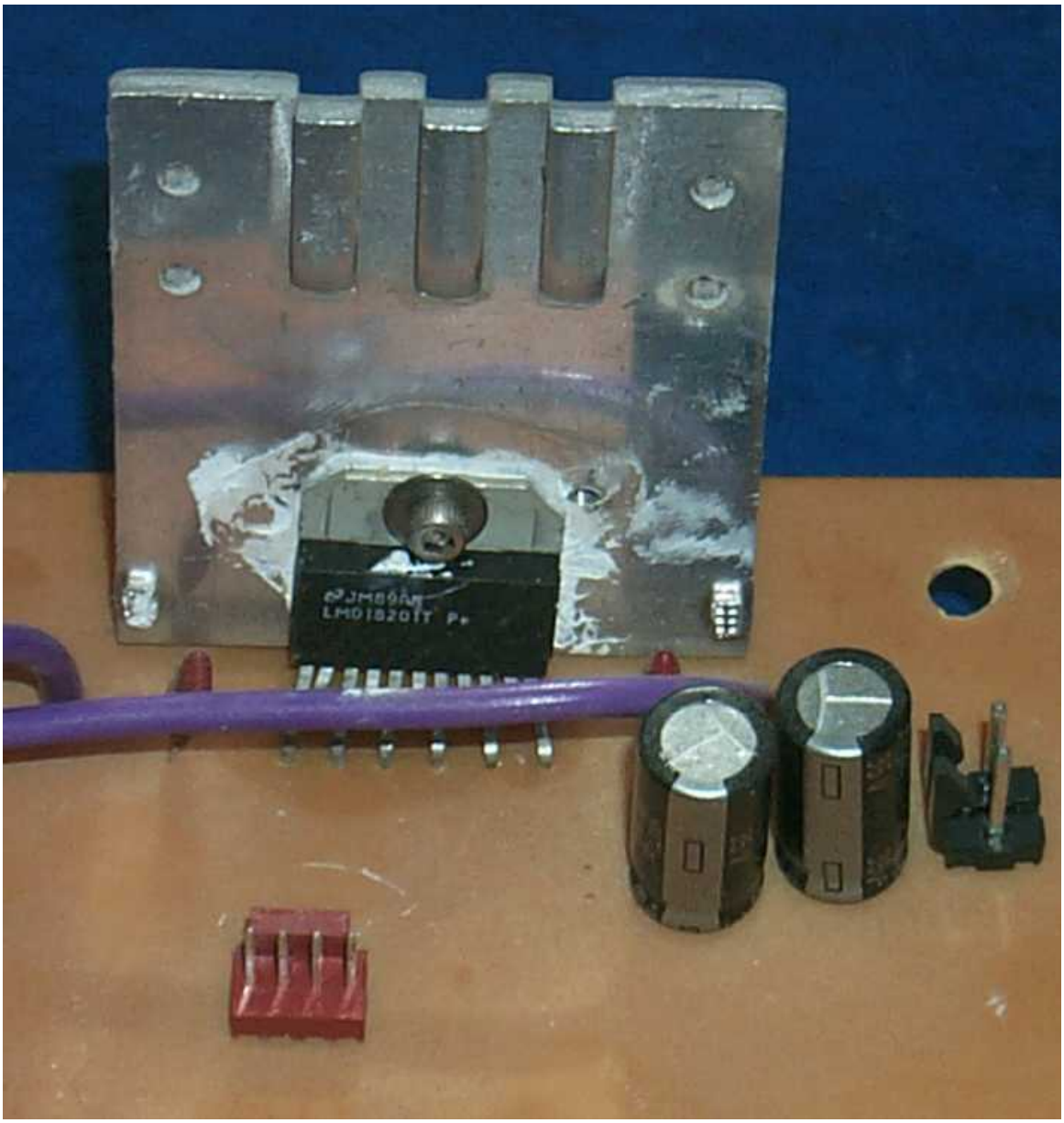

Figure 6.5: LMD18201 Monolithic H-Bridge

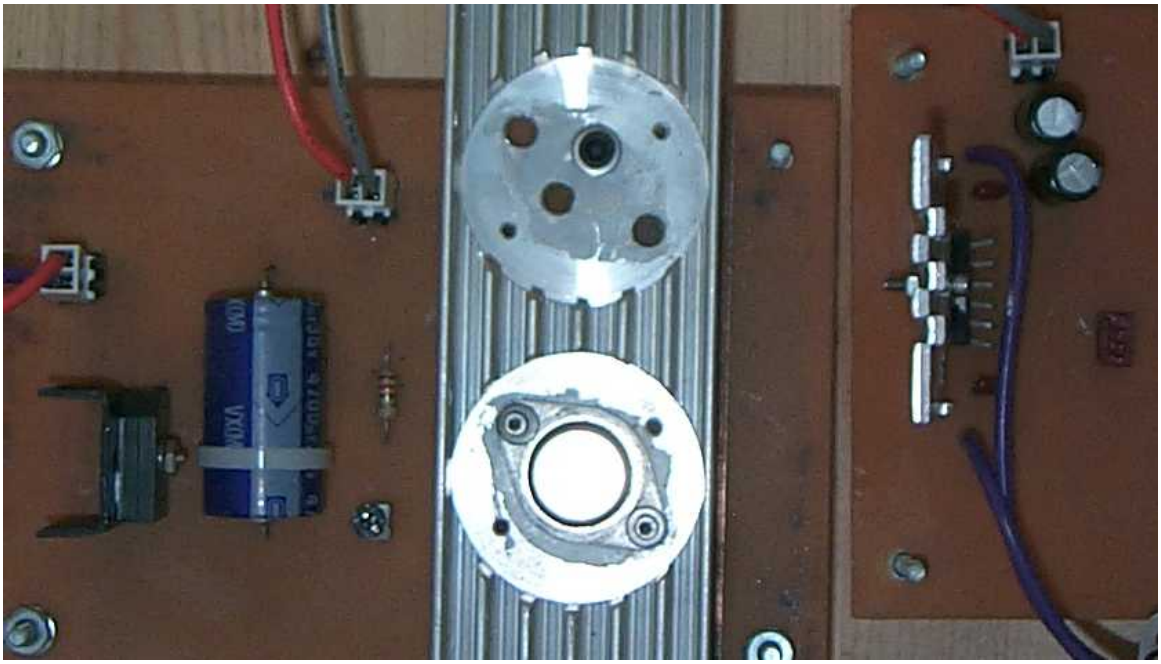

Figure 6.6: Overall System Test Setup

Chapter 7

Summary & Conclusions

7.1 Comparison of Simulated and Experimental Results

So far only initial testing has been run on the fabricated design. These initial tests of the bistable oscillator and PWM stage show that actual output is in accordance with simulated results. See Chapter 6.

7.2 Suggested Improvements

Although no experimental data has been gathered, it is likely that this design would benefit greatly from fully-differential internal circuitry. Differential topology would enhance dynamic range, reduce harmonic distortion, and increase rejection of substrate coupled noise.

One other possible improvement would be a more linear triangle wave oscillator. The bistable circuit could give better results using different components. The lesser linearity of the bottom 'point' of the waveform may degrade the PWM output quality.

Characterization of the fabricated design and analysis of experimental results, have shown that the following improvements would improve design performance:

Table 7.1: Suggested Improvements

- Coming soon...

Table 7.2: Time Estimates

	Estimated Hours	
Task	Wayne	Steve
Circuit Design	100	82
Class Time	45	45
Layout	50	102
DRC Process	8	10
LVS Process	12	16
Top-Level Sim	30	8
Extracted Sim	10	2
Documentation	30	20
TOTAL	285	285

Estimated Total Time, 570 hours.

7.3 Quantization of Fun Relating to ECE547 Project

Experimental results have shown that Wayne and Steve are having far more fun learning about VLSI design than control specimens that have not been exposed to VLSI design. Further experimental data will be collected in Spring 2002 to allow better modeling of the fun coefficient.

7.4 Estimate of Time Spent on Project

Table 7.2 lists estimated time spent on different project tasks.

Prologue

Steven Eugene Turner

Steven Eugene Turner is in his first year of graduate school, working towards an M.S. in Computer Engineering. He graduated from UMaine in May of 2001 with a double major in Electrical and Computer Engineering. He is a member of Eta Kappa Nu, Tau Beta Pi, and IEEE.
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Wayne Homer Slade, Jr.

Wayne is a candidate for the Master of Science in Electrical Engineering Degree from the University of Maine. Wayne graduated in December 2000 with a Bachelors of Science in Electrical Engineering. Wayne's academic interests include VLSI, Neural Network Modeling, Intelligent Systems, and Remote Sensing. Wayne is a member of IEEE and the Eta Kappa Nu.
wsladeeece.maine.edu

Bibliography

[1] R. Jacob Baker, Harry W. Li, and David E. Boyce. *CMOS Circuit Design, Layout, and Simulation.* IEEE Press, New York, NY, 1998.

[2] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits, Fourth Edition.* Oxford University Press, New York, NY, 1998.

Appendix A

Schematics

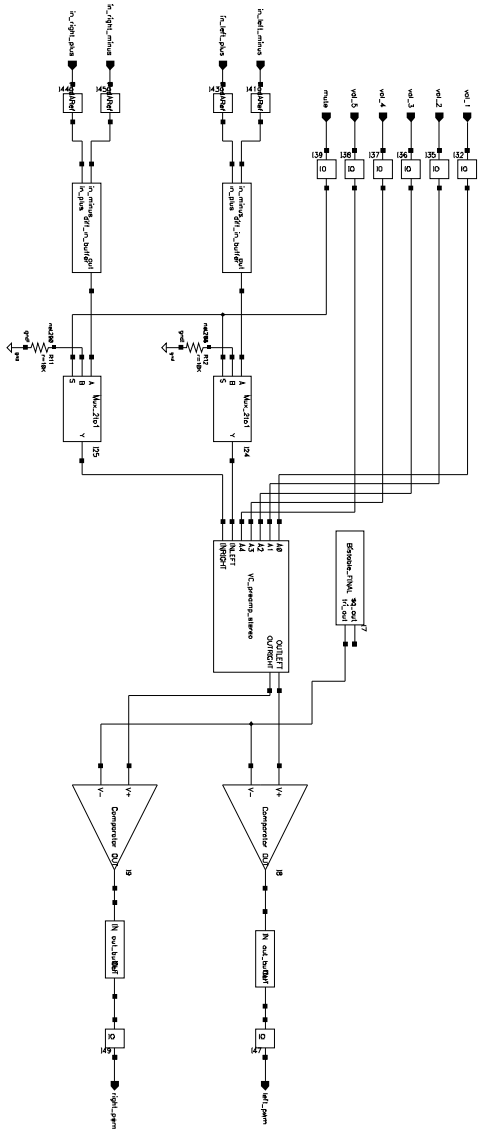

Figure A.1: Top Level Schemetic (Meat and Potatoes)

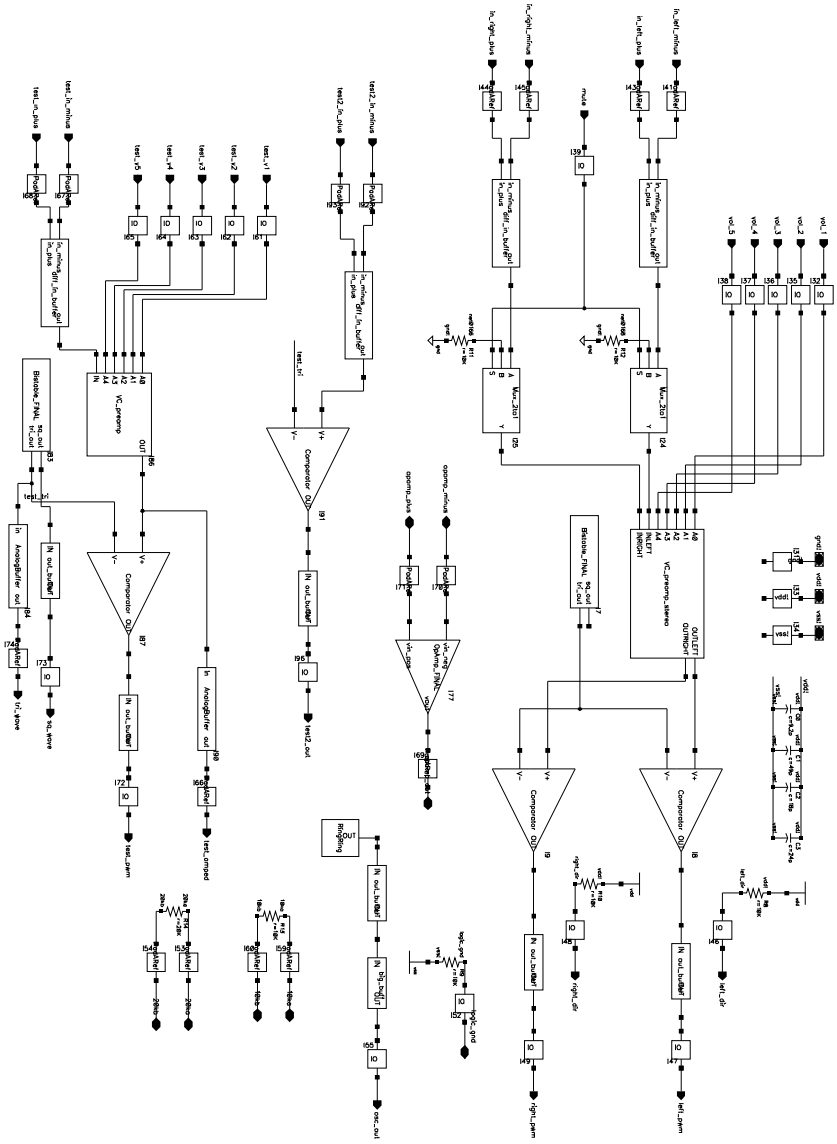

Figure A.2: Top Level Schemetic (Including Test Ckt)

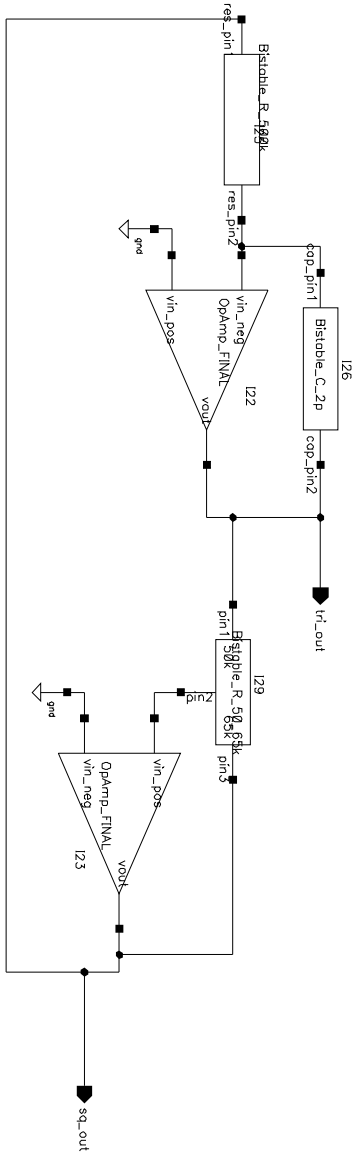

Figure A.3: Bi-stable Oscillator Schematic

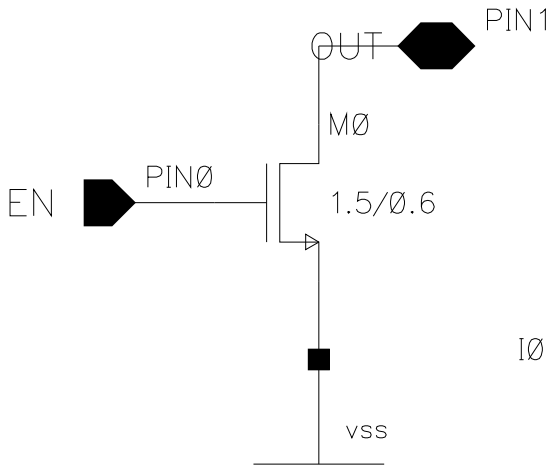

Figure A.4: Bit Zero Schematic

Figure A.5: Bit One Schematic

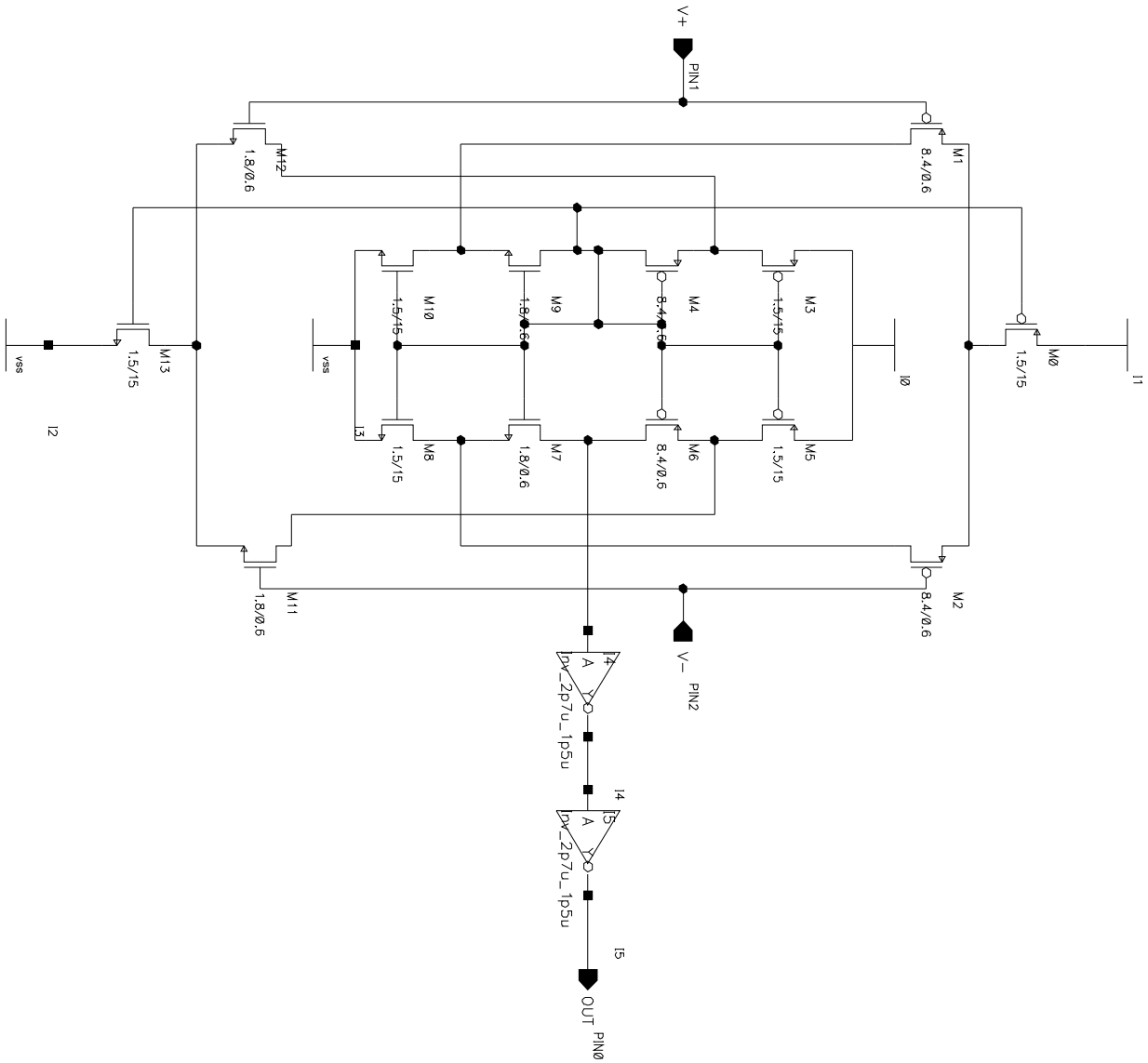

Figure A.6: Comparator Schematic

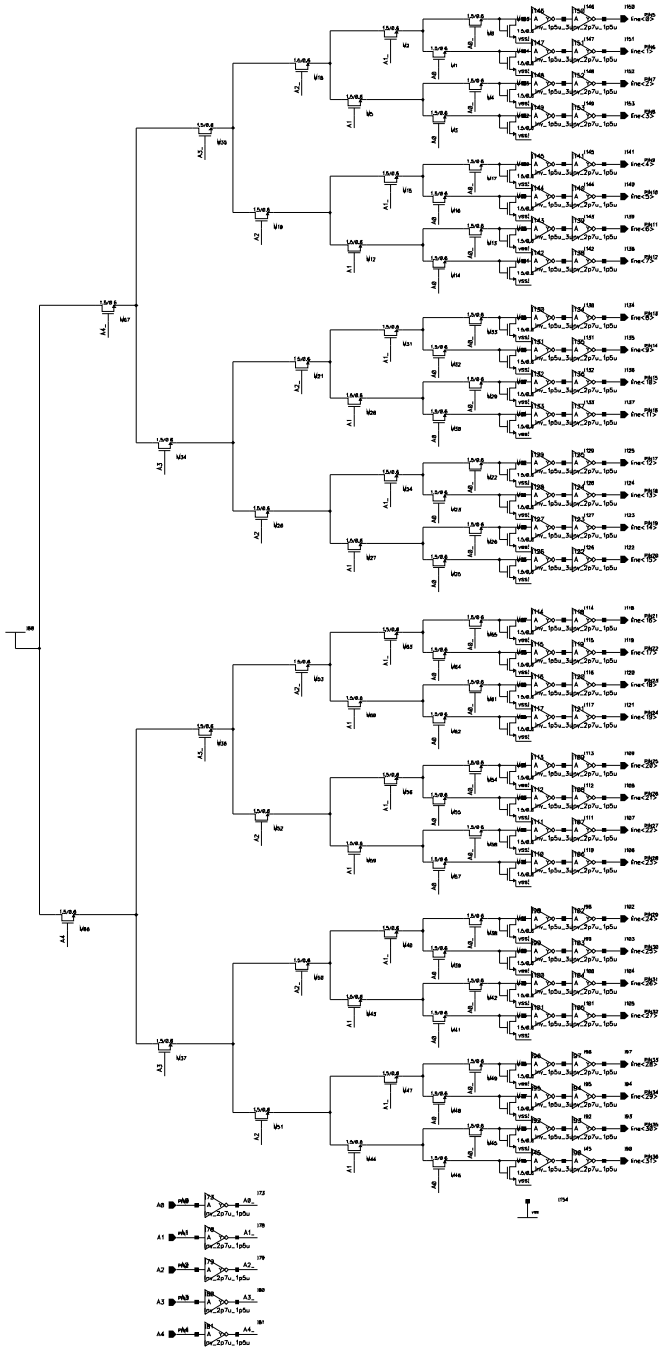

Figure A.7: Line Driver Schematic

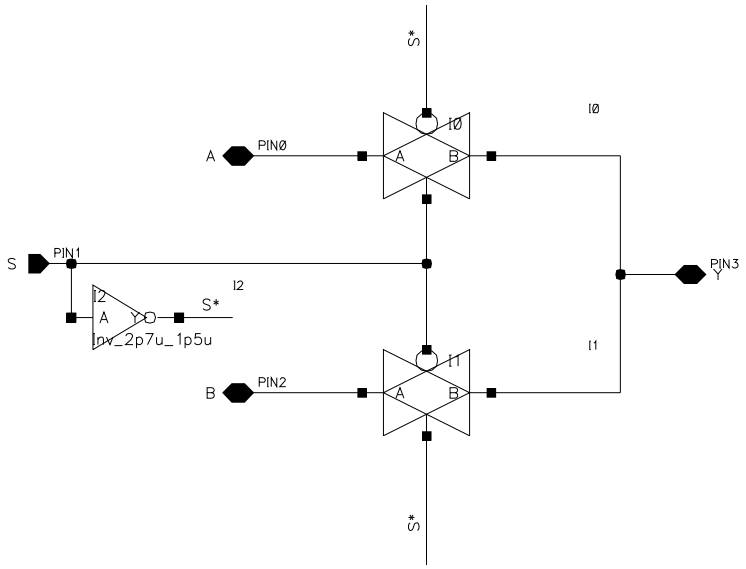

Figure A.8: Alternative 2 to 1 Mux Schematic

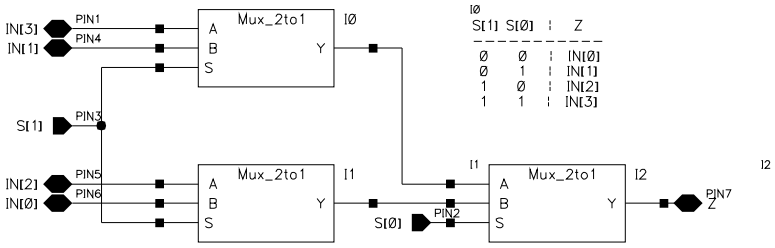

Figure A.9: 4 to 1 Mux Schematic

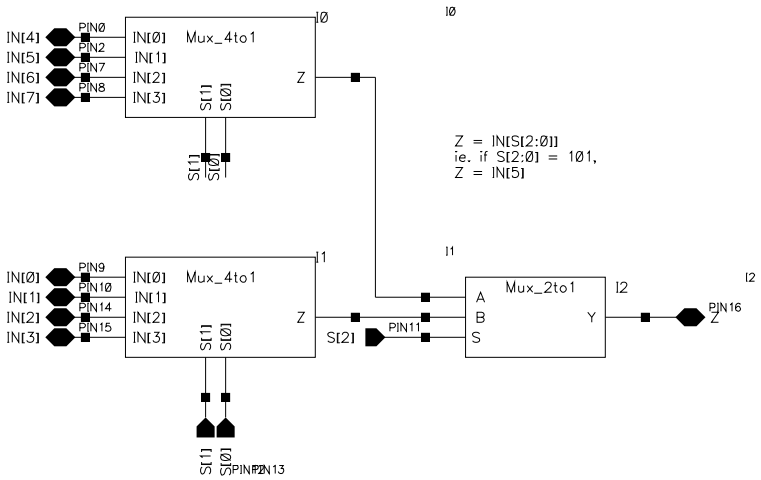

Figure A.10: 8 to 1 Mux Schematic

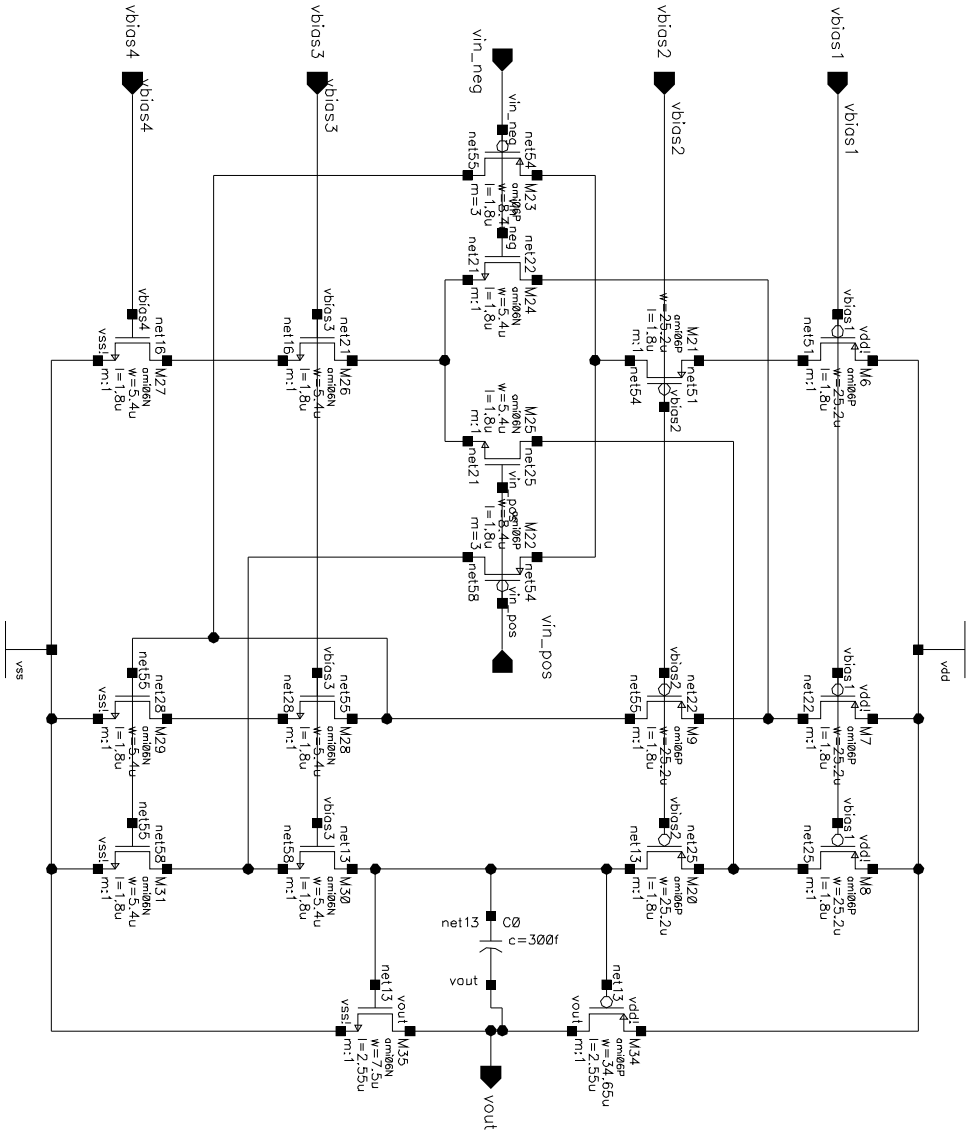

Figure A.11: OpAmp Amp Stages Schematic

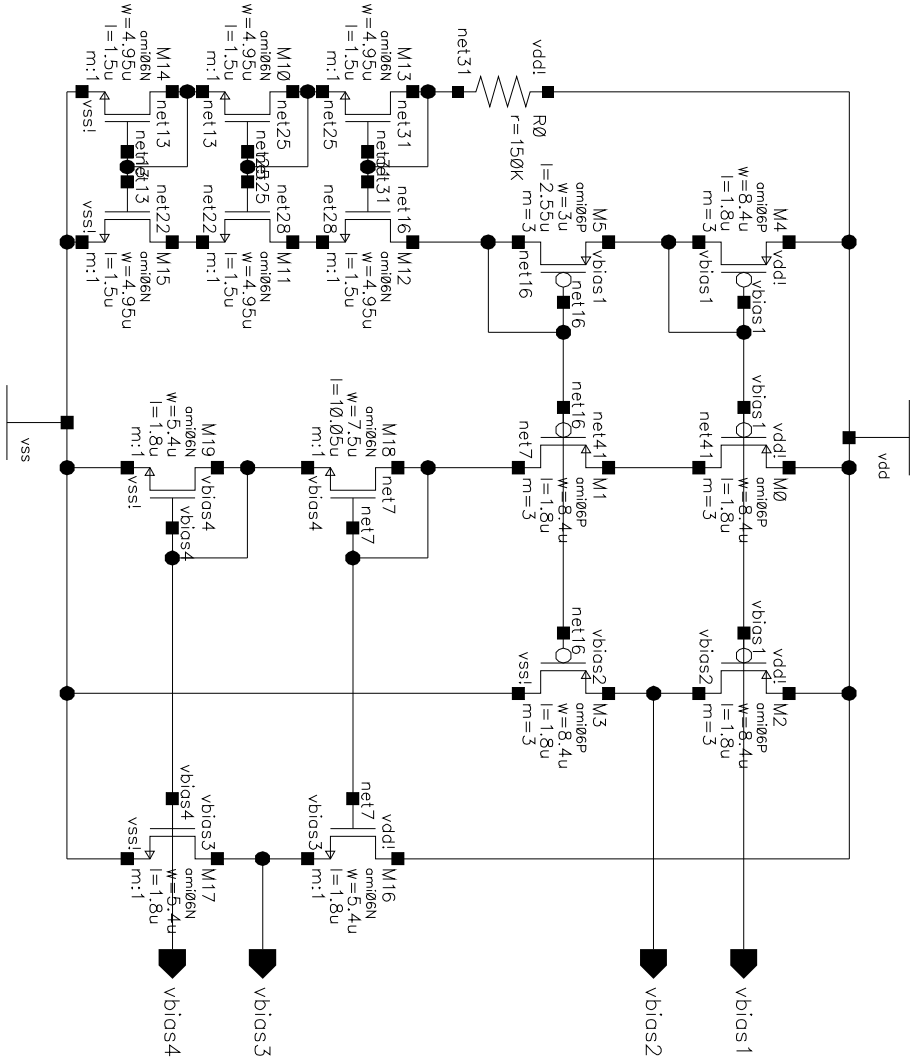

Figure A.12: OpAmp Bias Schematic

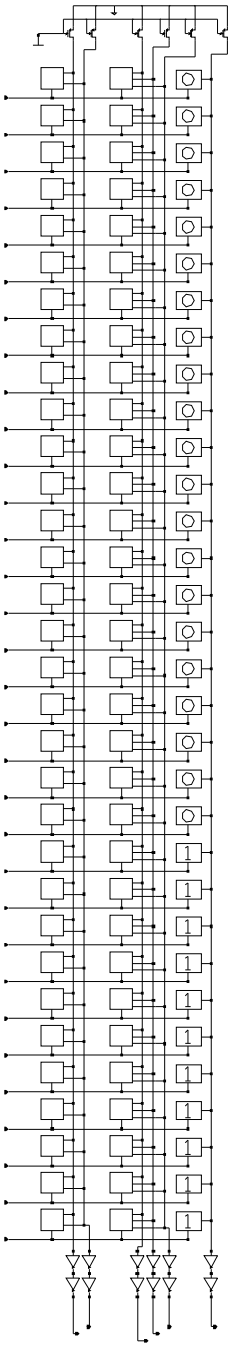

Figure A.13: VC_ROM Schematic

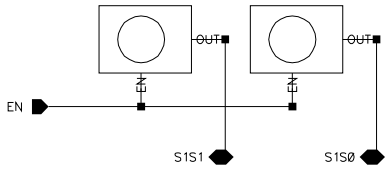

Figure A.14: Stage 1 Gain of 1 ROM Schematic

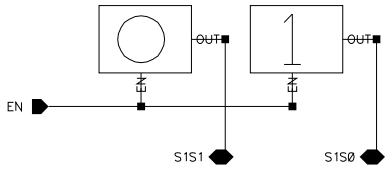

Figure A.15: Stage 1 Gain of 0.1 ROM Schematic

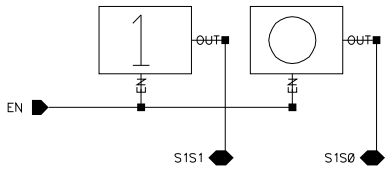

Figure A.16: Stage 1 Gain of 0.2 ROM Schematic

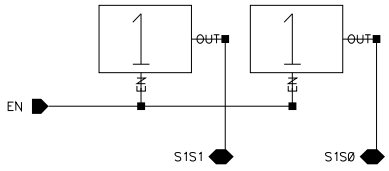

Figure A.17: Stage 1 Gain of 0.4 ROM Schematic

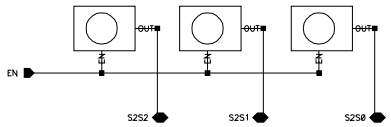

Figure A.18: Stage 2 Gain of 1 ROM Schematic

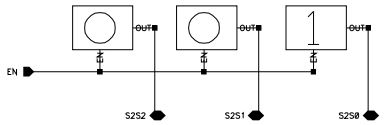

Figure A.19: Stage 2 Gain of 1.12 ROM Schematic

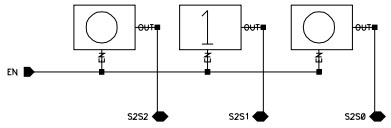

Figure A.20: Stage 2 Gain of 1.25 ROM Schematic

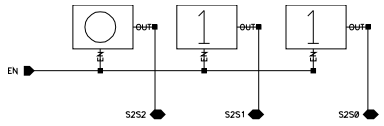

Figure A.21: Stage 2 Gain of 1.4 ROM Schematic

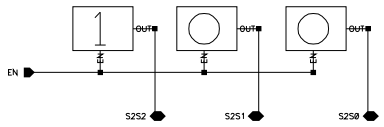

Figure A.22: Stage 2 Gain of 1.58 ROM Schematic

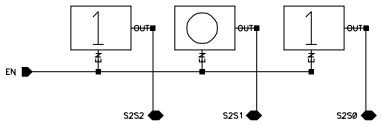

Figure A.23: Stage 2 Gain of 1.77 ROM Schematic

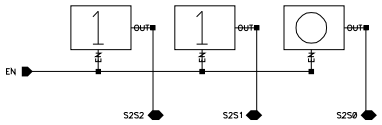

Figure A.24: Stage 2 Gain of 1.99 ROM Schematic

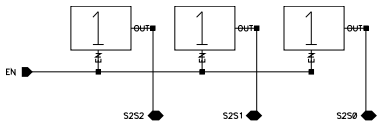

Figure A.25: Stage 2 Gain of 2.23 ROM Schematic

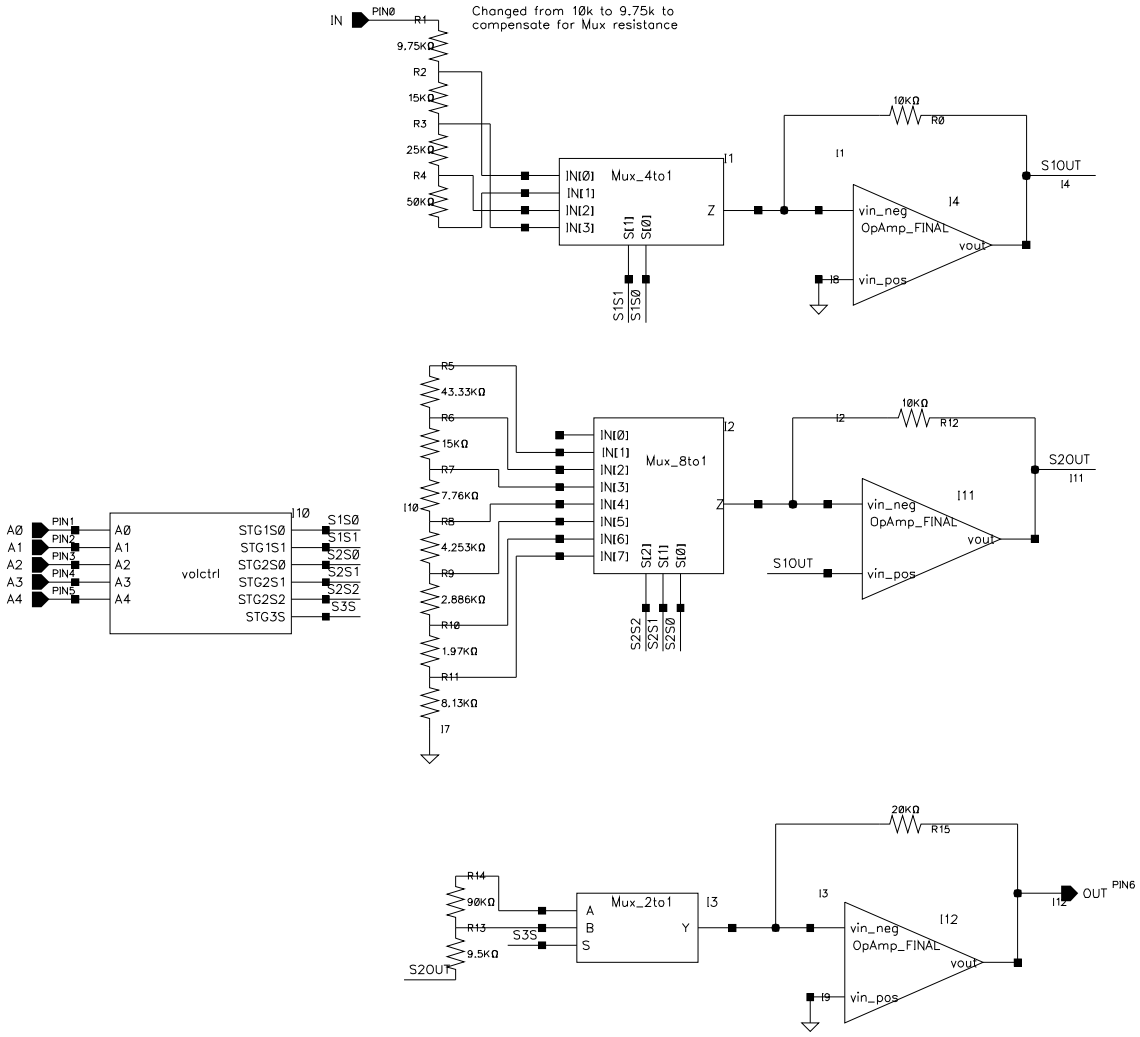

Figure A.26: Volume Control Preamp Schematic

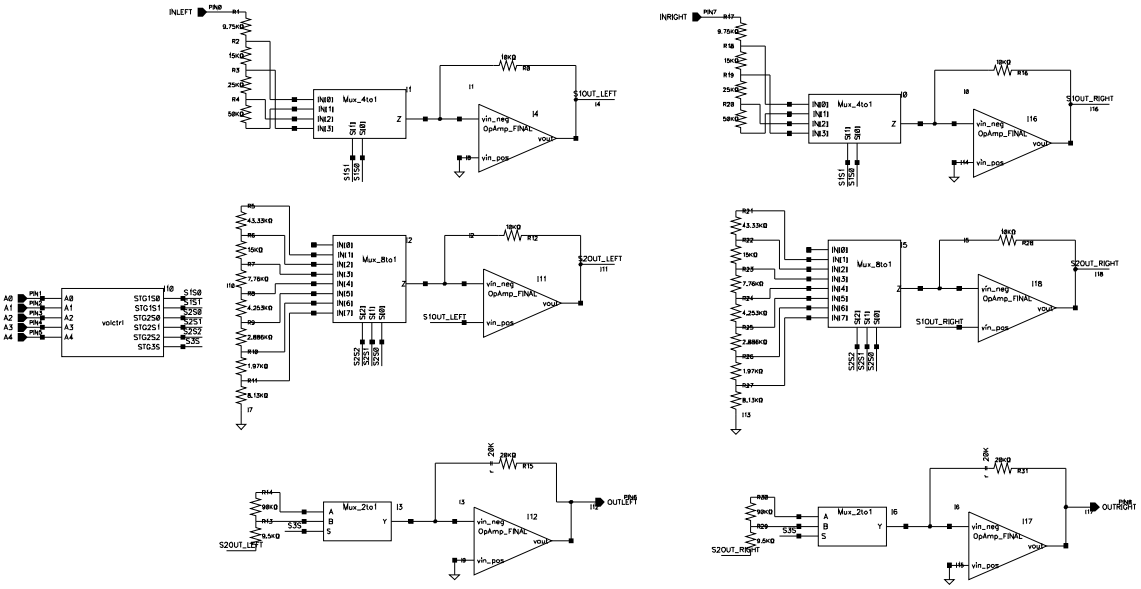

Figure A.27: Stereo Volume Control Preamp Schematic

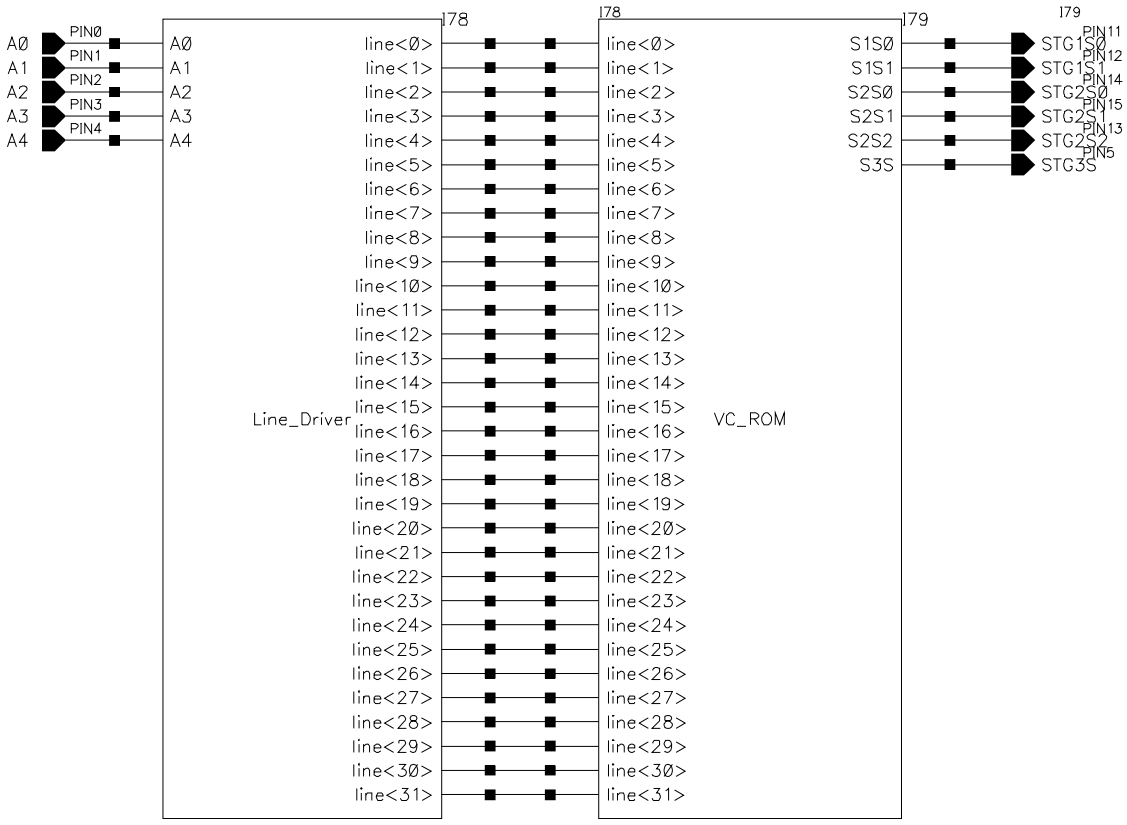

Figure A.28: Volctrl Schematic

Appendix B

Layout

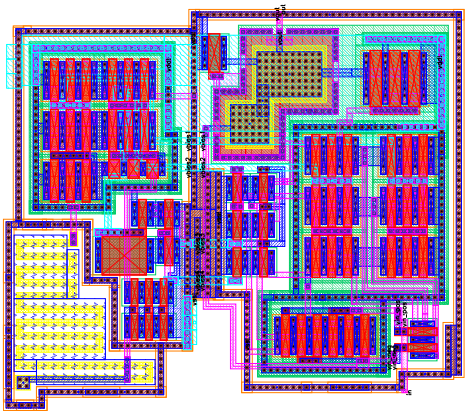

Figure B.1: Analog Input Buffer Layout

Figure B.2: Aquabats Logo Layout

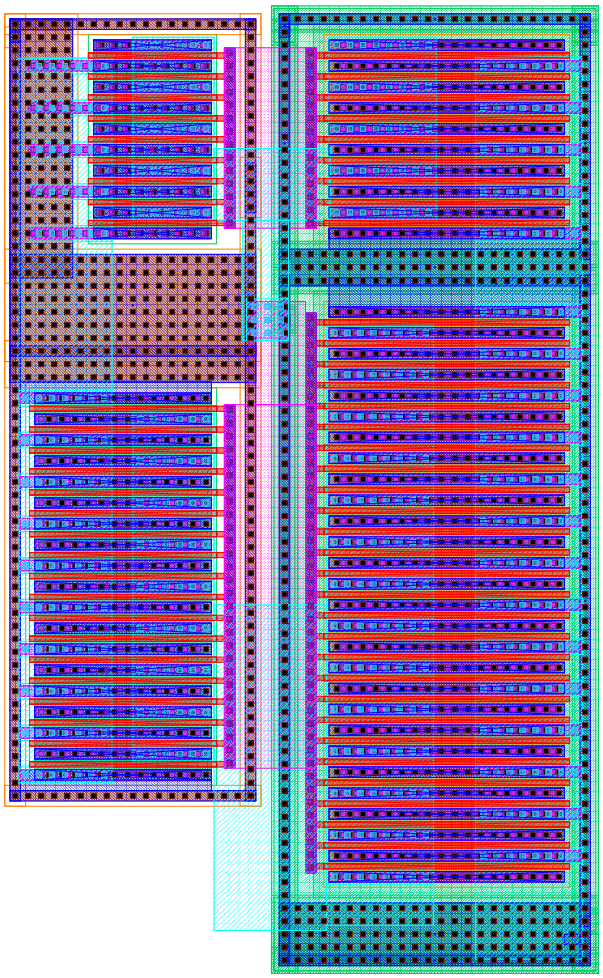

Figure B.3: Large Output Buffer Layout

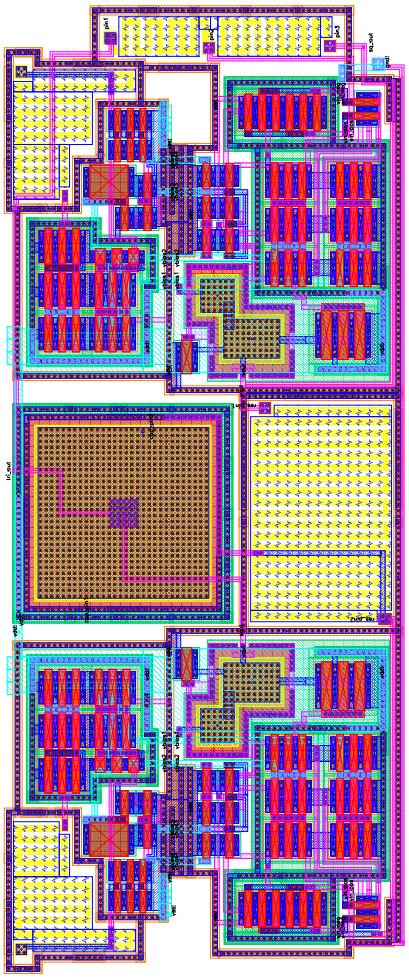

Figure B.4: Bistable Layout

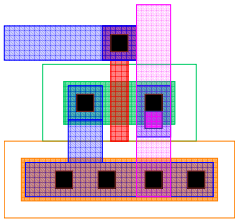

Figure B.5: Bit Zero Layout

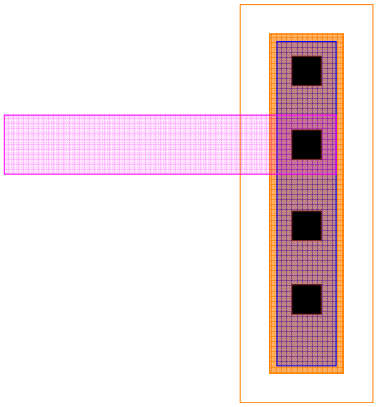

Figure B.6: Bit One Layout

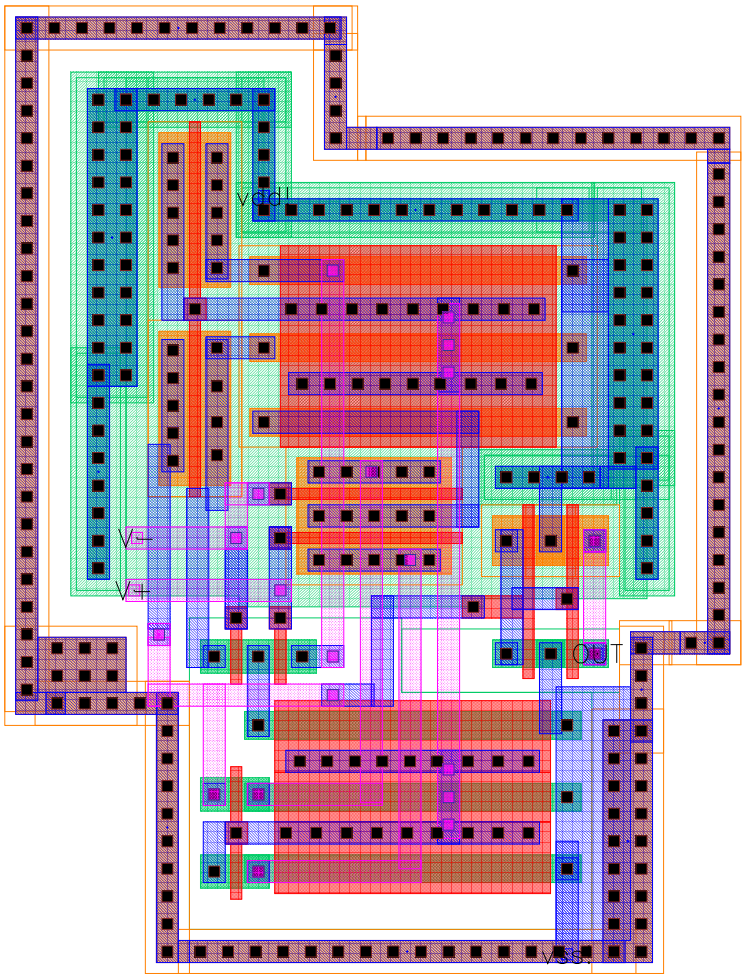

Figure B.7: Comparator Layout

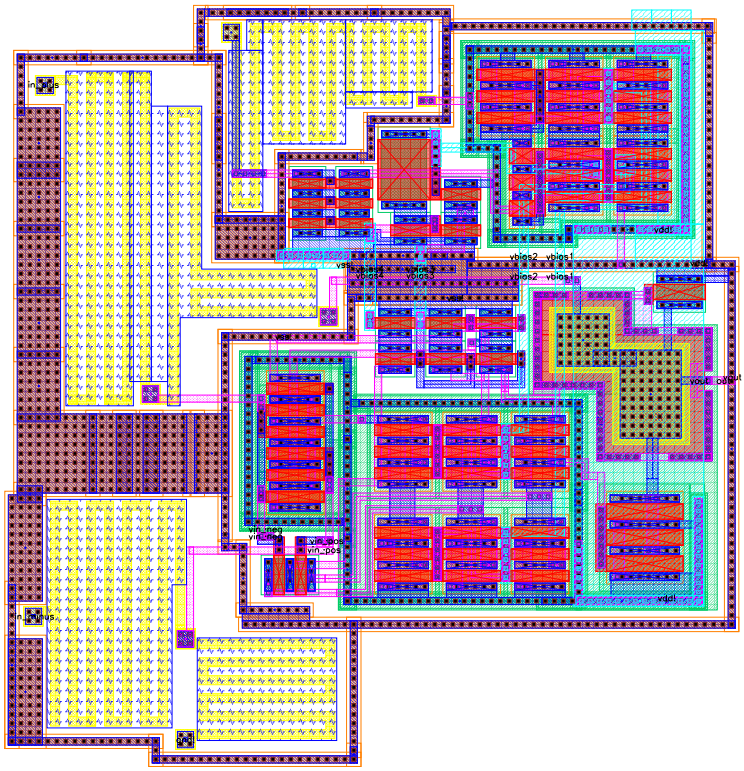

Figure B.8: Differential Input Buffer Layout

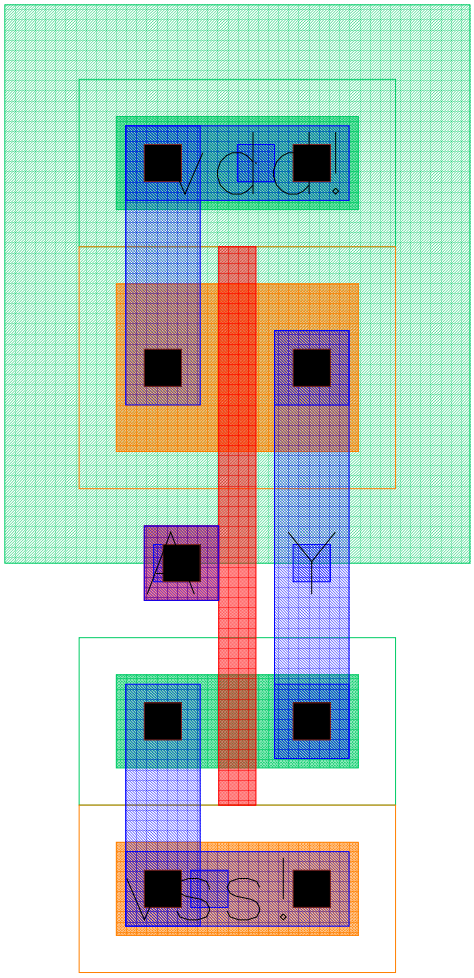

Figure B.9: 18/10 Inverter Layout

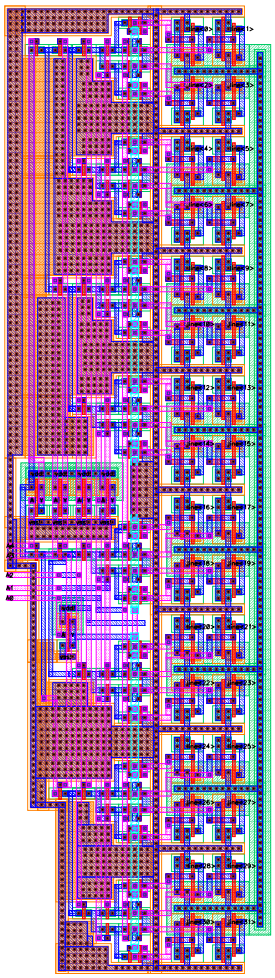

Figure B.10: Line Driver Layout

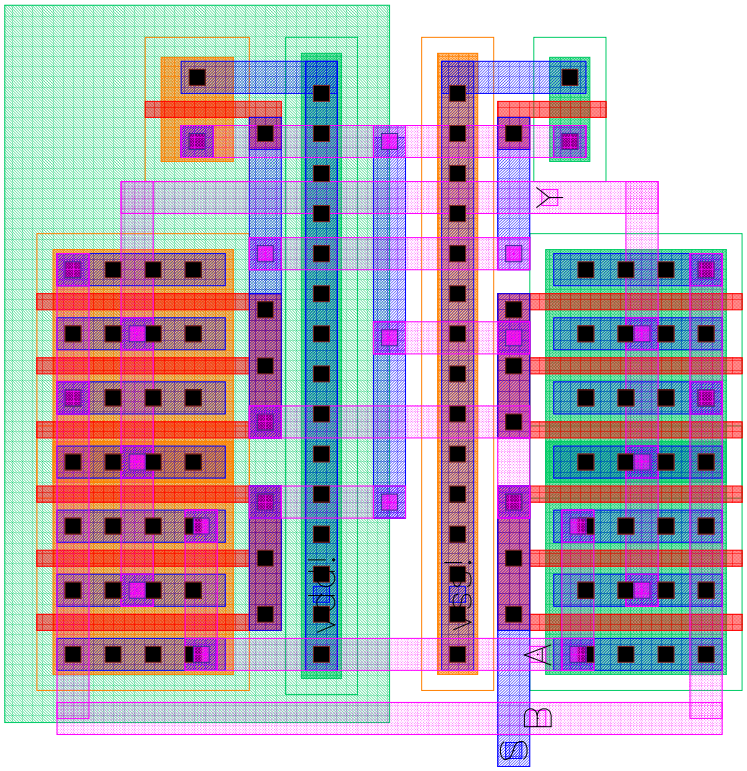

Figure B.11: 2 to 1 Mux Layout

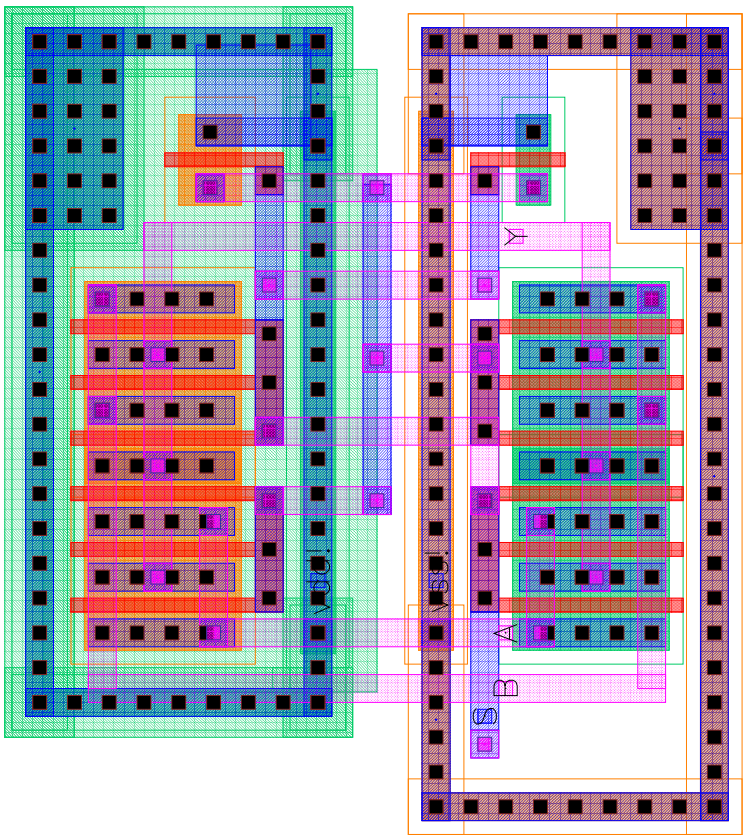

Figure B.12: Alternative 2 to 1 Mux Layout

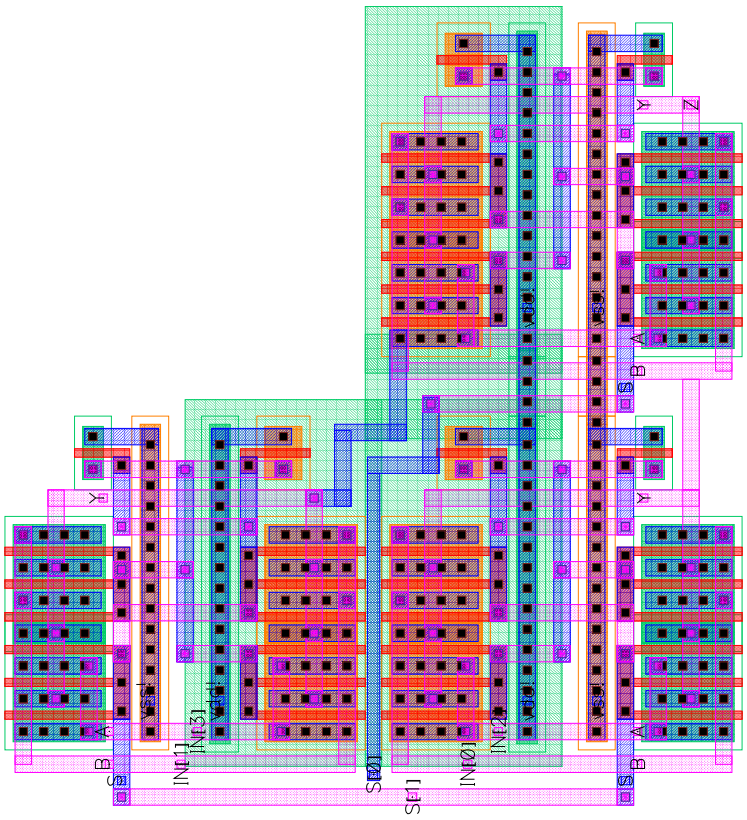

Figure B.13: 4 to 1 Mux Layout

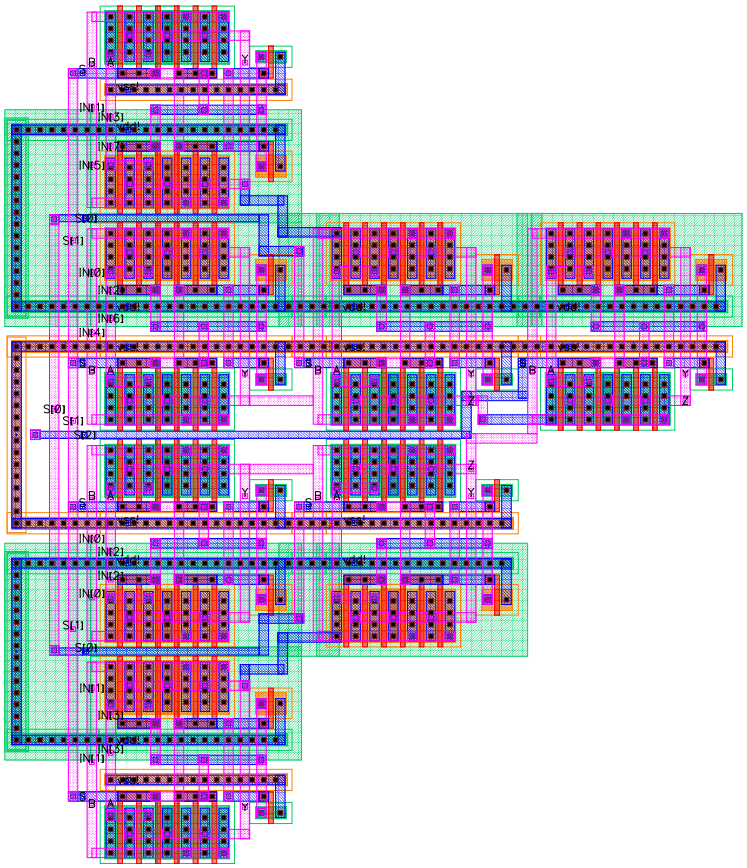

Figure B.14: 8 to 1 Mux Layout

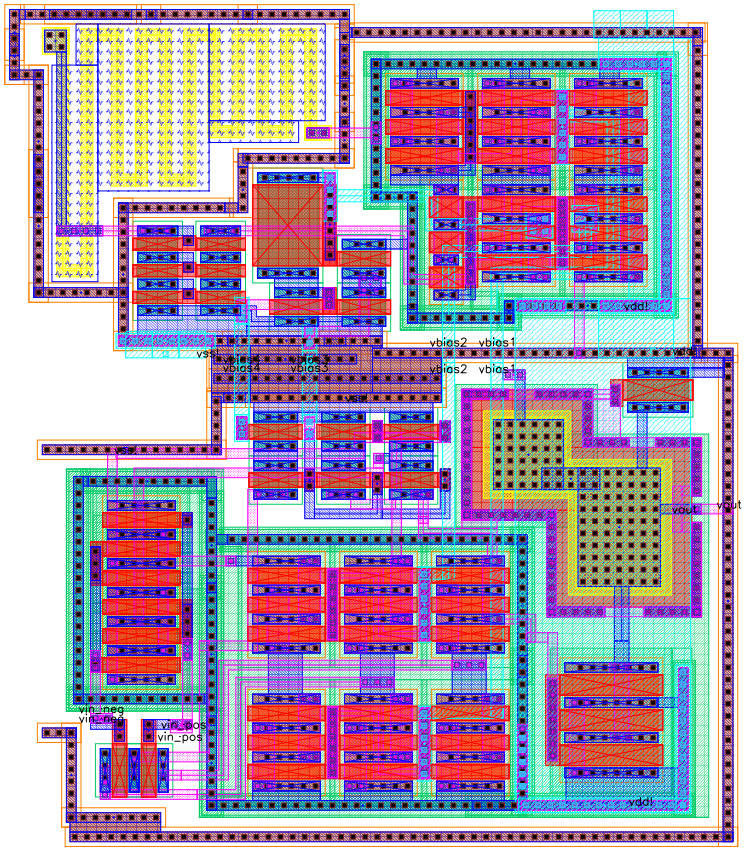

Figure B.15: Op Amp Layout

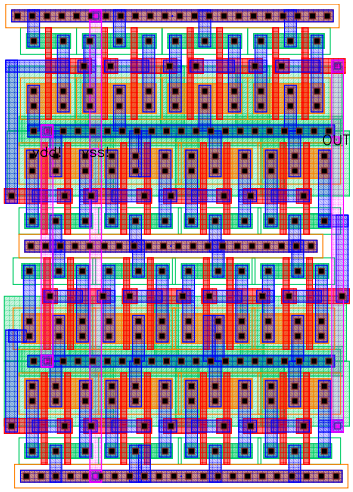

Figure B.16: Ring Oscillator Layout

Figure B.17: ROM Layout

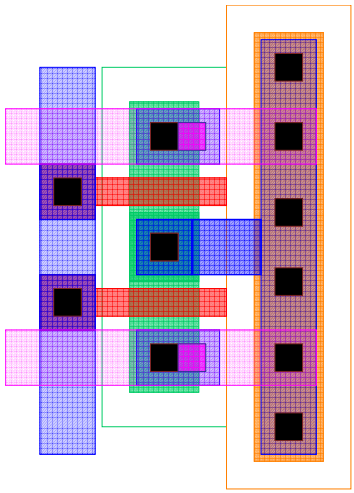

Figure B.18: Stage 1 Gain of 1 ROM Layout

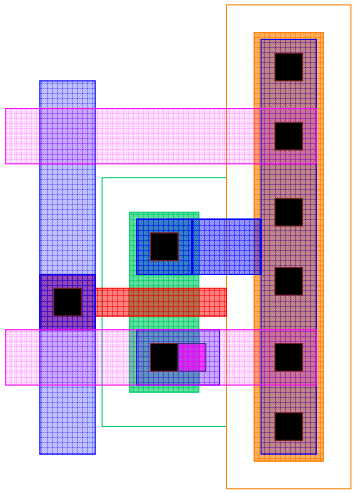

Figure B.19: Stage 1 Gain of 0.1 ROM Layout

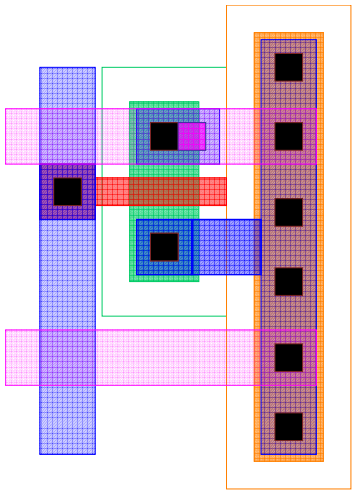

Figure B.20: Stage 1 Gain of 0.2 ROM Layout

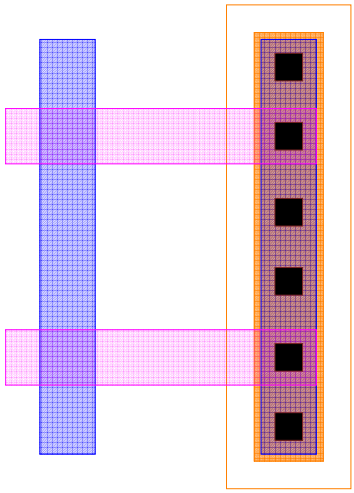

Figure B.21: Stage 1 Gain of 0.4 ROM Layout

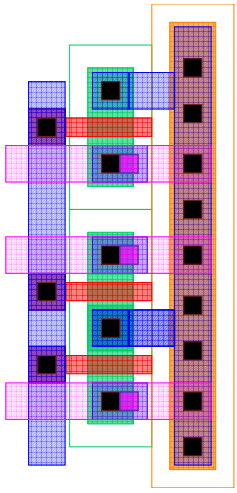

Figure B.22: Stage 2 Gain of 1 ROM Layout

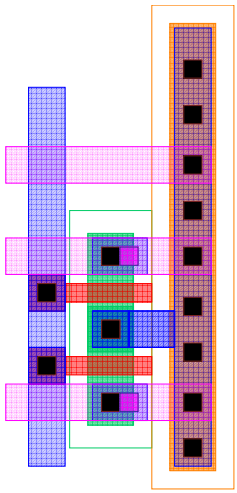

Figure B.23: Stage 2 Gain of 1.12 ROM Layout

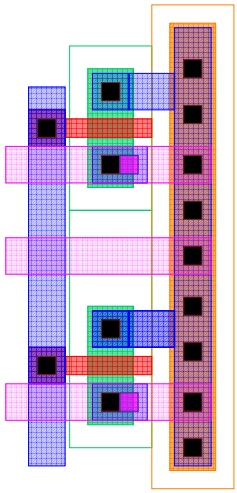

Figure B.24: Stage 2 Gain of 1.25 ROM Layout

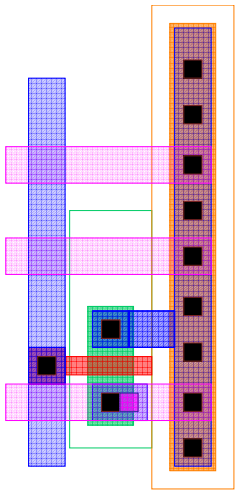

Figure B.25: Stage 2 Gain of 1.4 ROM Layout

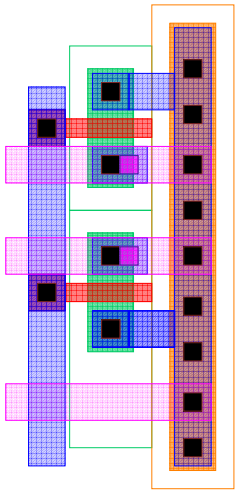

Figure B.26: Stage 2 Gain of 1.58 ROM Layout

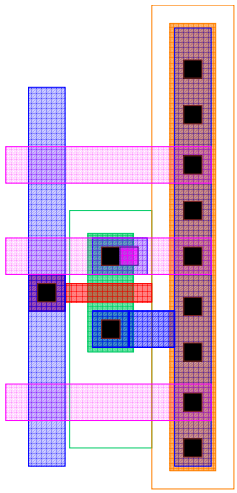

Figure B.27: Stage 2 Gain of 1.77 ROM Layout

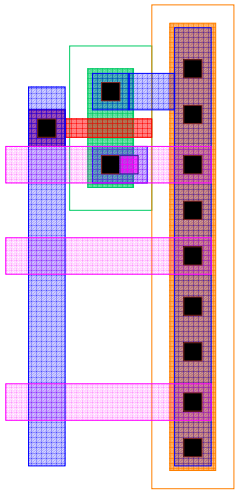

Figure B.28: Stage 2 Gain of 1.99 ROM Layout

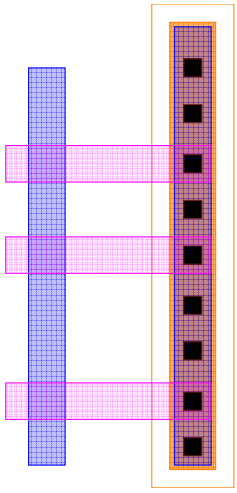

Figure B.29: Stage 2 Gain of 2.23 ROM Layout

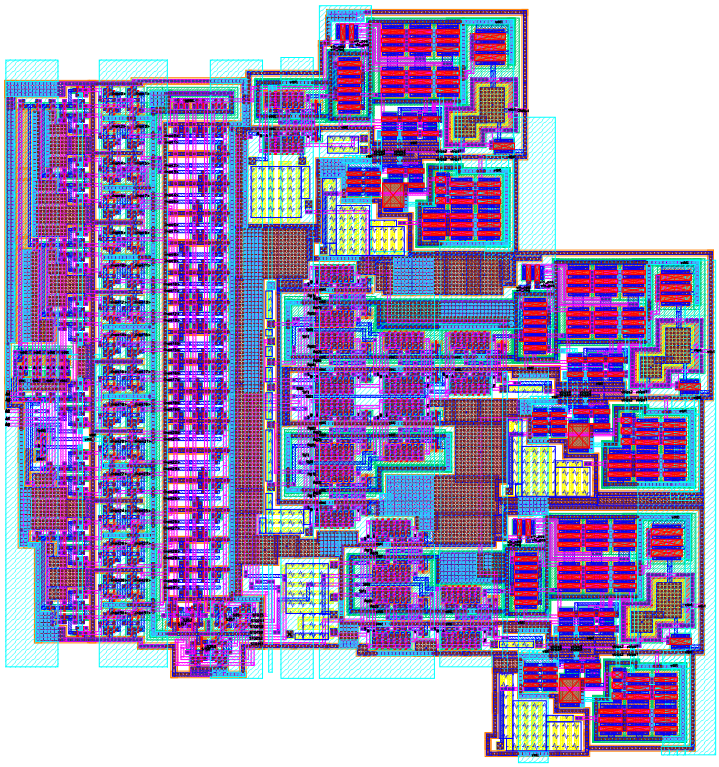

Figure B.30: VC_Preamp Layout

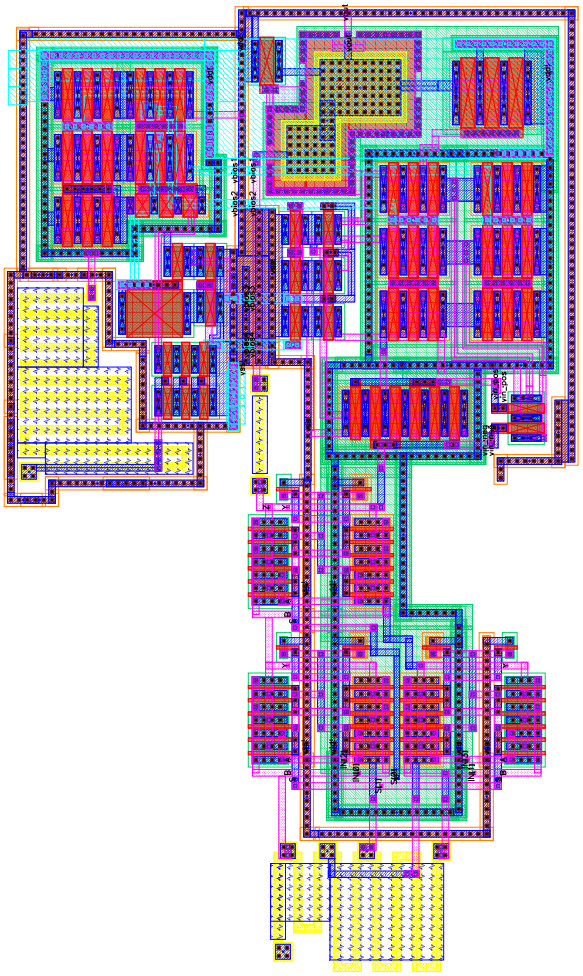

Figure B.31: VC_Preamp Stage 1 Layout

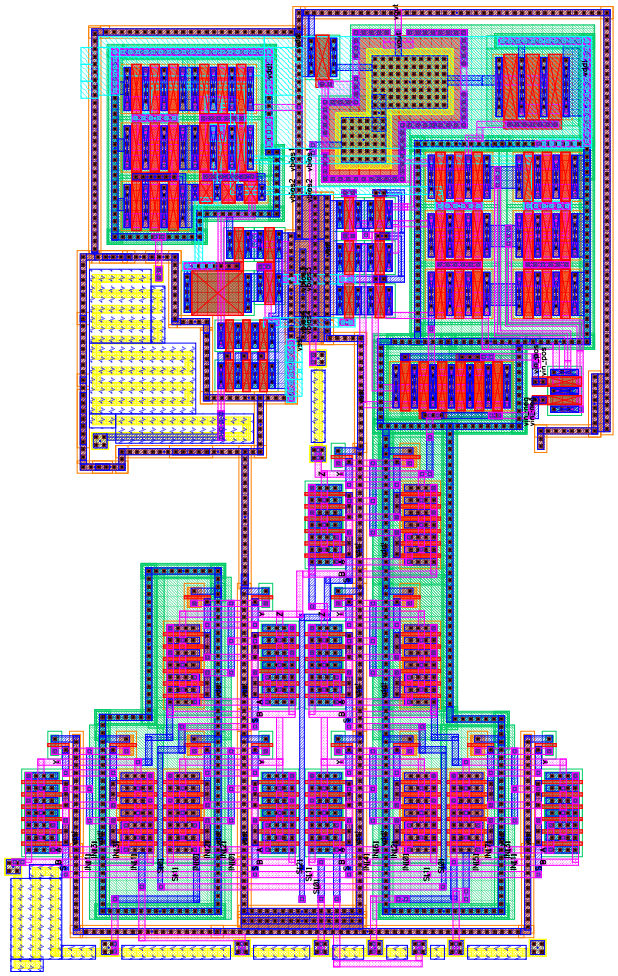

Figure B.32: VC_Preamp Stage 2 Layout

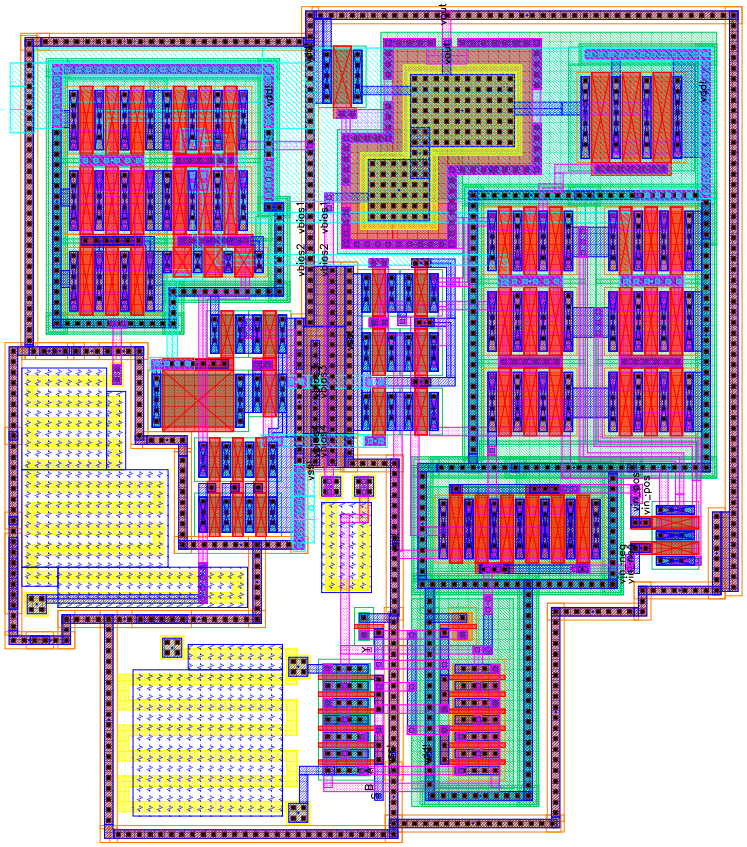

Figure B.33: VC_Preamp Stage 3 Layout

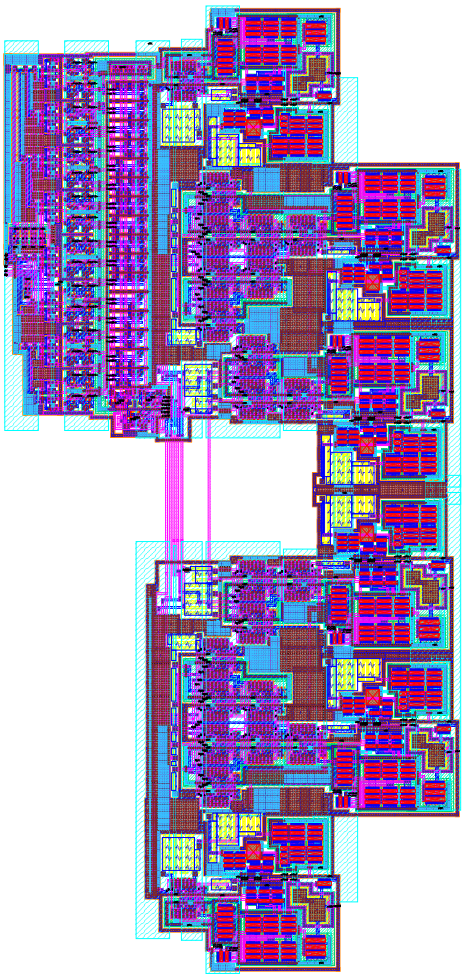

Figure B.34: VC_Preamp Stereo Layout

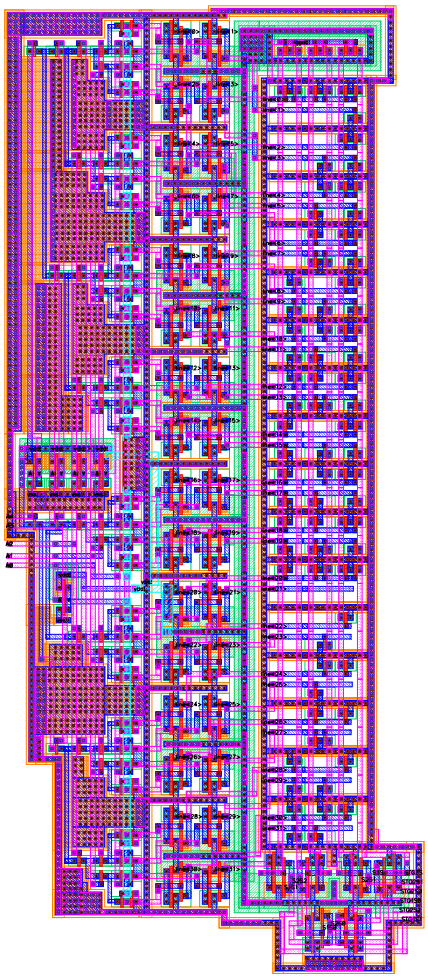

Figure B.35: Volctrl Layout

Appendix C

Chip Pinout

The following table lists the pinout for the *Class-D Front-End* design.

Table C.1: PinOut

Pin	Pad Type	Name	Desc
1	padvdd	vdd	VDD pin
2	padio	sq_wave	Bistable test, square wave output
3	padaref	tri_wave	Bistable test, triangle wave output
4	padaref	20kb	$20k\Omega$ test resistor, terminal B
5	padaref	20ka	$20k\Omega$ test resistor, terminal A
6	padio	test2_out	Comparator test circuit output
7	padaref	test2_in_plus	Comparator test positive differential input
8	padaref	test2_in_minus	Comparator test negative differential input
9	padaref	in_left_plus	Left channel positive input
10	padaref	in_left_minus	Left channel negative input
11	padaref	in_right_plus	Right channel positive input
12	padaref	in_right_minus	Right channel negative input
13	padio	left_pwm	Left channel PWM output
14	padio	left_dir	Left channel DIR output
15	padio	mute	Mute input bit
16	padio	vol_5	Volume control input bit
17	padio	vol_4	Volume control input bit
18	padio	vol_3	Volume control input bit
19	padio	vol_2	Volume control input bit
20	padio	vol_1	Volume control input bit

Continued...

Table C.1: PinOut

Pin	Pad Type	Name	Desc
21	padvss	vss	VSS pin
22	padio	logic_gnd	Logical GND for H-Bridge
23	padio	test_v5	Test circuit volume control input bit
24	padio	test_v4	Test circuit volume control input bit
25	padio	test_v3	Test circuit volume control input bit
26	padio	test_v2	Test circuit volume control input bit
27	padio	test_v1	Test circuit volume control input bit
28	padio	right_dir	Right channel DIR output
29	padio	right_pwm	Right channel PWM output
30	padgnd	gnd	GND pin
31	padaref	opamp_out	Test op-amp output
32	padaref	opamp_minus	Test op-amp minus input
33	padaref	opamp_plus	Test op-amp plus input
34	padio	osc_out	Test ring oscillator output
35	padaref	test_in_plus	Test circuit positive input
36	padaref	test_in_minus	Test circuit negative input
37	padaref	10kb	$10k\Omega$ test resistor, terminal B
38	padaref	10ka	$10k\Omega$ test resistor, terminal A
39	padaref	test_amped	Test circuit preamp output
40	padio	test_pwm	Test circuit PWM output