Sigma−Delta Modulator

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Chapter 1: Project Overview

A sigma−delta modulator is one method for providing the front end to an analog to digital converter. When an analog signal is digitized, quantization error is introduced into the frequency spectrum. The sigma−delta's function is to push the quantization error that is near the signal into a higher frequency band near the sampling frequency. After this is done the signal can be low pass filtered and the original signal can be restored in a digitized form.

This project consists of a sigma−delta modulator with first order noise shaping characteristics. The block diagram of the first order loop is shown in Figure 1, Appendix D.

In the sigma−delta modulator, the difference between the analog input signal and a the output of the digital to analog converter is the input into the integrator. The integrator integrates over each clock period. The clock is at a much higher frequency than the input sinusoid, causing the sine wave to be approximately flat over the clock period. The input to the integrator is the difference between the two pulses. The integration of the pulse difference is linear over one clock period. The output of the integrator represents an accumulation of the error term between the input and the DAC output.

This integral then digitized by a clocked quantizer, and the quantizer output is the output of the sigma−delta modulator. In the feedback path, the DAC shifts the logic level so that the feedback term matches the logic level of the input; making the difference equally weighted.

The transient output of the sigma−delta modulator is a pulse density modulated signal that represents the input sine wave. This waveform is more dense with digital ones when the signal represented is high, and less dense when the waveform is low. A typical transient output is given in Figure 2, Appendix D.

Figure 2 in Appendix D, shows the input in the upper frame, the integrator output in the middle frame, and the transient output in the lower frame. It can be seen that the integrator has varying slopes over short clock sampling times.

The first order sigma−delta described above can be modeled as delays in the Z−domain. The z−domain model is shown in Figure 3, Appendix D. The integrator is simply represented as a clock delay of one with feedback, which functions as an accumulator. The comparator/quantizer is best modeled as an added error term to simplify the complexities of nonlinear math. In this model, the quatization error is idealized to be noncorrelated to the input signal. It can be easily shown that the transfer function of the input to output is simply a clock delay of one, while the error term introduced by the quantization is multiplied by a transfer function of $(1-Z^{-1})$. This is equivalent to a $(1-e^{-jwT})$ term in the frequency domain, which is also the same as 2 sin $(\omega T/2)$. This leads to a dome shaped signal output, centered around $\omega T/2$. First order noise shapingforces the noise into a sine wave shape spread out over the sampling frequency. The desired signal remains in the lower frequency region to be decimated and filtered.

MATLAB and the Simulink tool were used to analyze the first order linear model. The first order results are shown in Figure 4, Appendix D. Ideally, a first order loop will provide 60 dB of resolution.

The specifications for this project were to design a first order sigma−delta modulator achieving a noise resolution of 24 dB or 6 bits of digital resolution up to 10 kHz, with a clock frequency of at least 1 MHz. This prior specification means that the difference between the signal peak and the noise floor must have a difference of 24 dB in all frequency bins up to 10 kHz.

Chapter 2 : Circuit Description

2.1 Top Level Design

The top level design used is shown in Appendix A, Figure 9. The integrator is a simple Miller integrator, using a large resistor and small capacitor to minimize layout space. The output feeds the input of a comparator referenced to ground to quantize this signal to VDD or VSS. This output is then fed to a D flip−flop, which inserts the delay necessary to clock the circuit. The output of this is fed into a DAC reference level adjustment, which converts this back to the dynamic range of the input signal. The DAC operates from the Q and Qbar outputs of the flip−flop. The sum at the input to the Miller integrator is a negative sum because the DAC output is negatively referenced. The summing resistance values are equal to assign an equal weight to both parts in the integration. The following sections detail the design aspects of each circuit component.

2.2 The Integrator

2.2.1 Setting the Integrator Gain

The loop gain for this circuit is not crucial, but it is necessary that the gain of the integrator is small enough so that the device does not saturate or run into the positive or negative rails. Ideally, the gain of the loop should be one, so this circuit can be implemented in other architectures such as the MASH structure. This architecture contains combined first order loops so the noise of the first stage cancels out, and the loop has second order noise shaped error. This circuit is highly sensitive to loop gain for complete cancellation, so the gain needs to be approximately unity.

To achieve a gain of one, the integrator gain factor T/RC is formed from time domain analysis, and set to one. For a given clock period, R and C values can be calculated.

2.2.2 Op Amp Design Issues

The operational amplifier that the integrator uses must have high gain to effectively carry out a smooth integration, as well as a large enough bandwidth to support the high frequency square waves it will be integrating. The op amp operates at the clock frequency, since the differences are being integrated over that region of time. Therefore, the gain bandwidth product of the op amp must be greater than one at the clock frequency to effectively pass the signal. Several times this bandwidth is needed so several odd harmonics of the square wave are integrated. This requires the amplifier to have both a large gain and high bandwidth. The amplifier used is shown in Figure 5 of Appendix A.

The key thing to note about the amplifier is the frequency compensation network. The capacitor and resistor are used to push the high frequency zero out of the passband of the op amp, and into the attenuated region of operation. Both components are across the high gain block of the op amp, and in turn are being acted upon by the Miller effect. This helps reduce the size of the capacitor needed.

The multipliers used on the biasing transistors on the output are used so the output bias can still be sufficiently high, while reducing the output capacitance significantly. This also helps keep the needed capacitor in the compensation network small, and increase the slew rate of the amplifier. The slew rate comes into play here during the integration but is not a problem since the clock period is so small that the voltage range does not change much during this range.

An output stage to this amplifier is not needed since the only current needed is to drive the feedback capacitance and the input capacitance of the comparator.

2.3 Comparator Design

The only key design issue that arose with the comparator design is propagation delay. If the delay of the comparator became a problem, it would limit the highest clock rate and thus highest oversampling ratio of the modulator.

The comparator design used is shown in Appendix A, Figure 6. Notice that this design bears a strong resemblance to the op amp as described in the previous section. The similarity between the two designs helped during the layout stage of the project, where the only difference is the resistor and capacitor compensation network. The only reason this design is possible is because of the relatively large amount of space available for this design.

The comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed, as it will only slow down the switching speed. Notice that the lower left biasing transistor has a multiplier of 2 as opposed to the op amp design that does not have this multiplier. This is to increase the gain of the transistors, and help them switch faster without significantly increasing the output capacitance.

2.4 Flip Flop Design

The D flip−flop is composed of two D latches arranged in a master−slave configuration. Each D latch consists of two transmission gates and two inverters. The transmission gates are oppositely clocked. The input passes through transmission gate 1 when the gate is turned 'on'. The signal passes through two inverters and is held by transmission gate 2, which is turned 'off'. The output Bbar is taken at the output of the first inverter between the two transmission gates. The output B of the D Latch is taken at the output of the second inverter between the two transmission gates. In the flip−flop, the input comes into input D of the first D latch. The output B of the first D latch drives input D of the second D Latch. The outputs Q and Qbar are taken off the outputs of the second D latch B and Bbar respectively.

2.5 Digital to Analog Converter

The digital to analog converter is necessary to convert the −2.5 to 2.5 volt signal at the output to a −0.7 to 0.7 volt signal to be subtracted from the input. The DAC must reference the feedback signal in the modulator so that the difference at the integrating amplifier does not saturate the amplifier. The DAC consists of two transmission gates and two pairs of resistors. The gate of the NMOS on transmission gate 1 is tied to the gate of the PMOS on transmission gate 2. Likewise, the gate of the PMOS on transmission gate 1 is tied to the gate of the NMOS on transmission gate 2. The first pair of gates is driven by Q from the output of the D flip−flop. The second pair of gates is driven by Qbar from the output of the D flip−flop. Qbar is the inverse of Q, so this design turns only one transmission gate on at a time. The input to each transmission gate is a voltage divided down from the positive and negative 2.5 volt rails. This voltage division is accomplished using a 2.5 kΩ resistor tied to ground and a 1 kΩ resistor connected to the respective rail.

Chapter 3: Simulation

3.1 Integrator Simulation Results

When simulating the integrator to see how well it would work, a step function was input to the circuit at the clock frequency. The reason for this method of testing is because this is essentially what the integrator will have as an input at normal operating conditions. During a clock period, the change of the sine wave is small, and very close to a flat pulse. The integrator will have to be able to integrate the difference between the input step and the output step. The integrator is able to handle the input pulse and integrates it to a fairly clean triangular wave.

3.2 Op Amp Simulations

The op amp had special design considerations that had to be taken into account, which are discussed in the design section in more detail. It is necessary to have a high op amp gain at the signal frequency and a very high gain bandwidth product to allow for several harmonics of the square wave to pass. The simulation results are shown in Figure 3 in Appendix D.

From the simulation it can be shown that the op amp has 80 dB of gain at 10 kHz and a gain bandwidth of 45 MHz. This should be plenty of space for the square wave harmonics to pass through. The op amp also has a phase margin of 50 degrees.

3.3 Comparator Simulations

The comparator simulations are relatively simple to perform. The comparator is set up so the threshold is zero volts. This was done by grounding the inverting input. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail. The propagation delay of the comparator is 5ns.

3.4 D Flip−Flop Simulations

To test the flip−flop, the input signal used was a square wave with a frequency less than that of the clock. To verify the correct operation of the flip−flop the input, output and clock signal were analyzed. The flip−flop was determined to work because the input was passed on the rising edge of the clock and held while the clock was high, and did not pass on any other clock transistions.

3.5 DAC Simulations

In the operation of the sigma−delta modulator, the DAC receives a square wave signal from the flip−flop. To test the operation of the DAC, a −2.5 to 2.5 volt square wave was applied to the input of the DAC. The DAC shifts the voltage levels to ± 0.7 volts to eliminate offset problems in the differencing stage.

3.6 Top Level Simulation

The ultimate goal of the top level simulation is to obtain a fast fourier transform of the pulse density modulated output and analyze the difference between the signal and the noise floor. Since the input is a sine wave, the recovered frequency domain signal should be a single spike at the frequency of the original signal.

The Cadence DFT function on the output signal was used to do this. The DFT requires evenly spaced samples, but the spectre SPICE simulator does not use this type of format.

The simulator takes fewer points when the signal has a gradual change and more points when the signal is quickly changing. A function in the analog environment window called strobing was used to gather the correct number of evenly spaced samples. The DFT requires a given number of samples, so it is necessary to set the strobe period so the number of points taken will be the same as the number of points strobed.

When taking the DFT of the output, the first period of the output was skipped to ignore startup transients. The DFT was taken from the second period to the end of the recorded time. For final simulations a 4096 point DFT was used, which allowed enough room for many samples while not taking a long time to simulate.

To simulate the performance, a test signal is applied to the circuit that is smaller than the cutoff of 10 kHz that was specified earlier. This is due to the noise shaping characteristics of the sigma−delta modulator. If a small input frequency is used, then the modulator will be modulating the harmonics that occur after the signal. If a 10 kHz input frequency is applied, then it is not possible to see the noise shaping characteristics of the modulator in the frequency band of interest. As a result, for the final simulations a 1 kHz test signal was used which minimized simulation time as well as gave full insight into how the circuit performed. The display output in Figure 6, Appendix D shows how the modulator performed with an input signal of 1 kHz, 0.5 volt amplitude, and a sampling frequency of 5 MHz.
From this plot it can be shown that the modulator outputs about 35 dB up to 10 kHz, and well up to 100 kHz. This results in 5 bits of resolution for an A/D converter that uses this sigma−delta modulator.

Chapter 4: Layout

4.1 Operational Amplifier Layout

The sigma−delta modulator layout is shown in Figure 4, Appendix B. The design of the op amp makes use of multipliers, which can make difficult to identify individual transistors at first. The differential pair transistors, along with the bottom biasing transistors, are grouped together in the bottom left hand side. These are being fed by the top PMOS devices that have been overlapped to save space. Since the use of a multiplier forces the PMOS devices to use mutual drains or mutual sources, these are connected together. The gates to all three PMOS devices are common, so they are connected together as well. The 380 kΩ resistor is snaked on the top of the design to help make the design more square, as well as save space. The 15 kΩ resistor is small enough so that it can be placed between the differential pair and the output. The capacitor is added to complete the rectangle, and a guard ring is added to help protect against substrate noise. The integrator will be sensitive to any digital noise injected into the substrate by other digital devices on the circuit. The total size of the op amp is 86 microns x 45 microns.

4.2 Comparator Layout

The design of the comparator was such that it would be similar enough to the op amp design so the layout could be copied and easily verified. The only differences between the comparator design and the op amp design is the use of the compensation resistor and capacitor, and the extra multipliers on a biasing NMOS device. The addition of the multiplier was fairly easy, since there was plenty of space available. The layout is shown in Figure 3, Appendix B. The total size of the comparator is 86 microns x 45 microns.

4.3 D Flip−Flop Layout

The flip−flop layout consists of 4 instances of the transistor layout and 5 instances of the inverter layout. The layout of the flip−flop is in such a way that the two D Latches and the inverter on the clock line are easily distinguishable. The flip−flop also features a guard ring connected to VSS to protect other sensitive portions of the circuit from the high frequency noise associated with the fast switching of this device. The flip−flop measures 36 microns x 60 microns. The flip−flop layout is shown in Figure 2, Appendix B.

4.4 D/A Layout

The layout of the DAC consists of two instances of the transistor and two 1 kΩ and two 2.5 kΩ resistors made of high resistive doped poly2. The DAC has both an input and a complementary input, so both of these are run to the center of the design. The transmission gates are minimum size. The total size is 35 microns x 45 microns. The D/A layout is shown in Figure 1, Appendix B.

4.5 Top Level Layout

The top level design was laid out in attempt to make the modulator as rectangular as possible. The 1 MΩ resistors are run on the bottom of the layout, making the design fairly rectangular. The small 100 fF capacitor is near the op amp layout, since it is connected directly as a feedback path. The layout order is very similar to that of the schematic, which made it easier for wiring purposes. The VDD line is run on top of the devices, while the VSS and ground lines run between the resistors and the other devices. The entire design took up only 250 microns x 130 microns, so there was plenty of space left over on the chip. The layout can be seen in Figure 5, Appendix B.

4.6 Chip Level Layout

This layout can be seen in Figure 6 of Appendix B. Since the top level designs were so small, as many instances of the top level layout were inserted as possible. There are two top level models on the chip that are completely bonded out, including all intermediate

nodes. These intermediate nodes contain transmission gates. An extra pin is used to externally enable and disable the transmission gates. These were included to prevent the internal loading of the devices by the relatively large wire bond capacitances.

There were also two top level designs that only have input, clock, and output nodes bonded out. This was done for simplicity, for comparasion between these top level designs and the designs that contain intermediate nodes. Each individual device on the chip was bonded out, so these can be tested if anything goes wrong with the chip. Also it will allow testing of any device that may have caused the failure.

Included on the chip were eight "dummy" top level models that are simply in the chip to take up space. These dummy blocks are connected to VDD and VSS for LVS purposes, since these are global variables included in the schematic. In addition to these top level "dummy" blocks are eight "dummy" comparators. These are also wired up to VDD and VSS, and are used to take up space on the chip. These are inserted into the chip so MOSIS will not quietly fill empty chip space.

On the output nodes of the chip are buffers, which are to buffer the output of the circuit from the large wire bonding capacitance that is produced. The buffer is simply two inverters, one 5 x minimum size and the other 20 x minimum size.

Chapter 5: Verification

See Appendix C for LVS output of notes. The entire chip level design passes LVS, so the layout is wired the same as the schematic. Care was taken to make sure that every level passed LVS and DRC before proceeding to the next device.

Chapter 6: Experimental Results

To be done on the return of the fabricated chip.

Chapter 7: Conclusion

The sigma−delta modulator was designed, simulated, and laid out has been submitted to MOSIS and is currently waiting for fabication. We have learned many different things during this project, since this is the first layout that either of us has ever worked on. We hope that this class continues to be offered, as there are many benefits to such an experience. This project introduced us to design, simulation and layout as well as allowed us to gain familiarity with tools used in industry.

Appendix A:

Figure 1: Operational Amplifier Schematic

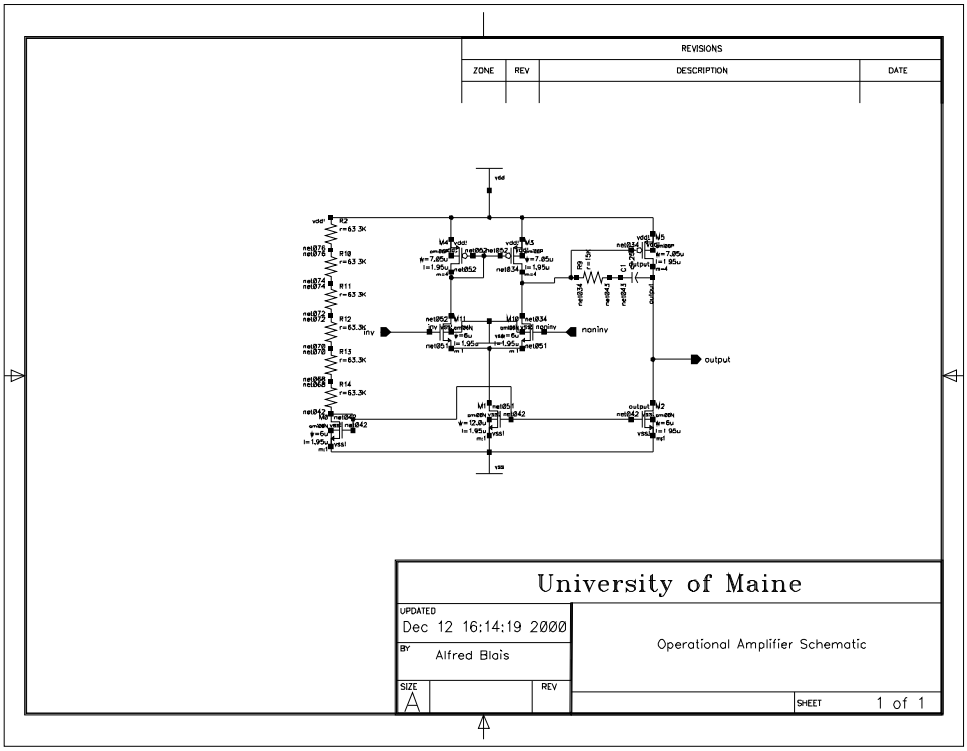


Figure 2: Comparator Schematic

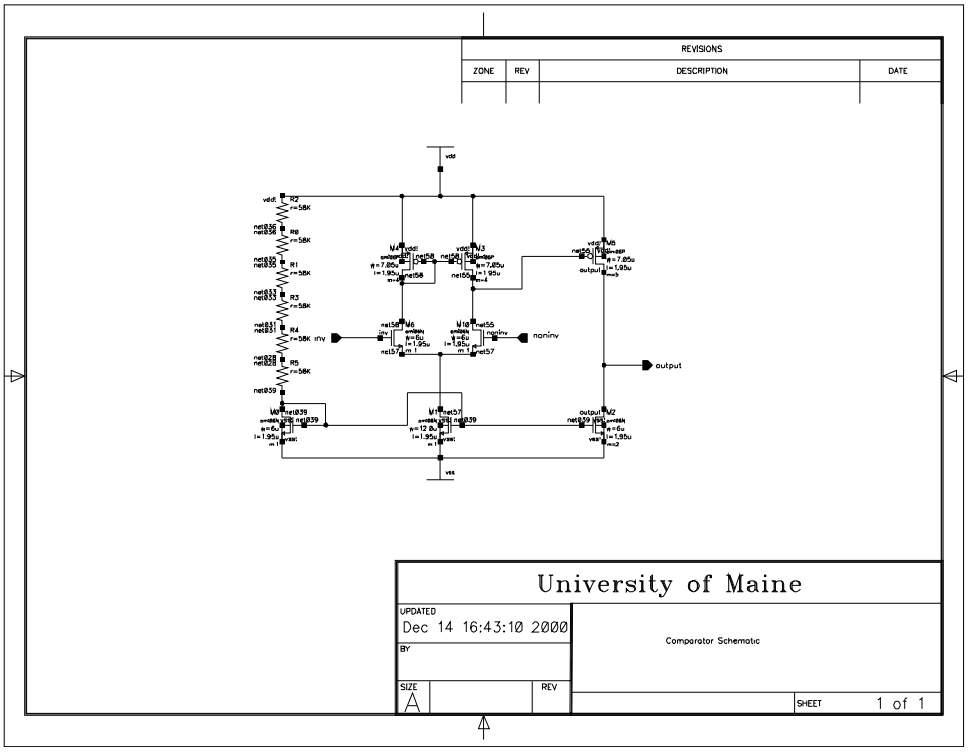


Figure 3: D Flip−Flop Schematic

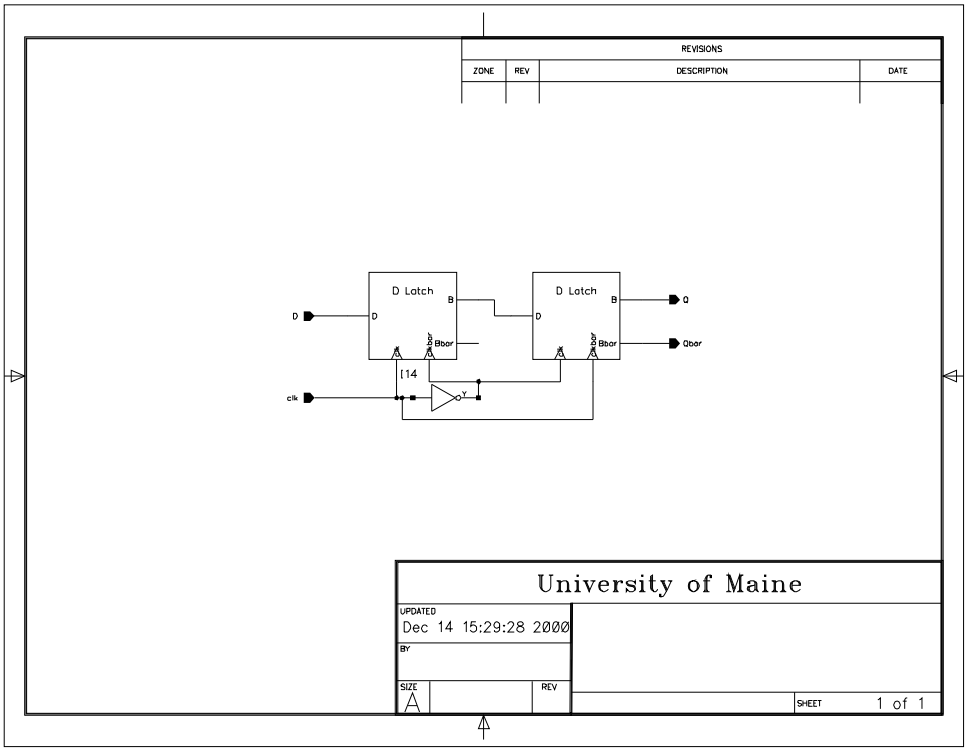


Figure 4: D/A Schematic

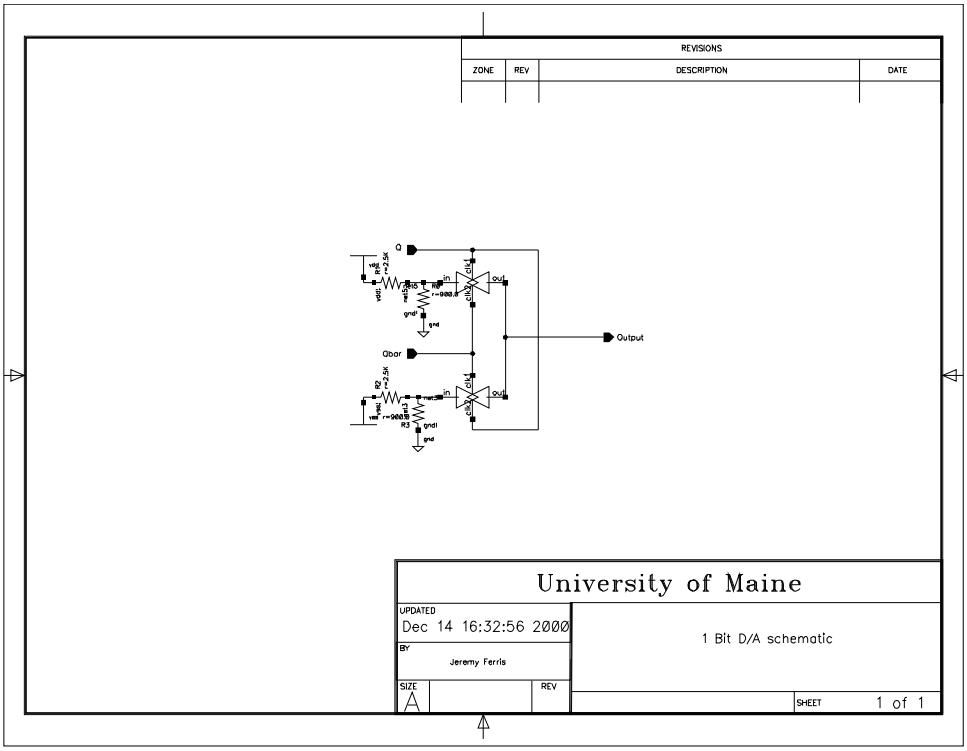


Figure 5: D Latch Schematic

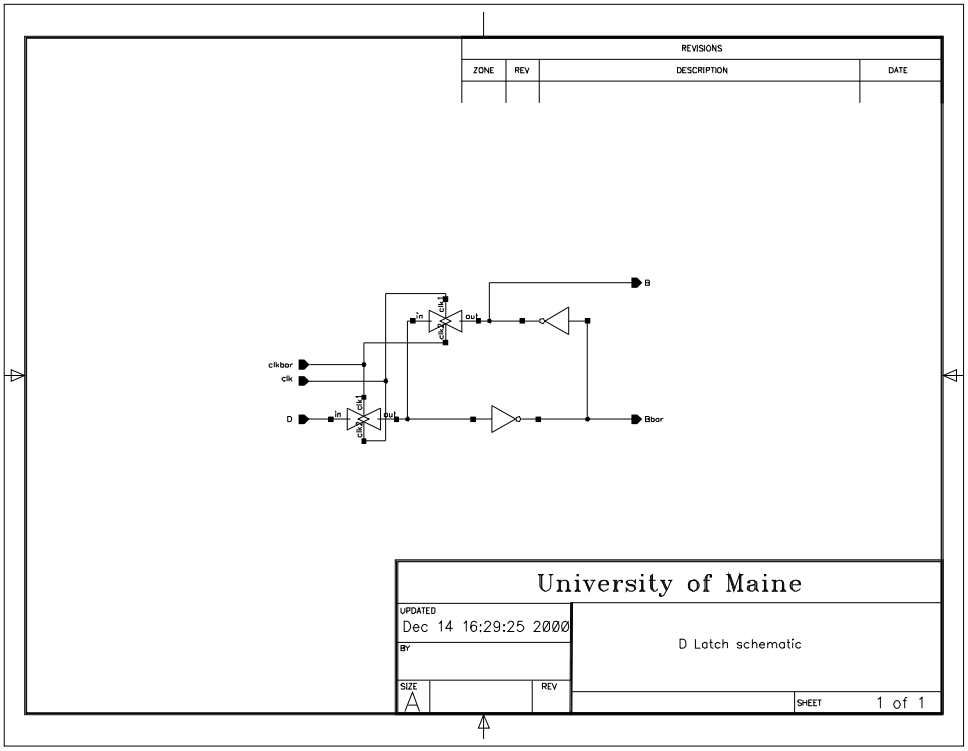


Figure 6: Inverter Schematic

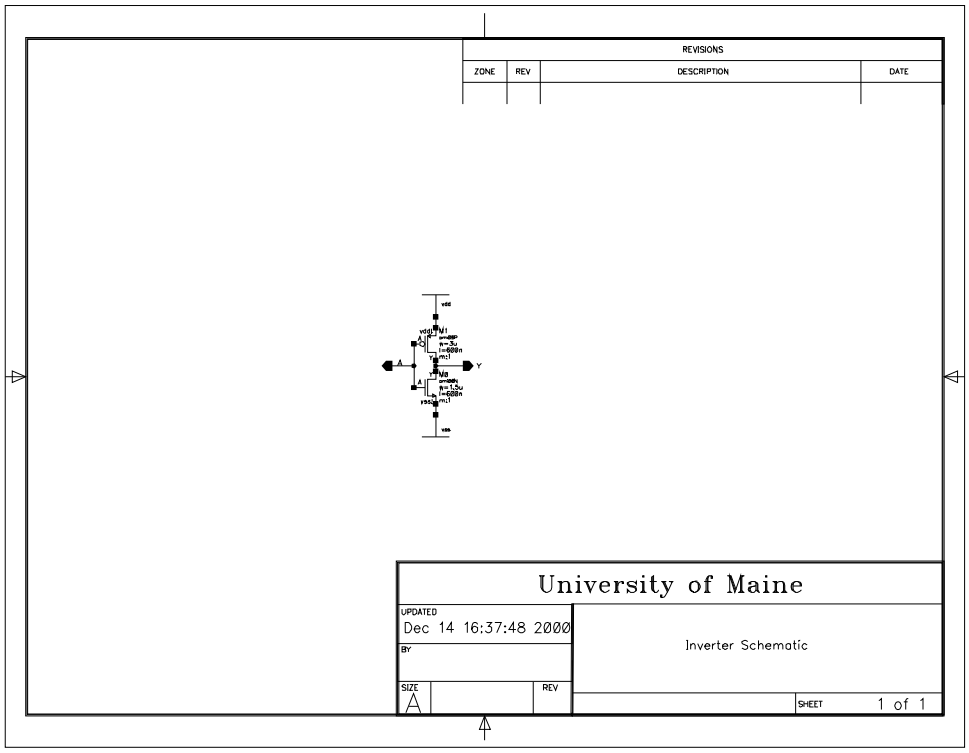


Figure 7: Buffer Schematic

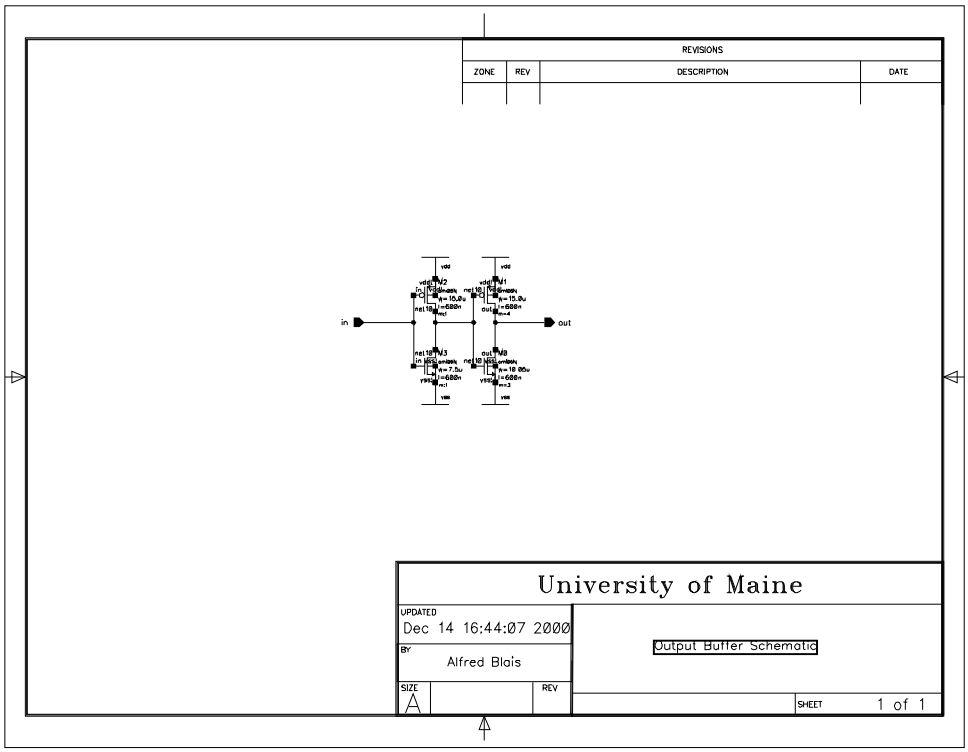


Figure 8: Transmission Gate

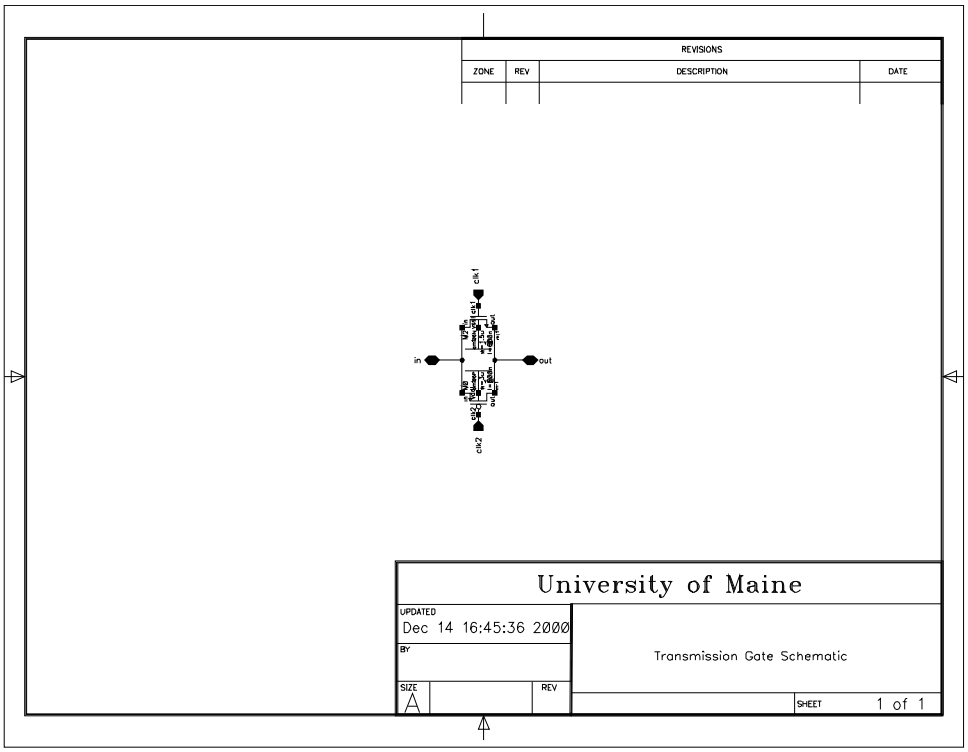
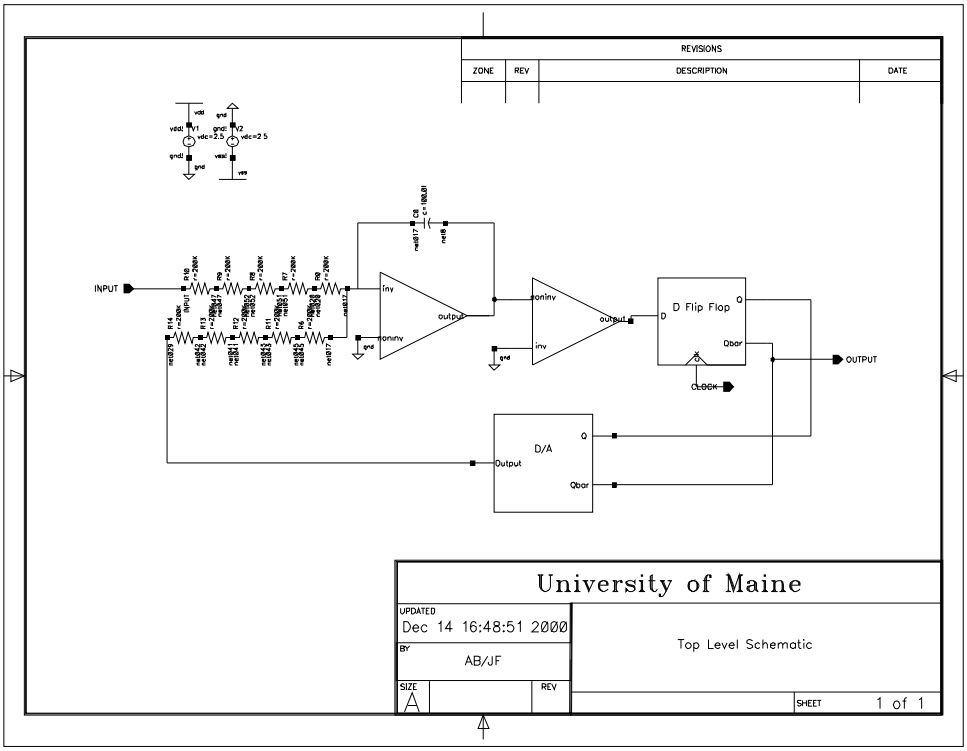


Figure 9: Top Level Schematic



APPENDIX B:

Figure 1: D/A Layout

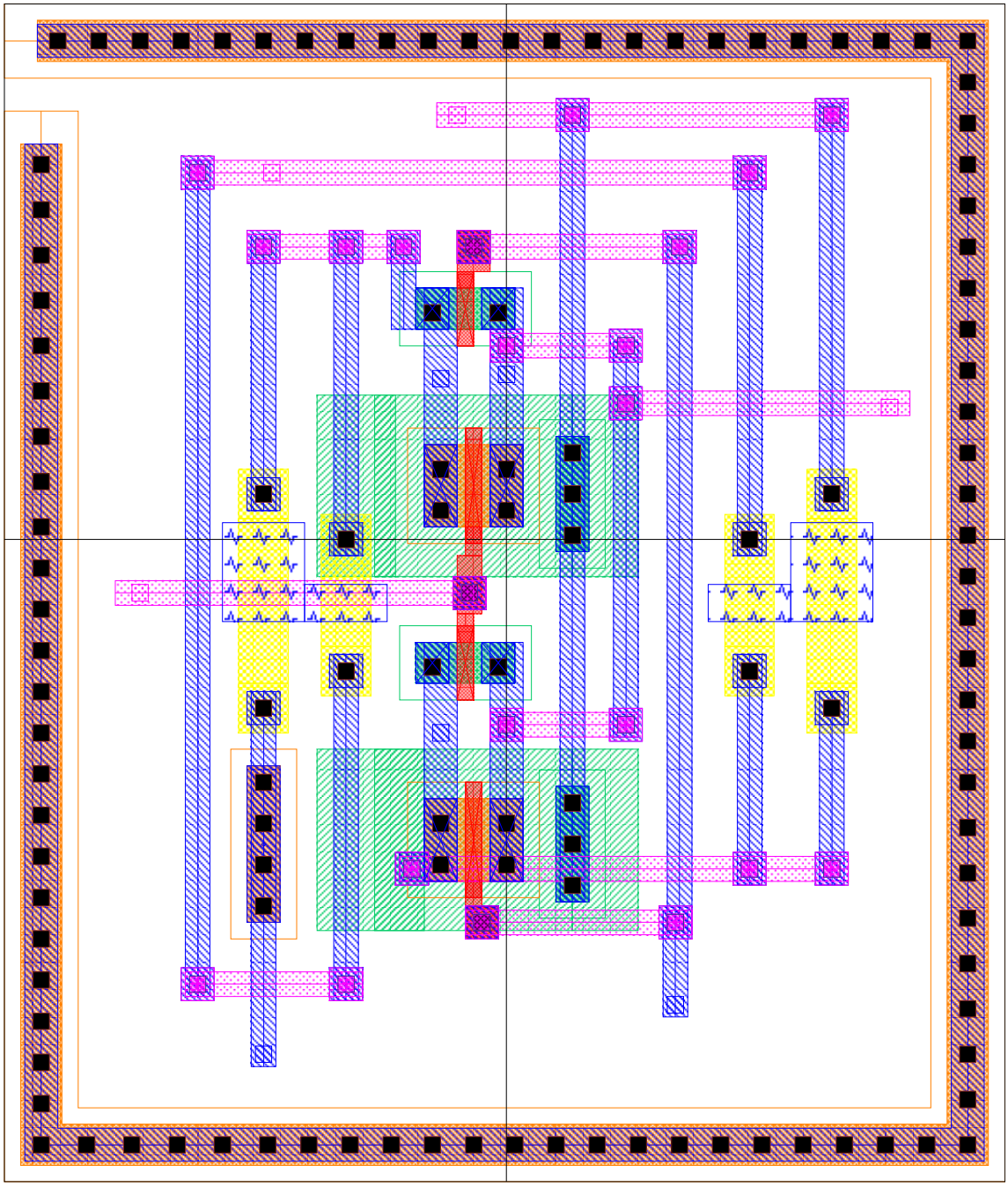


Figure 2: D Flip−Flop Layout

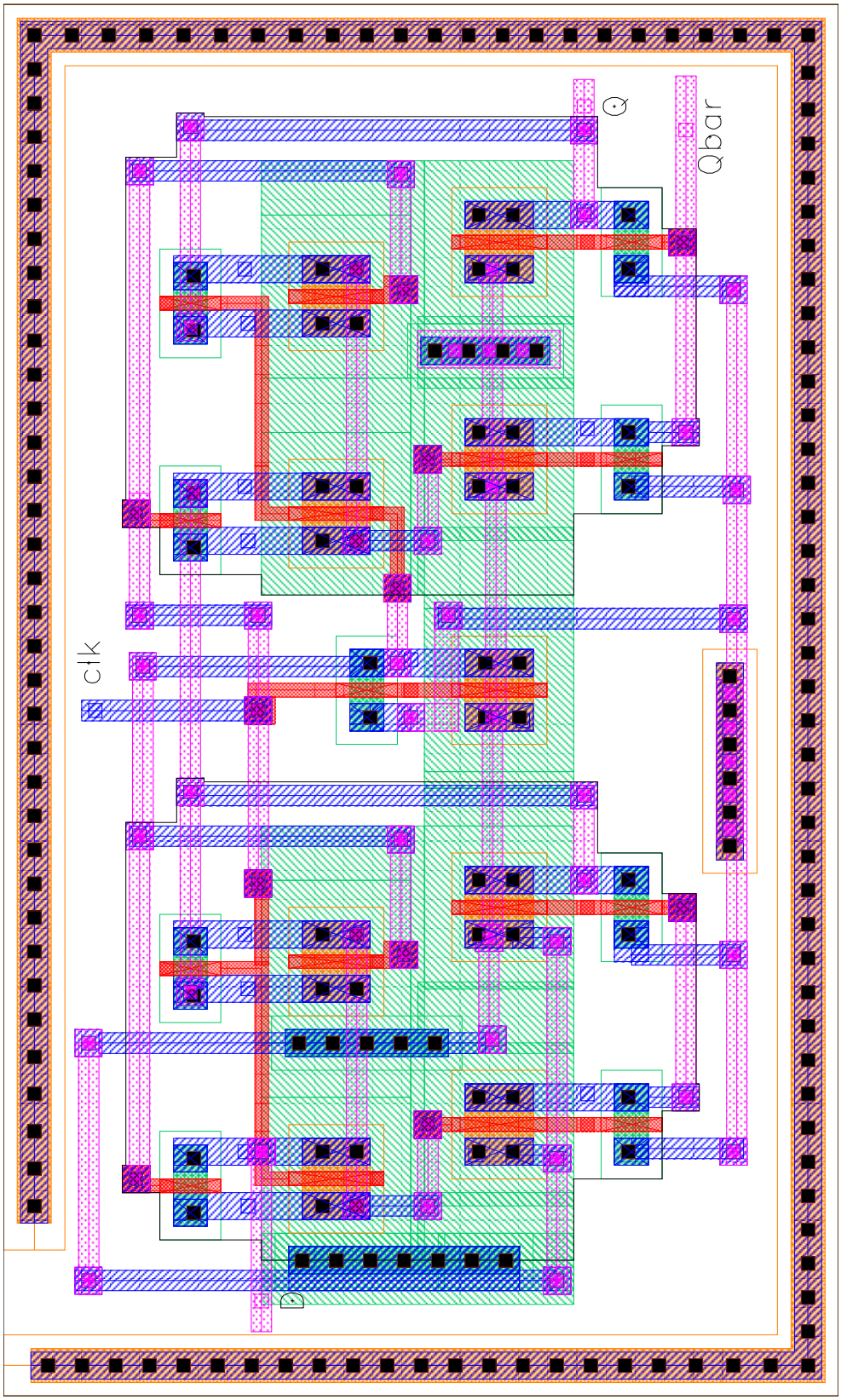


Figure 3: Comparator Layout

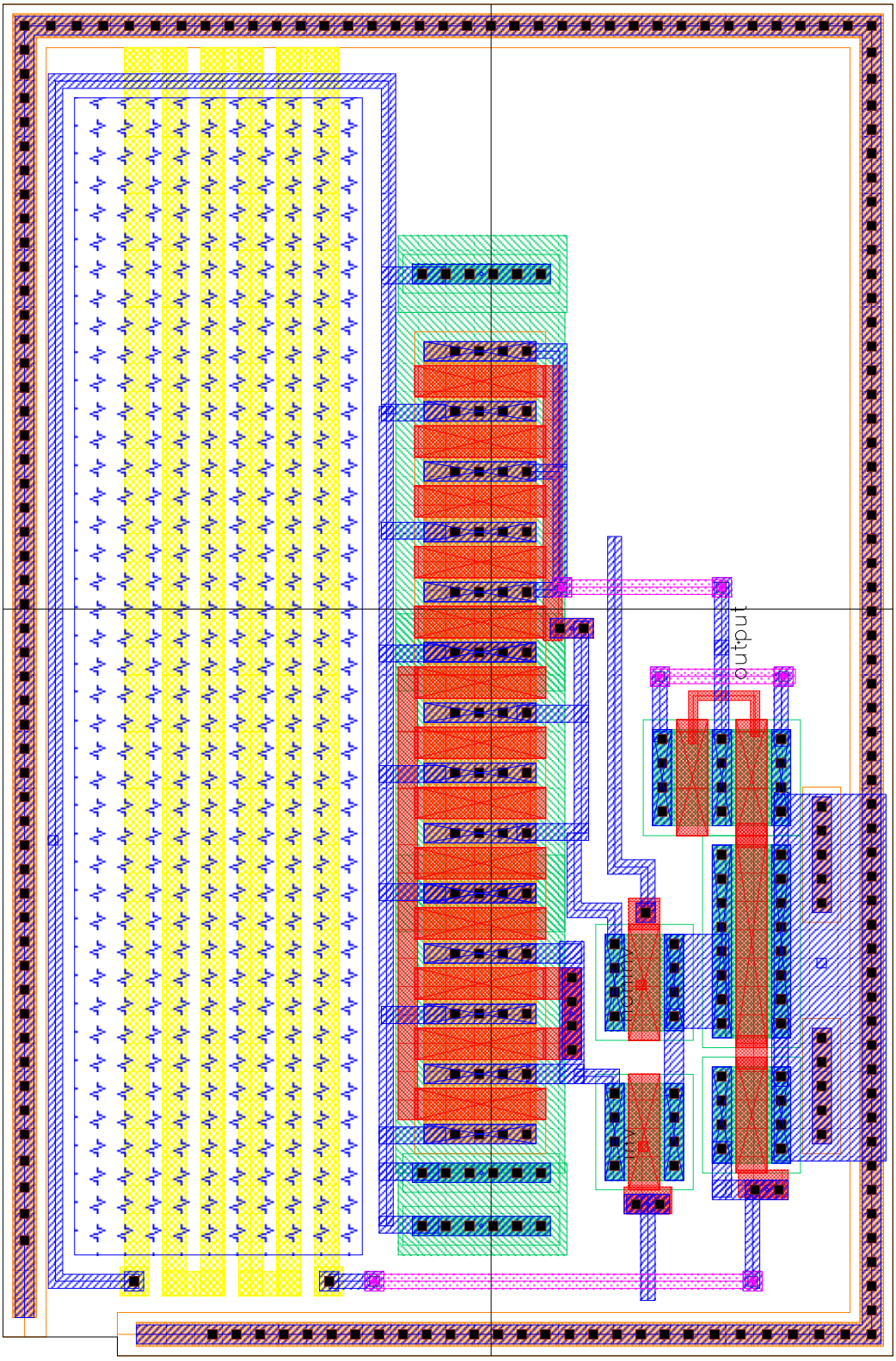


Figure 4: Operational Amplifier Layout

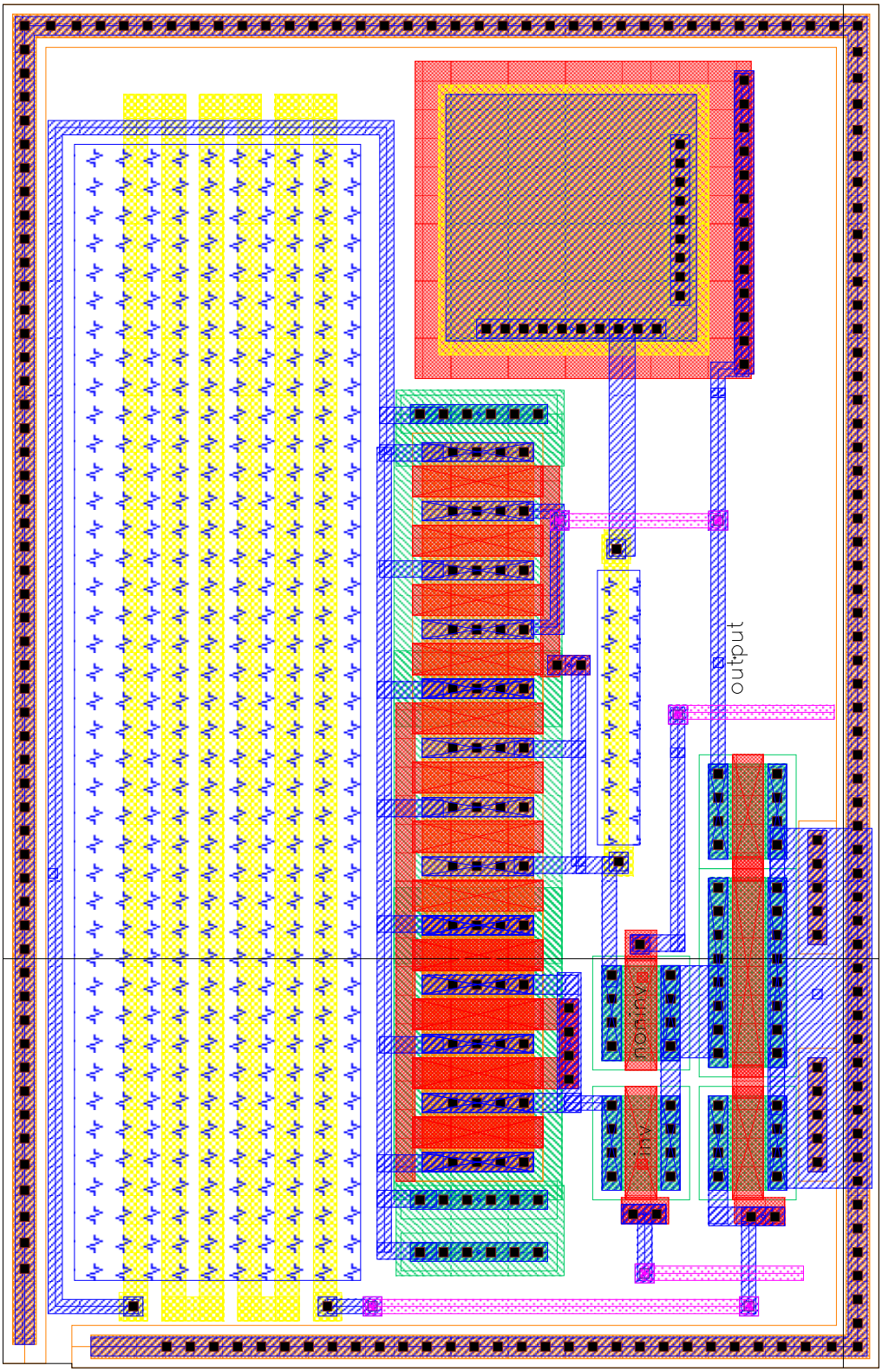


Figure 5: Top Level Layout

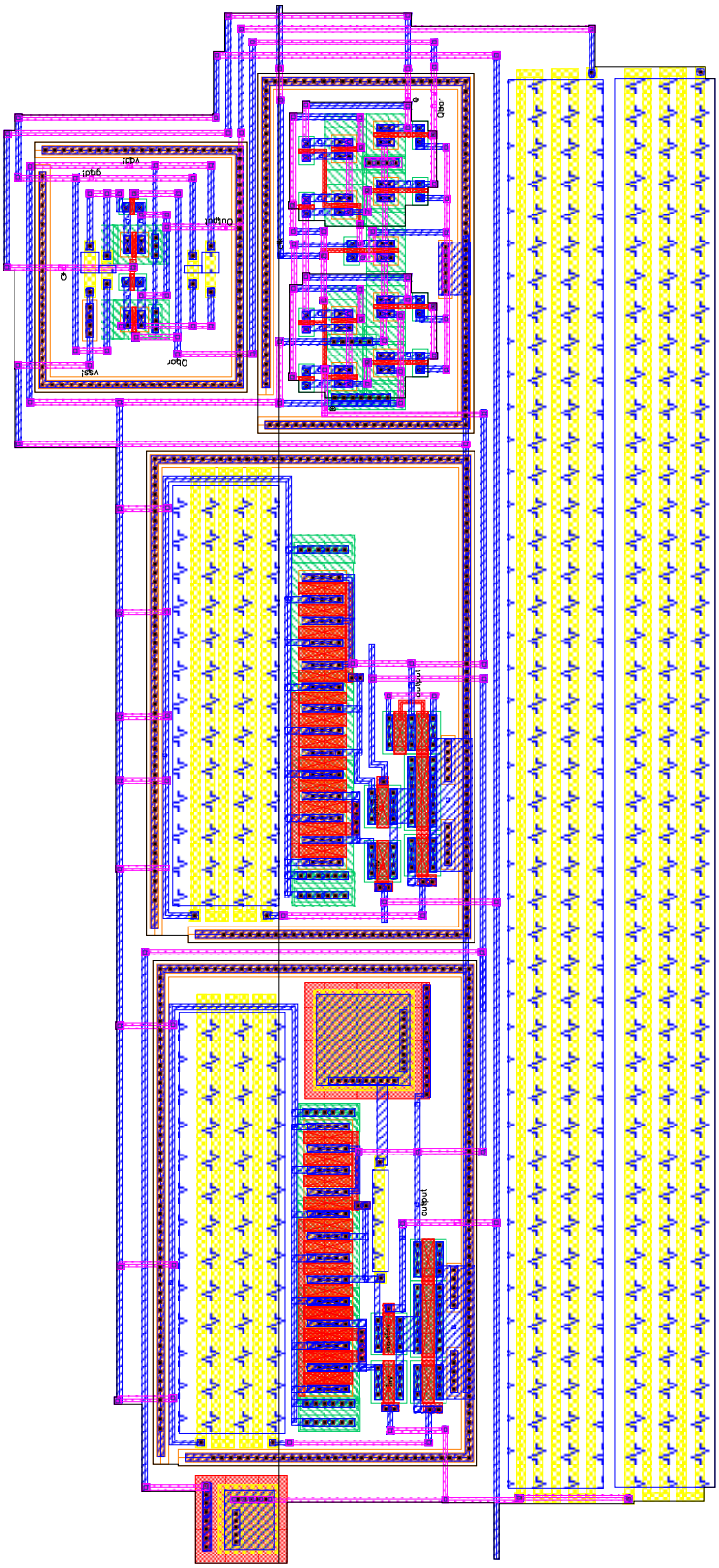


Figure 6: Chip Level Layout

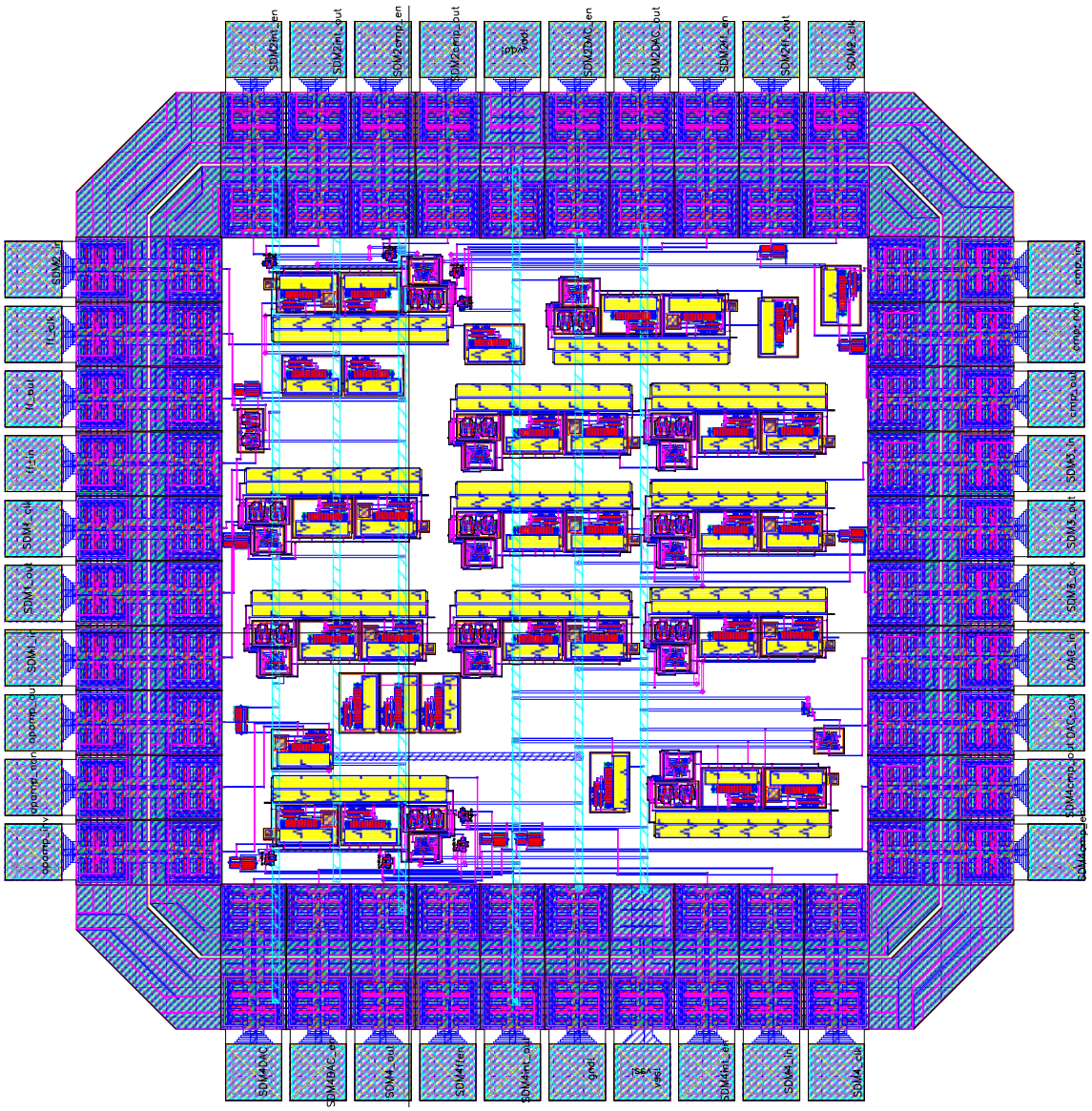
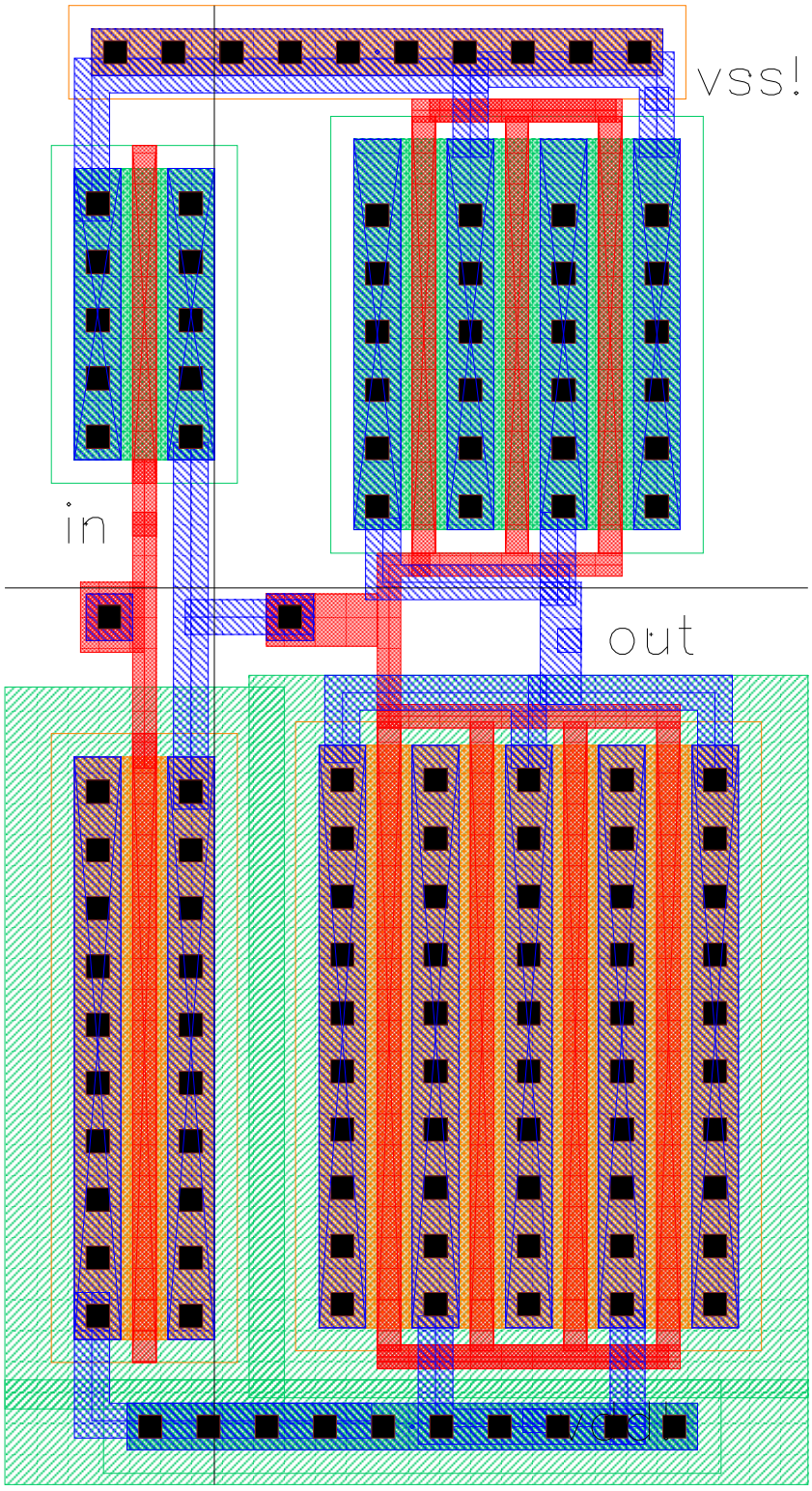


Figure 7: Buffer Layout



APPENDIX C:

Chip Level LVS Output

@(#)$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $

Like matching is enabled.
Net swapping is enabled.
Creating /usr/data/ECE547_Fall00/Sigma_Delta/LVS/xref.out file.
Fixed device checking is enabled.
Using terminal names as correspondence points.

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout/netlist

count	
684	nets
40	terminals
389	res
25	cap
1102	pmos
855	nmos

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic/netlist

count	
684	nets
40	terminals
389	res
25	cap
319	pmos
387	nmos

Terminal correspondence points

1	DAC_in
2	DAC_out
3	SDM1_clk
4	SDM1_in
5	SDM1_out
6	SDM2DAC_en
7	SDM2DAC_out
8	SDM2_clk
9	SDM2_in
10	SDM2cmp_en
11	SDM2cmp_out
12	SDM2ff_en
13	SDM2ff_out
14	SDM2int_en
15	SDM2int_out

16	SDM3_clk
17	SDM3_in
18	SDM3_out
19	SDM4DAC
20	SDM4DAC_en
21	SDM4_clk
22	SDM4_in
23	SDM4_out
24	SDM4cmp_en
25	SDM4cmp_out
26	SDM4ffen
27	SDM4int_en
28	SDM4int_out
29	cmp_inv
30	cmp_non
31	cmp_out
32	ff_clk
33	ff_in
34	ff_out
35	gnd!
36	opamp_inv
37	opamp_non
38	opamp_out
39	vdd!
40	vss!

The net−lists match.

	layout	schematic	
	instances		
un−matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	2371	1120	
total	2371	1120	
	nets		
un−matched	0	0	
merged		0	0
pruned	0	0	
active	684	684	
total	684	684	
	terminals		
un−matched	0	0	
matched but different type	0	0	

total 40 40

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Comparator LVS Output

@(#)$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $

Like matching is enabled.
Net swapping is enabled.
Creating /usr/data/ECE547_Fall00/Sigma_Delta/LVS/xref.out file.
Fixed device checking is enabled.
Using terminal names as correspondence points.

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout/netlist

count	
14	nets
5	terminals
6	res
13	pmos
6	nmos

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic/netlist

count	
14	nets
5	terminals
6	res
3	pmos
5	nmos

Terminal correspondence points

1	inv
2	noninv
3	output
4	vdd!
5	vss!

The net−lists match.

	layout	schematic	
	instances		
un−matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	25	14	
total	25	14	
	nets		
un−matched	0	0	

merged		0	0
pruned	0	0	
active	14	14	
total	14	14	
	terminals		
un−matched	0	0	
matched but different type	0	0	
total	5	5	

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

D/A LVS Output

@(#)$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $

Like matching is enabled.
Net swapping is enabled.
Creating /usr/data/ECE547_Fall00/Sigma_Delta/LVS/xref.out file.
Fixed device checking is enabled.
Using terminal names as correspondence points.

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout/netlist

count	
8	nets
6	terminals
4	res
2	pmos
2	nmos

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic/netlist

count	
8	nets
6	terminals
4	res
2	pmos
2	nmos

Terminal correspondence points

1	Output
2	Q
3	Qbar
4	gnd!
5	vdd!
6	vss!

The net−lists match.

	layout	schematic	
	instances		
un−matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	8	8	
total	8	8	
	nets		
un−matched	0	0	
merged		0	0

pruned	0	0
active	8	8
total	8	8
	terminals	
un−matched	0	0
matched but different type	0	0
total	6	6

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

D Flip−Flop LVS Output

@(#)$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $

Like matching is enabled.
Net swapping is enabled.
Creating /usr/data/ECE547_Fall00/Sigma_Delta/LVS/xref.out file.
Fixed device checking is enabled.
Using terminal names as correspondence points.

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout/netlist

count	
11	nets
4	terminals
9	pmos
9	nmos

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic/netlist

count	
11	nets
6	terminals
9	pmos
9	nmos

Terminal correspondence points

1	D
2	Q
3	Qbar
4	clk

The net−lists match.

	layout	schematic	
	instances		
un−matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	18	18	
total	18	18	
	nets		
un−matched	0	0	
merged		0	0
pruned	0	0	
active	11	11	
total	11	11	

	terminals	
un−matched	0	0
matched but different type	0	0
total	4	6

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Op Amp LVS Output

@(#)$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $

Like matching is enabled.
Net swapping is enabled.
Creating /usr/data/ECE547_Fall00/Sigma_Delta/LVS/xref.out file.
Fixed device checking is enabled.
Using terminal names as correspondence points.

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout/netlist

count	
15	nets
5	terminals
7	res
1	cap
12	pmos
5	nmos

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic/netlist

count	
15	nets
5	terminals
7	res
1	cap
3	pmos
5	nmos

Terminal correspondence points

1	inv
2	noninv
3	output
4	vdd!
5	vss!

The net−lists match.

	layout	schematic	
	instances		
un−matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	25	16	
total	25	16	

nets

un−matched	0	0	
merged		0	0
pruned	0	0	
active	15	15	
total	15	15	
	terminals		
un−matched	0	0	
matched but different type	0	0	
total	5	5	

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Top Level LVS Output

@(#)$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) $

Like matching is enabled.
Net swapping is enabled.
Creating /usr/data/ECE547_Fall00/Sigma_Delta/LVS/xref.out file.
Fixed device checking is enabled.
Using terminal names as correspondence points.

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout/netlist

count	
45	nets
0	terminals
27	res
2	cap
36	pmos
22	nmos

Net−list summary for /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic/netlist

count	
45	nets
6	terminals
27	res
2	cap
17	pmos
21	nmos

The net−lists match.

	layout	schematic	
	instances		
un−matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	87	67	
total	87	67	
	nets		
un−matched	0	0	
merged		0	0
pruned	0	0	
active	45	45	
total	45	45	
	terminals		
un−matched	0	0	

matched but different type	0	0
total	0	6

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/data/ECE547_Fall00/Sigma_Delta/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

APPENDIX D:

Figure 1: First Order Sigma−Delta Modulator Block Diagram

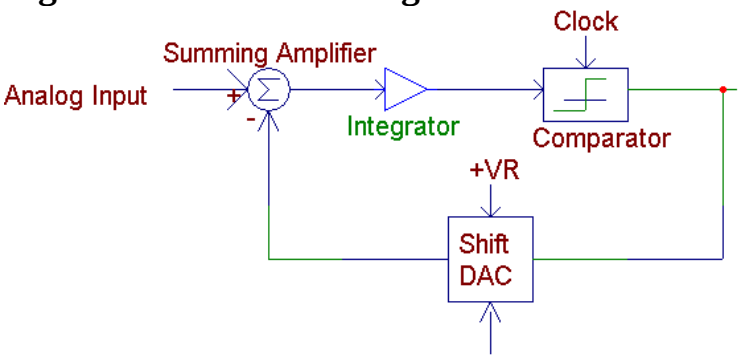


Figure 2: First Order Sample Output

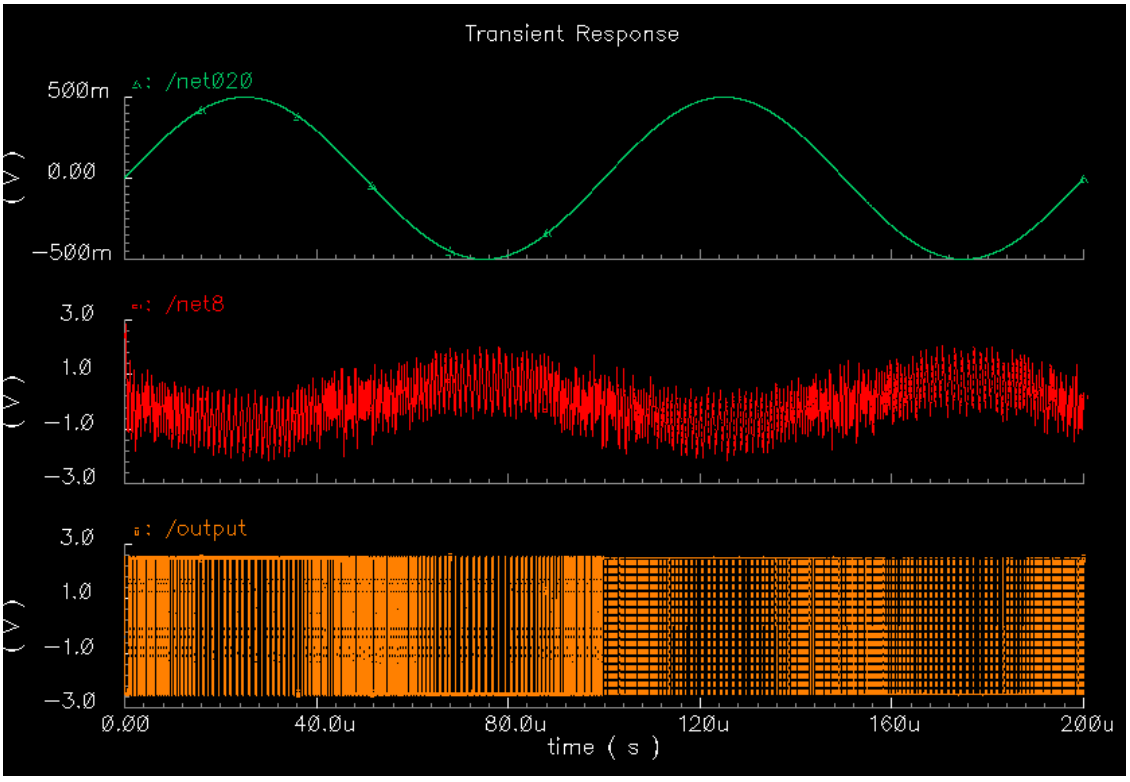
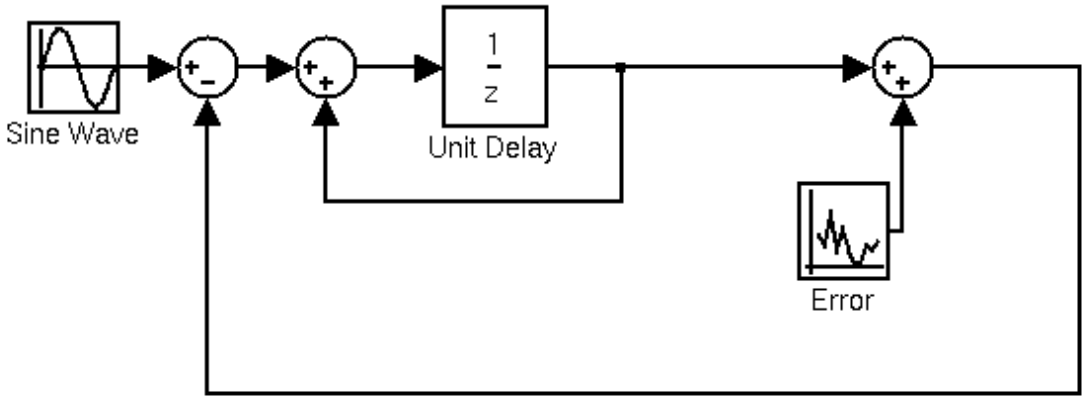
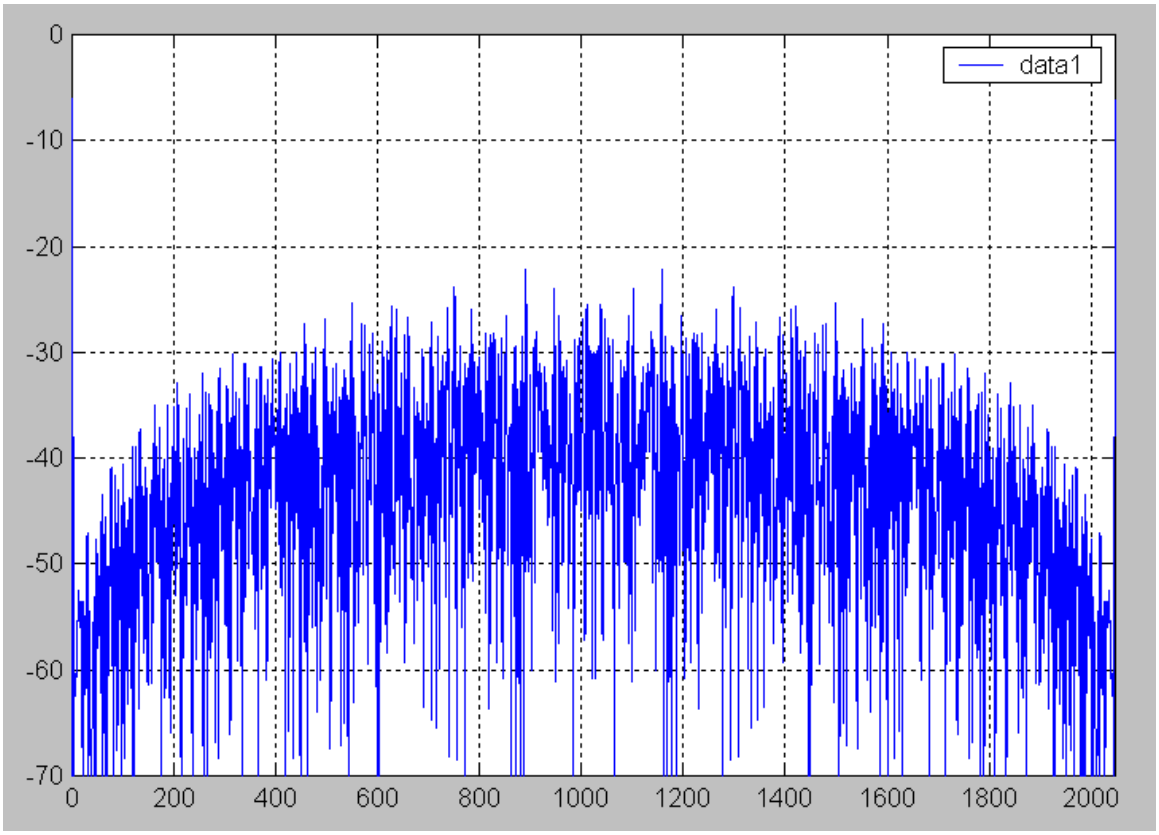


Figure 3: Z−Domain Linear Model



Error transfer function H(z)=(1−1/Z)E(z)
Signal transfer function H(z)=(1/Z)X(z)
Where X(z) is signal, E(z) is quantization error

Figure 4: Matlab/Simulink Simulation Results



# of bins

Figure 5: Op Amp Open Loop Frequency Response

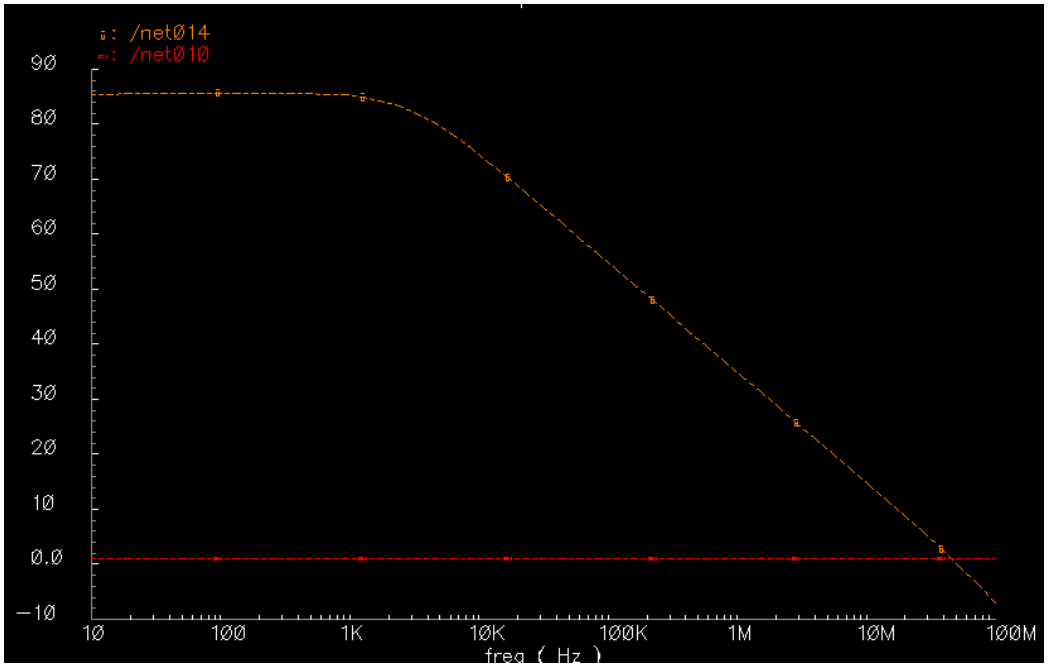
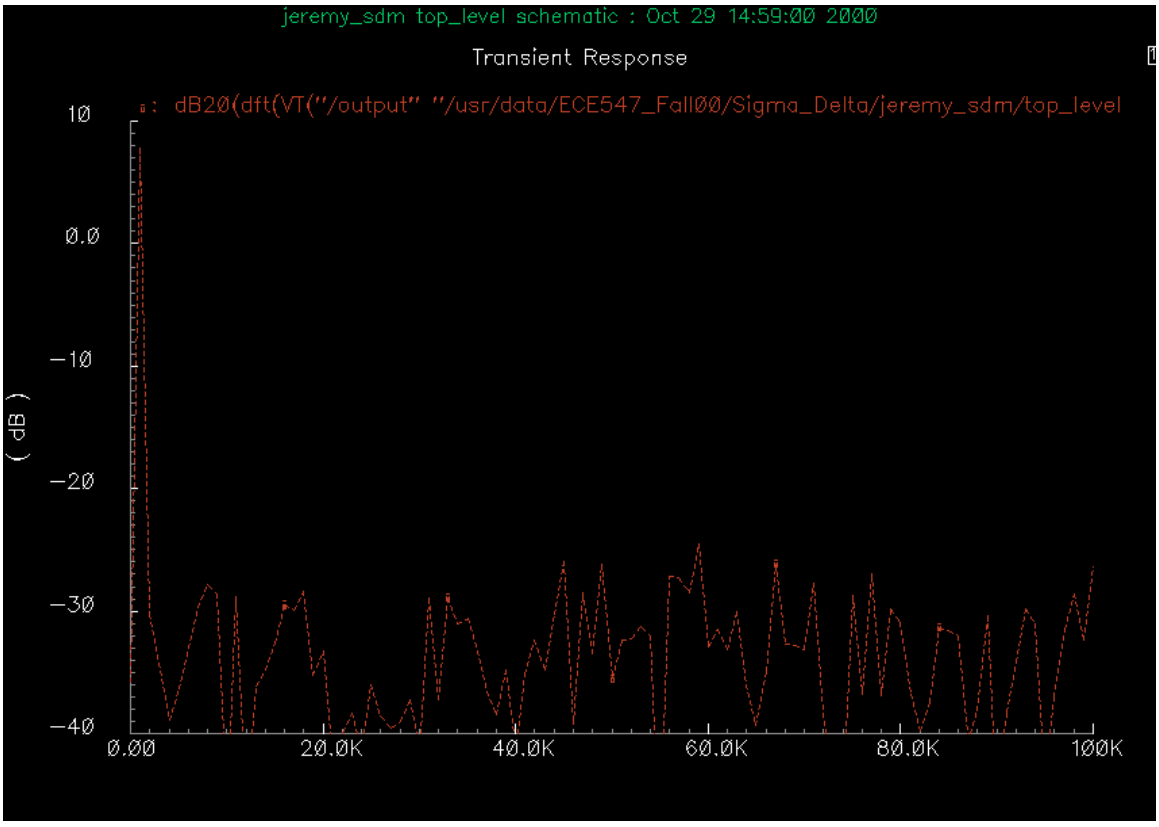


Figure 6: Top level Simulation Results



Appendix E:

Biography of Authors

Jeremy Ferris is a senior electrical engineering student at the University of Maine. He has previously worked on IBIS models, reverse engineered an 8−bit buffer and worked on analog to digital converters as a co−op at Quadic Systems.

Alfred Blais is a senior electrical engineering student at the University of Maine. He has previously worked in capital projects at International Paper Company and also has worked on analog to digital converter designs as a co−op at Quadic Systems.