Design of a 8-bit CMOS Unit-Element Current-Steering Digital-to-Analog Converter

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Abstract

The report discusses pros and cons of different topologies of digital-to-analog converters. And then chooses unit-element current-steering architecture in this project. The goal is to design an eight-bit digital-to-analog converter which is supplied by 5V power and works at 50MHz or higher clock frequency. The overall design includes four major parts----eight identical registers to get stable signals from digital inputs; row and column decoders to convert binary signals to thermometer codes; a current cell array consisting of 16*16 current cells whose output currents are controlled by thermometer codes; op-amp stage to transform current difference in the current cell array to analog output voltage.

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I Introduction

1.1 DAC

Digital-to-Analog converter (DAC) is a device converting digital (usually binary) codes to analog signals (for example, current, voltage). It is more and more widely used in this “digital world”. For example, most modern audio signals are stored in digital form (such as MP3s, MP4s and CDs) and they need to be transferred into analog signal in order to be heard. Thus, DACs are used in MP3 players, MP4 players and CD players. Also video signals from digital sources, such as computers, need to be converted to analog signals if they are to be displayed on an analog monitor.

1.2 DAC types

There are several different topologies for DAC, such as resistor string architecture, resistor ladder architecture, charge division architecture, current division architecture and current steering architecture. Each of them has pros and cons.

1.2.1 Resistor string architecture

The simplest DAC topology is resistor string architecture. It consists of 2^N identical resistors and switches, the analog output is the voltage division of the resistors. This structure results in good accuracy and is inherently monotonic. This is also fast for 8-10 bits DAC and compatible with purely digital technologies. The disadvantage of this topology is that the output is always connected to 2^N -1 switches in “off” state and one switch in “on” state. When resolution becomes a big value, a large parasitic capacitance appears at the output and conversion speed becomes much slower. Also this architecture occupies large area. In addition, the settling time is large, especially for DAC with 10 bit or higher resolution. [1]

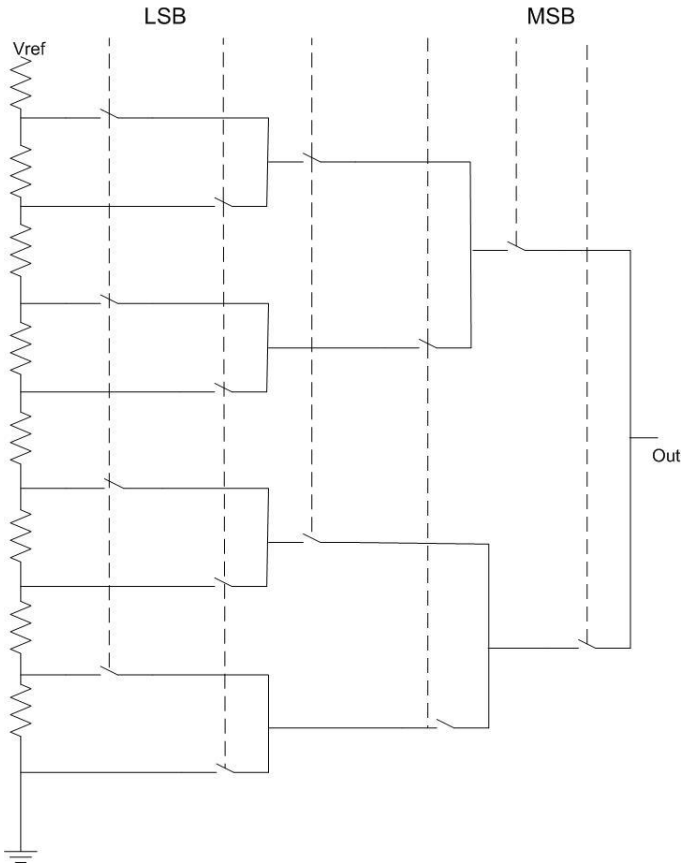

Fig.1. 1 Resistor String DAC

1.2.2 Resistor ladder architecture

Another DAC is called R-2R ladder network which consists of resistors R and 2R. For example, analyzing a 3-bit resistor ladder DAC is as follows:

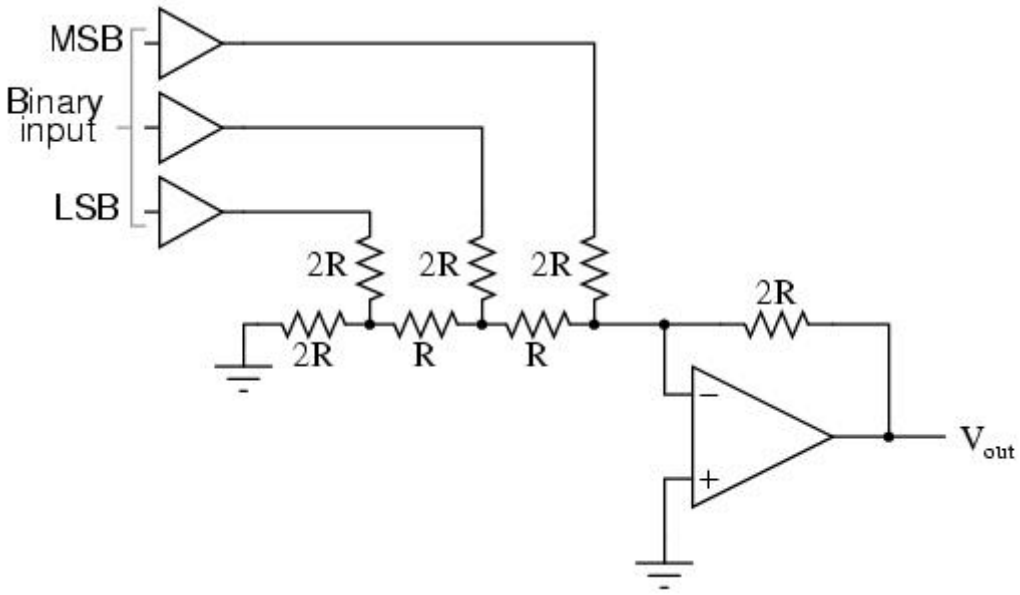

Fig.1. 2 Resistor Ladder DAC

Mathematically analyzing this ladder network is a bit more complex, a where each input resistor provided an easily-calculated gain for that bit. Thevenin's theorem and simulation program like SPICE can be used for each binary input to determine circuit response.

Table 1 3-bit resistor ladder DAC output

Binary	Output Voltage (V)
000	0
001	-1.25
010	-2.5
011	-3.75
100	-5
101	-6.25
110	-7.5
111	-8.75

The value of the feedback resistor can be modified to obtain any desired "span". For example, when using +5 volts for a "high" voltage level and 0 volts for a "low" voltage level, an analog output directly corresponding to the binary input (011 = -3 volts, 101 = -5 volts, 111 = -7 volts, etc.) can be obtained by using a feedback resistance with a value of 1.6R instead of 2R. [2]

1.2.3 Charge division architecture

Charge division DAC is popular in CMOS technology. From Fig. 1.3, Capacitors C1 to CN are all identical, and each capacitor inject the amount of charge $Q = C*V_{REF}$ to the output node. Each switch is controlled by the digital thermometer code, and thus the number of nodes turned on determines the charge on the output node. [3]. Other topologies can also be implemented in a binary version by using different capacitors.

A significant problem with charge -division architectures is that building capacitors takes up a substantial amount of chip area. Also several nonlinearities arise and this type DAC becomes relatively inaccurate.

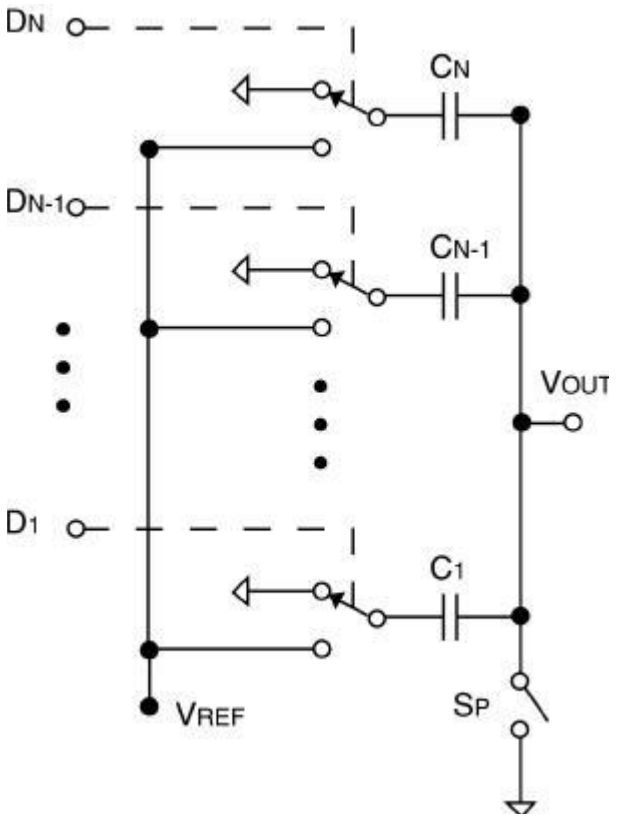

Fig.1. 3 Charge Division DAC

1.2.4 Current division architecture

Typical current division architecture is shown in Fig. 1.4. The four devices on the leftmost side draw 4/7 of the reference current, while the center and right sides draw 2/7 and 1/7 of the reference, respectively. The selected currents add, giving the analog current representation of the digital input. Two major drawbacks exist in this topology. First, the stack of current dividing transistors positioned above I_{REF} reduces the available output voltage range, and thus impractical in low voltage circuits. Second, since each device divides the reference current, I_{REF} must be N times greater than each of the output currents. This can require a huge device to provide the current source. [3]

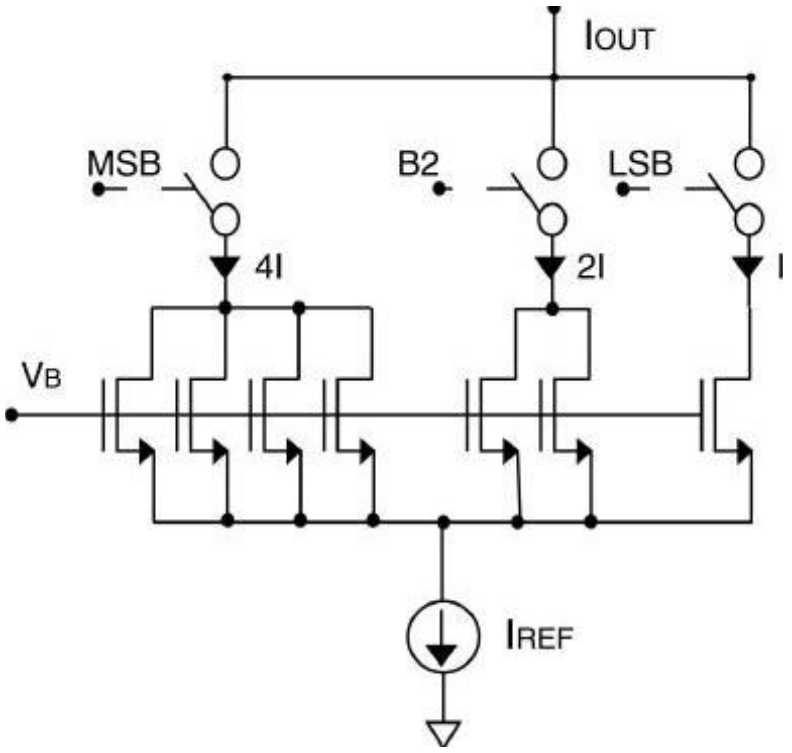

Fig.1. 4 Current Division DAC

1.2.5 Current steering architecture

Current steering architecture replicates a reference current source rather than divides it in each branch of the DAC. Each branch current is switched on or off based on the input codes. [4] The architecture can achieve high speed at the cost of complex structure and relatively large power and chip area. The key part is a precise current source. There are two different kinds of current-steering DAC----binary current–steering and unit-element current-steering. The architectures o

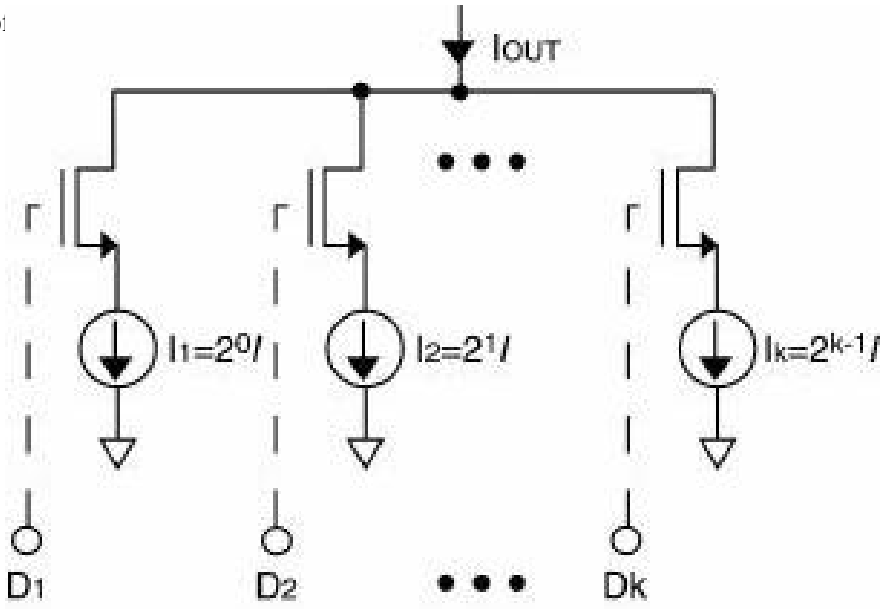

Fig.1. 5 Binary Current-Steering DAC

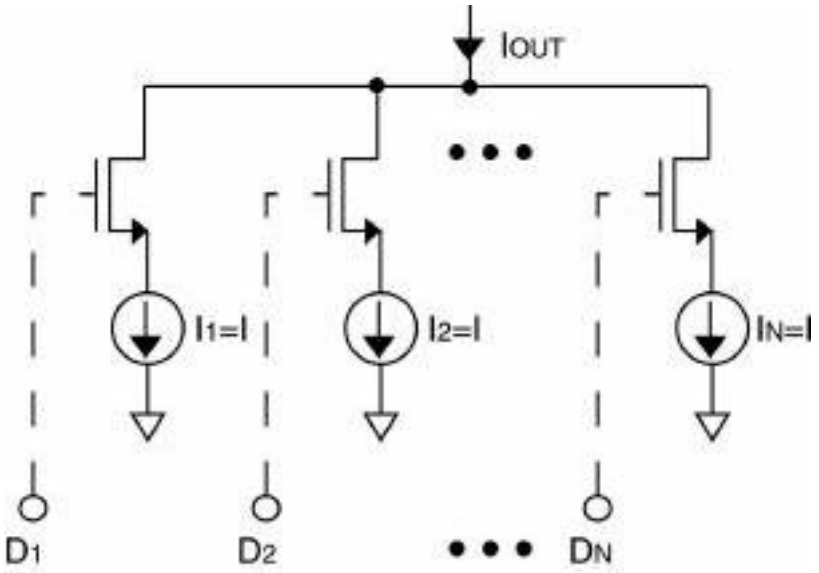

Fig.1. 6 Unit-element Current-Steering DAC

In binary type, the reference current is multiplied by two and larger currents represent higher magnitude digital signals. While in unit-element architecture, each branch produces equal currents, and 2^N current source elements are needed for the N bit DAC. Therefore, when the digital input increases by 1 LSB, one addition current source is turned on and avoid the problem of two signals switching to opposite directions simultaneously.

Unit-element current steering has better performance than binary ones in the following aspects.
First, it can obtain higher speed. It has inherently high current and thus widely used in high-speed cases. It is traditionally fabricated with bipolar technology, but now CMOS becomes a good alternative because of matched current mirrors. Secondly, the matching performance is better. Since each current source is identical, the current produced in each branch is the same. Finally, it can ensure monotonicity. That is, the digital input increments in either direction, analog output is varied by one switch turning on or off and this type reduce glitches in this aspect.

But its drawbacks are that it has complex structure. And since it needs 2^N current sources, it occupies large area, leading to large power consumption. It is obvious to see this point from the overall layout of this project which will be shown later.

1.3 Design Specifications

This design chooses unit-element current-steering topology. There are four major portions in this design:
(1) Register
(2) Binary-to-thermometer decoder
(3) Current source array
(4) Differential op-amp

8-bit digital inputs' glitches can be eliminated after registers, and by decoders, they are changed to 15*15 thermometer signals. These signals perform as controlled codes to determine how many current cells are on/ off and the values of Iout and Iout_neg. Finally, in the last stage, the difference between the inputs of differential amplifiers can be amplified and serve as the analog output.

The project's goal is to work in 50MHz (clock frequency) (LSB will work at 25MHz) and higher frequency. This is an 8-bit DAC at 5V and 0V. The ultimate simulation shows that it can perform well in 10MHz but have some problems with the settling time in 50MHz which will be discussed later.

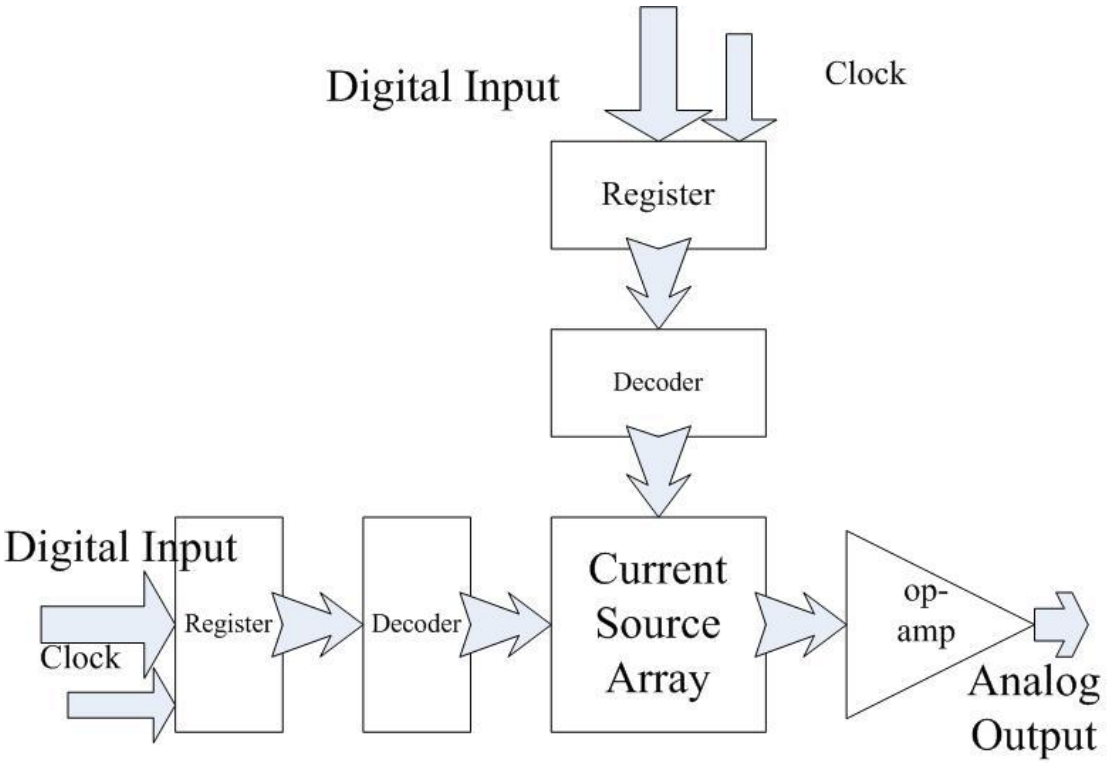

Fig.1. 7 Overall Structure of unit-element current-steering DAC

This design report totally has nine parts. In the first part, DAC applications, types and the goal in this project is illustrated. The following four parts （part 2 to part 5）describe each portion of this design separately, including the register, the binary-to-thermometer decoder, the current-cell array and op-amp with buffer. Part 6 introduces the overall design. Then specific details with pad and layout are demonstrated, separately in part 7 and 8. In the last part, issues about this project and the future development are discussed.

II Register

2.1 Schematic

Register is used to get a stable output from the digital input, that is, to eliminate glitches. There are different types of registers. The master-slave positive edge-triggered register is used in this project. It contains two cascading latches, one is negative (master stage) and the other is positive (slave stage). When the clock is in low stage, the lower position's transmission gate in the left is on and the higher position's transmission gate in the left is off, so the input D is passed to the master stage output. Also the lower position's transmission gate in the right is off and the higher position's transmission gate in the right is on. Coupled inverters on the right side hold the state of the slave latch. When the clock is in high stage, it goes into a hold mode. Coupled inverters on the left side hold the state of the output of master stage, which is then copied to the output of the register. [5]

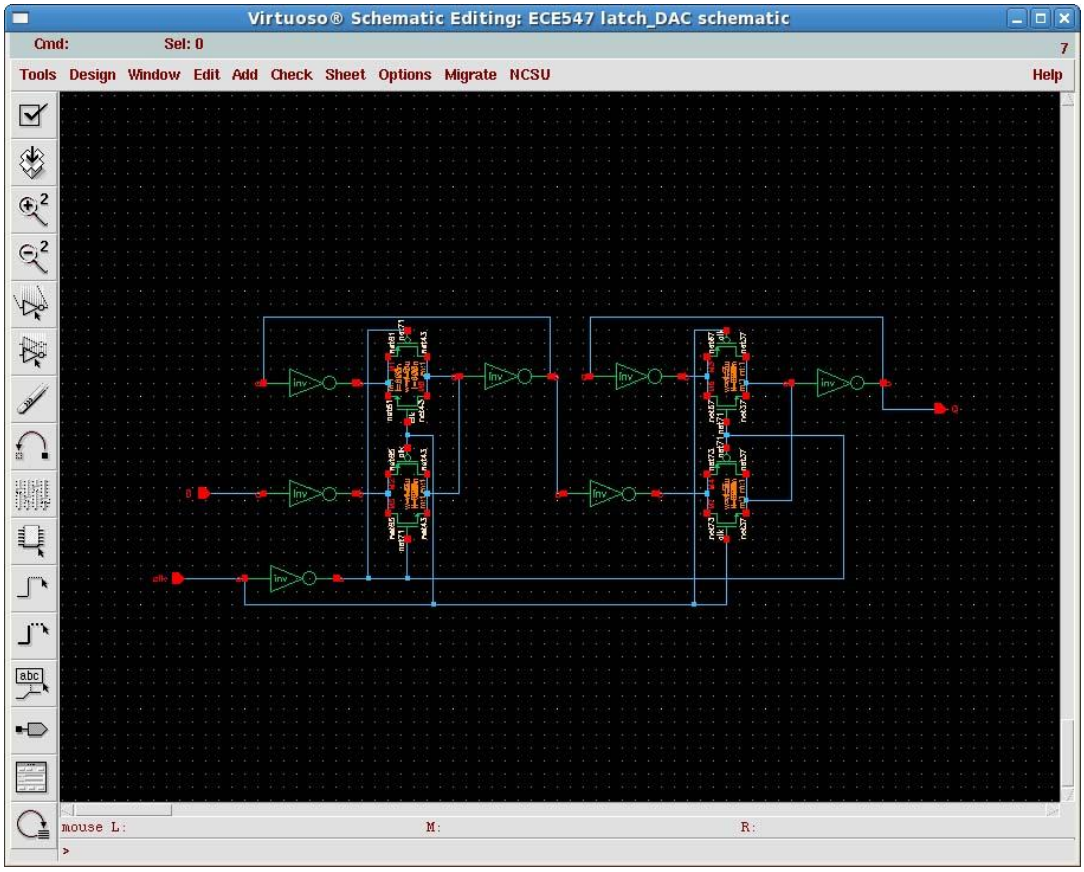

Fig.2. 1 Schematic of the master-slave register

2.2 Simulation Results

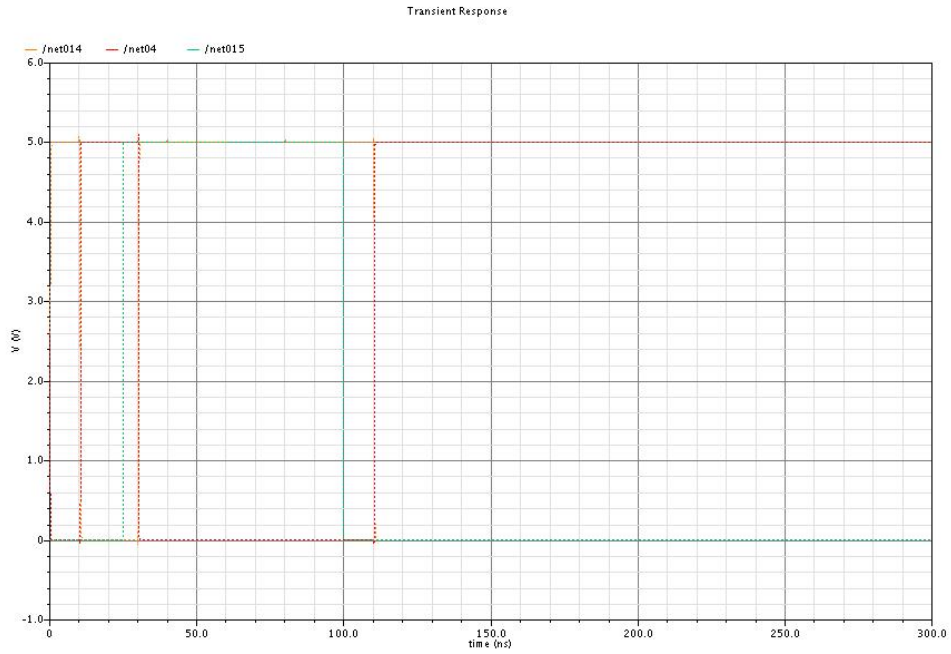

Fig.2. 2 Simulation result of the register

Simulation result at clock frequency of 100MHz is shown in Fig 2.2. Though the output has delay compared to input signal, the delay can be neglected because of its small value.

III Binary-to-thermometer decoder

3.1 Binary and thermometer codes

The decoder converts binary codes to thermometer ones. Thermometer code, so named because it is similar to a mercury thermometer, where the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. [6] For example, the Binary Code is shown with a length of 3 can represent 2^3=8 separate categories. And 16 bit thermometer codes can be represented by binary ones in a length of 4, and so on.

Although the thermometer codes need much more bits than their counterparts, especially when bit is large, they have advantages in only changing one bit every time to avoid glitches. For example, when binary code switches from 0111 to 1000, four bits change simultaneously and this may cause glitches. While thermometer codes, switching from 000 0000 0111 1111 to 000 0000 1111 1111, only change one bit and avoid glitches effectively.

Table2 Binary-to-thermometer Truth Table

Binary	Thermometer
0000	000 0000 0000 0000
0001	000 0000 0000 0001
0010	000 0000 0000 0011
0011	000 0000 0000 0111
0100	000 0000 0000 1111
0101	000 0000 0001 1111
0110	000 0000 0011 1111
0111	000 0000 0111 1111
1000	000 0000 1111 1111
1001	000 0001 1111 1111
1010	000 0011 1111 1111
1011	000 0111 1111 1111
1100	000 1111 1111 1111
1101	001 1111 1111 1111
1110	011 1111 1111 1111
1111	111 1111 1111 1111

3.2 Schematic

According to the truth table above, the logical relationship can be expressed as follows:

t1=b1+b2+b3+b4

t2=b1+b2+b3

t3=b1+b2+b3*b4

t4=b1+b2

t5=b1+b2*(b3+b4)

t6=b1+b2*b3

t7=b1+b2*b3*b4
t8=b1
t9=b1*(b2+b3+b4)
t10=b1*(b2+b3)
t11=b1*(b2+b3*b4)
t12=b1*b2
t13=b1*b2*(b3+b4)
t14=b1*b2*b3
t15=b1*b2*b3*b4
b1 is the most significant bit (MSB) and b4 is the least significant bit (LSB) of binary codes while t1 is LSB and t15 is MSB of thermometer codes.

The schematic of this decoder is in Fig 3.1. Inverters are added to obtain similar delay time in every branch of the decoder's output while retain the same logic. Each symbol represent a lower level schematic, such as AND, OR gate and inverter. Schematics of these symbols are shown in the appendix A1.

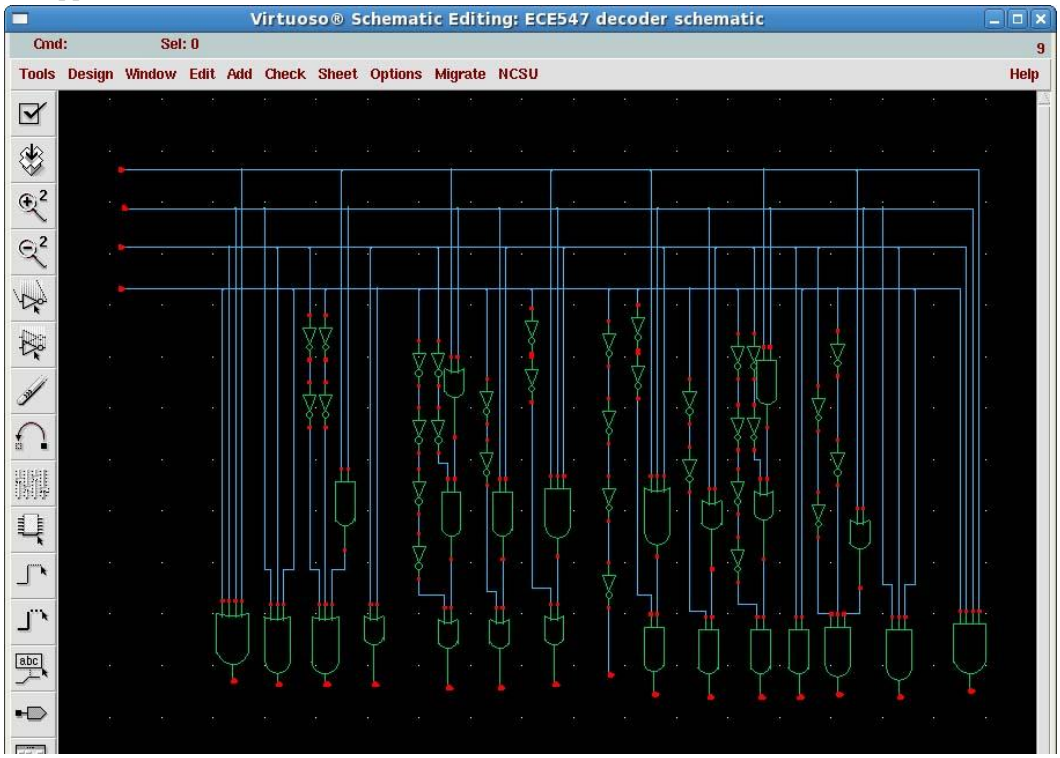

Fig.3. 1 Decoder Schematic

3.3 Simulation Result

The simulation result is shown from Fig 3.2 to Fig 3.5. From the figure, the overall output performance is good although small glitches and delay exist. After decoding, there are 15 row and 15 column signals, which act as control signals for current source blocks in the next stage.

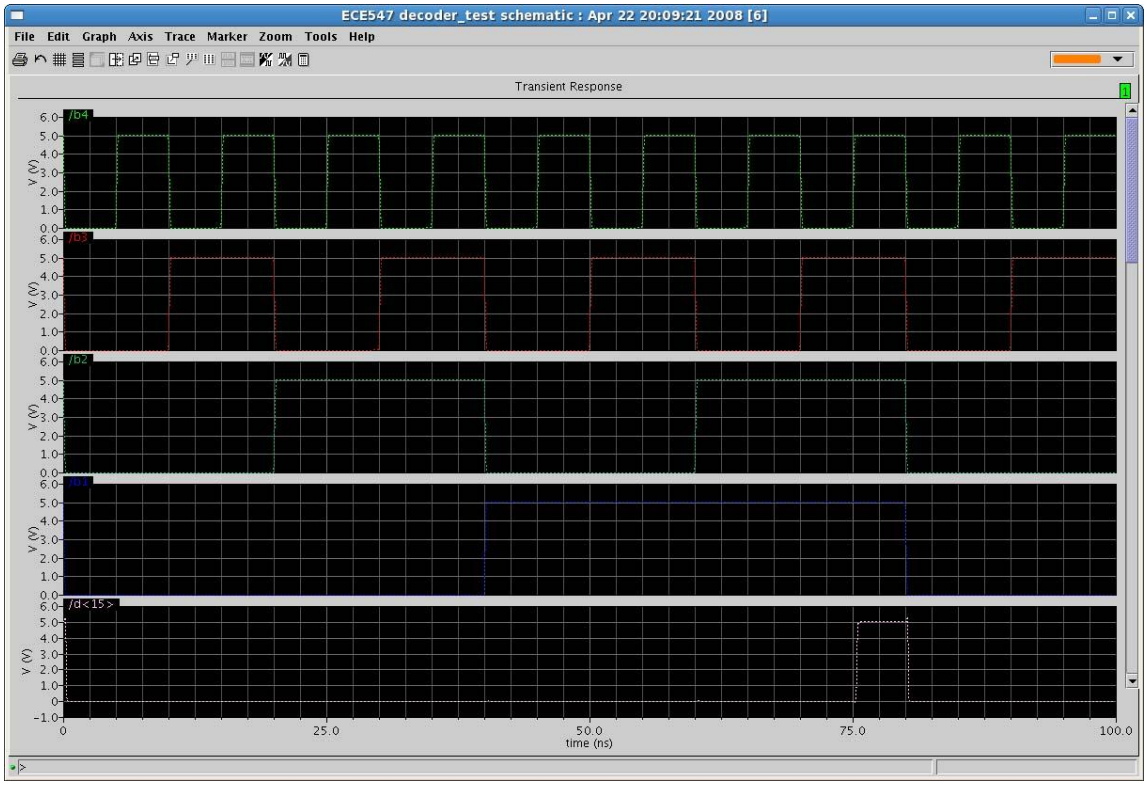

Fig.3. 2 Simulation Result of Input and output b15 in one period

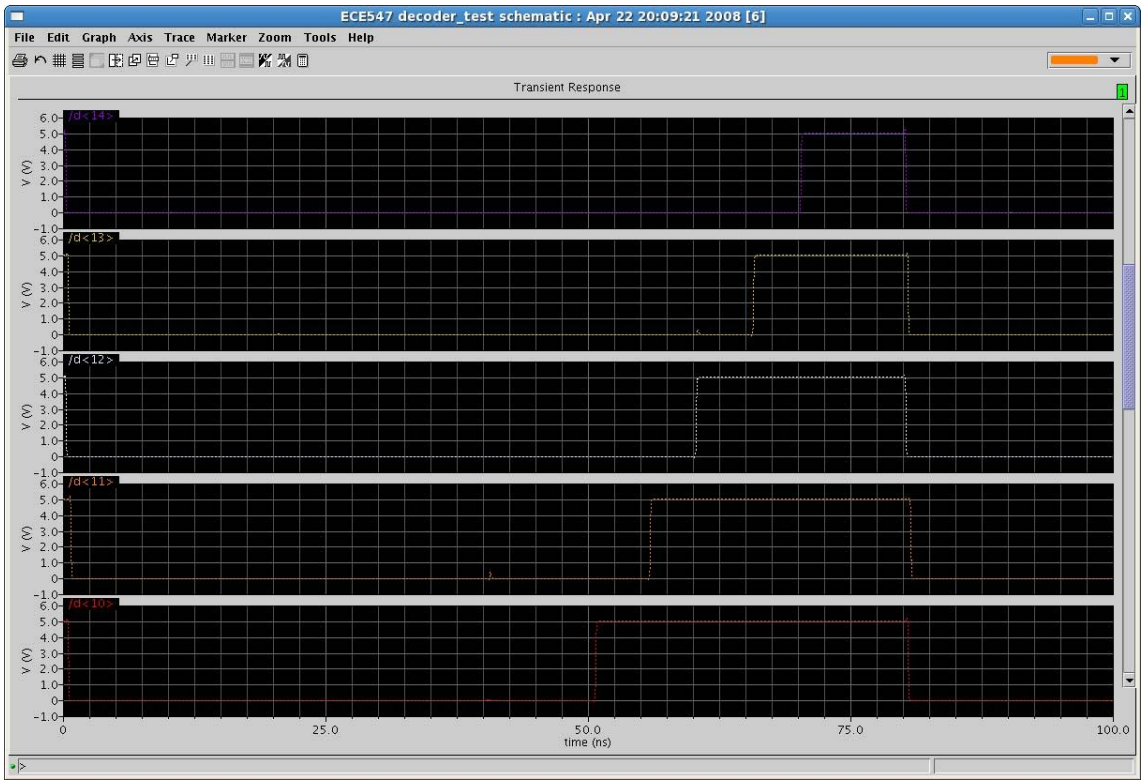

Fig.3. 3 Simulation Result of output b14-b10 in one period

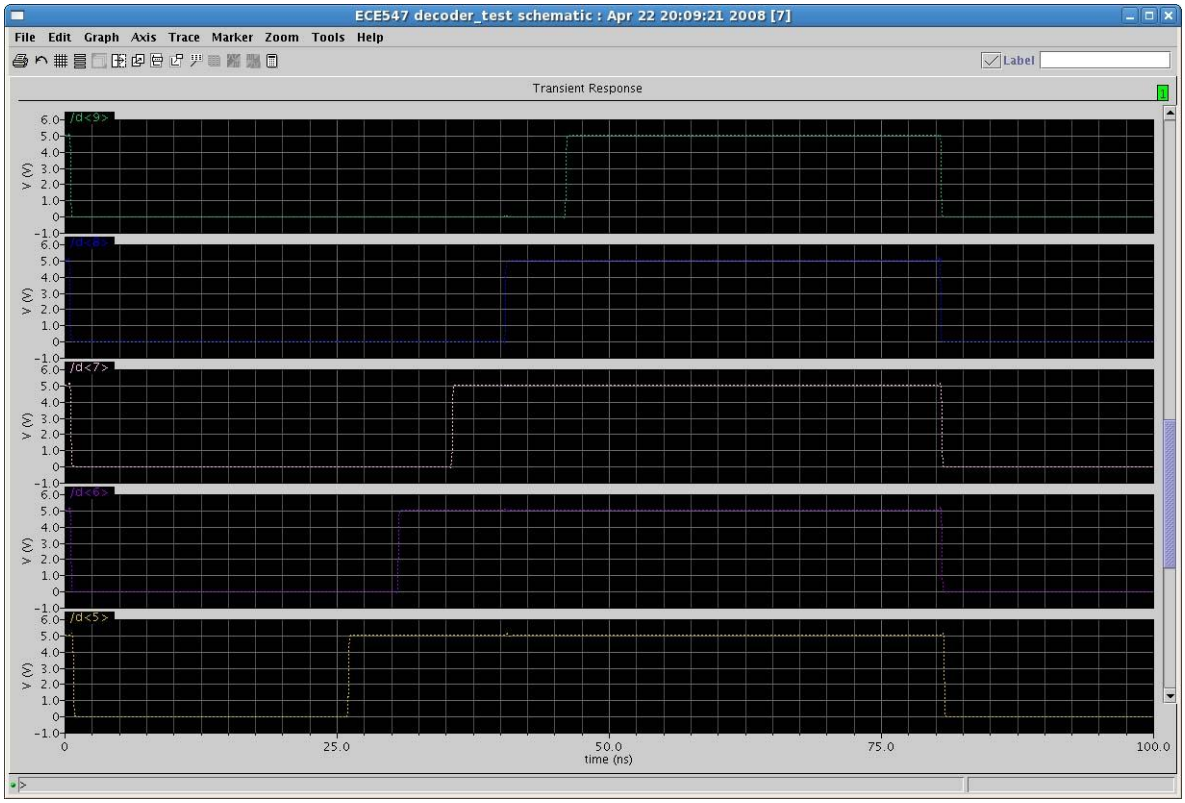

Fig.3. 4 Simulation Result of output b9-b5 in one period

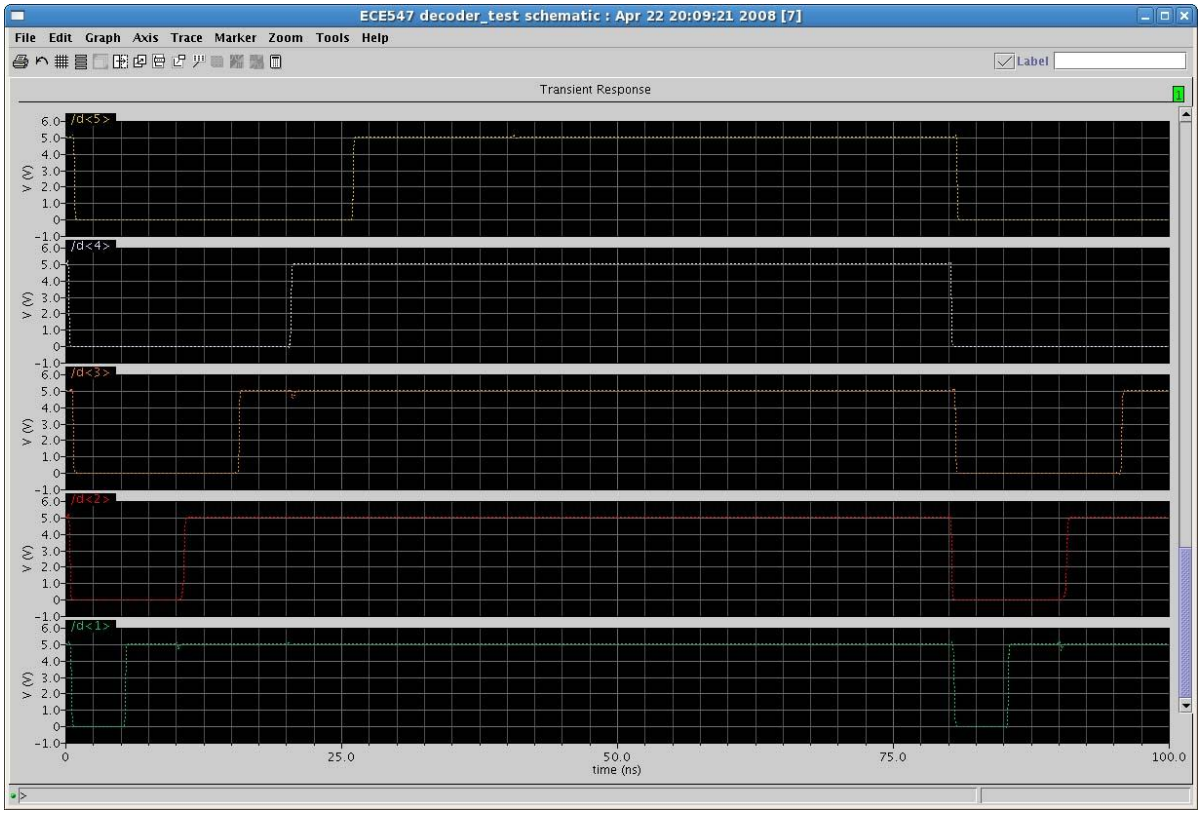

Fig.3. 5 Simulation Result of output b4-b1 in one period

IV Current cell array

4.1 cascade current source

Current cell array consists of 256 (16*16) current cells. This is the key part in this DAC since in this topology, precise current cells are critical. The current cell includes the analog part and the digital part. The analog part is a current source. And the digital part is to achieve correct logic to ensure the number of current sources that turn on should be equal to the value of the thermometer input code.

There are different topologies for current source. The logic below (Fig. 4.1) is the most popular cascade architecture in MOS technology. It can realize arbitrarily high output resistance by increasing the number of stacked cascade devices.

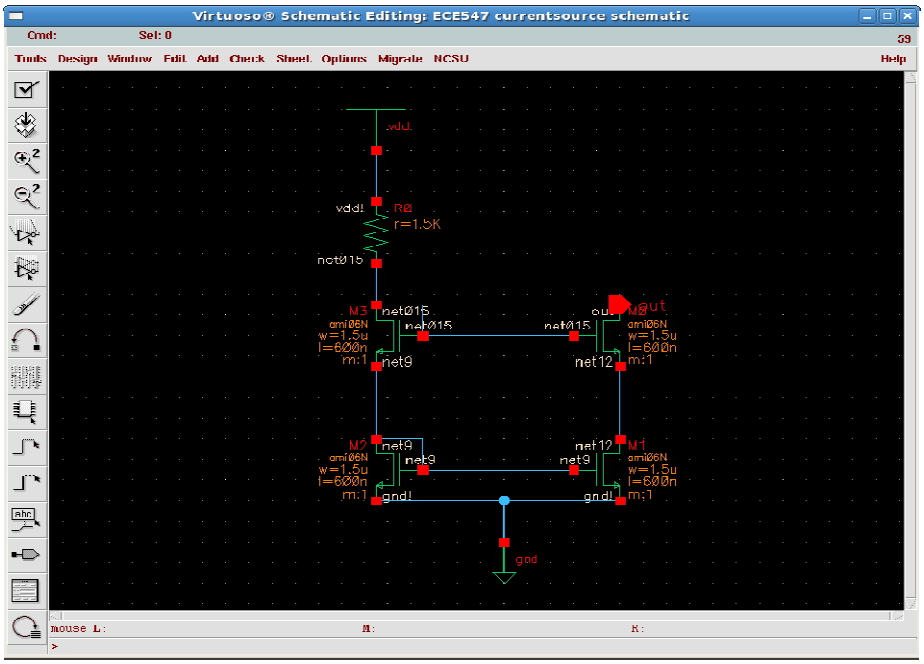

Fig.4. 1 Popular cascade current source

4.2 high swing current source

However, in this project, the current source used is shown in Fig 4.2. The transistor behaves as a shifter to improve the output swing voltage.

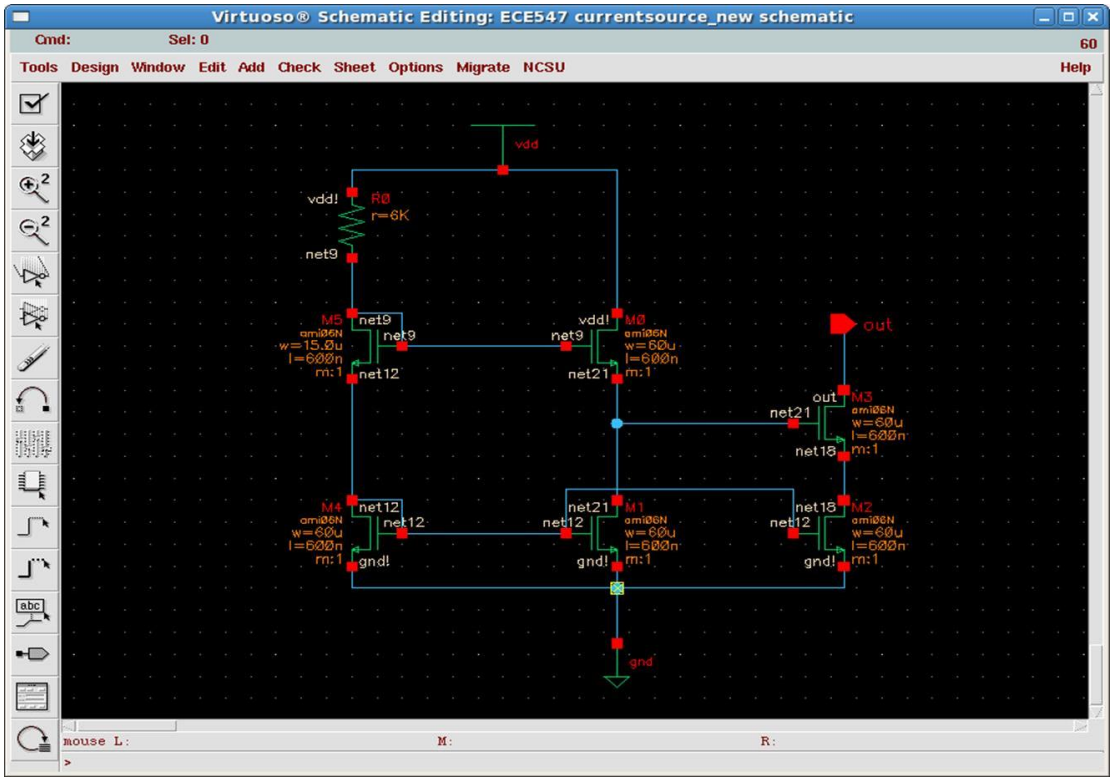

Fig.4. 2 High output swing current source

M0 behaves as the source follower and is biased by the output of the simple current mirror M4 and M1. Since Vgs of M0 is larger than its threshold voltage by the overdrive. However, Vds of M2 would be zero with equal thresholds and overdrives on all transistors. To bias M2 at the boundary between the active and triode regions, Vds1=Vov is required. Thus Vov of M5 is doubled by reducing its W/L by a factor of four to satisfy Vds1=Vov. Therefore, the Vout(min)=2Vov. Because the minimum output voltage does not contain a threshold component, the range of output voltages for which M2 and M3 both operate in active region is improved. Thus this type of level shifting is high-swing cascade current mirror. [6] Source follower is used to implement level shift and the current mirror behaves as an active load. [7]

For a digital input of 00000000, there will be zero current in Iout and 255*I_{REF} flowing in node Iout_neg . For an input of 11111111 the situation is reversed, and turning on the correct number of current sources can represent all digital values between these two extremes. The simulation result in Fig 4.3 shows that its output current is around 400uA.

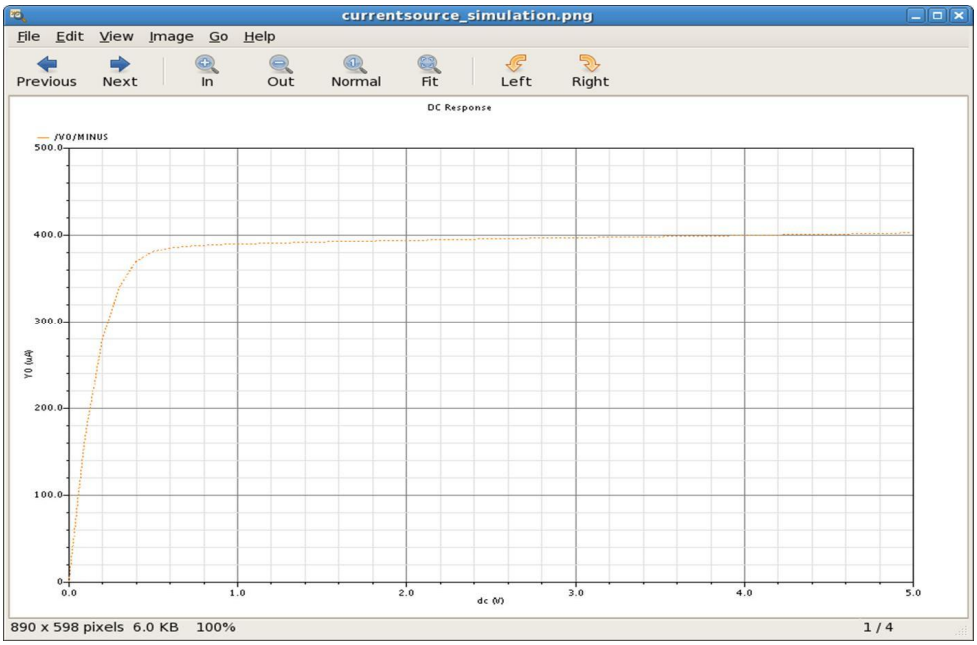

Fig.4. 3 Simulation Result of current source

4.3 current cell

When designing a current cell, the number of current sources that turn on should be equal to the value of the thermometer input code. If the previous row is high and either the current column or the current row is high, current source should source current through the positive output terminal OUT=ROW_{N-1} AND (ROW_N OR COL_N). [3] Combining this digital part and current source (analog part), the overall schematic of the current cell is shown in Fig 4.4.

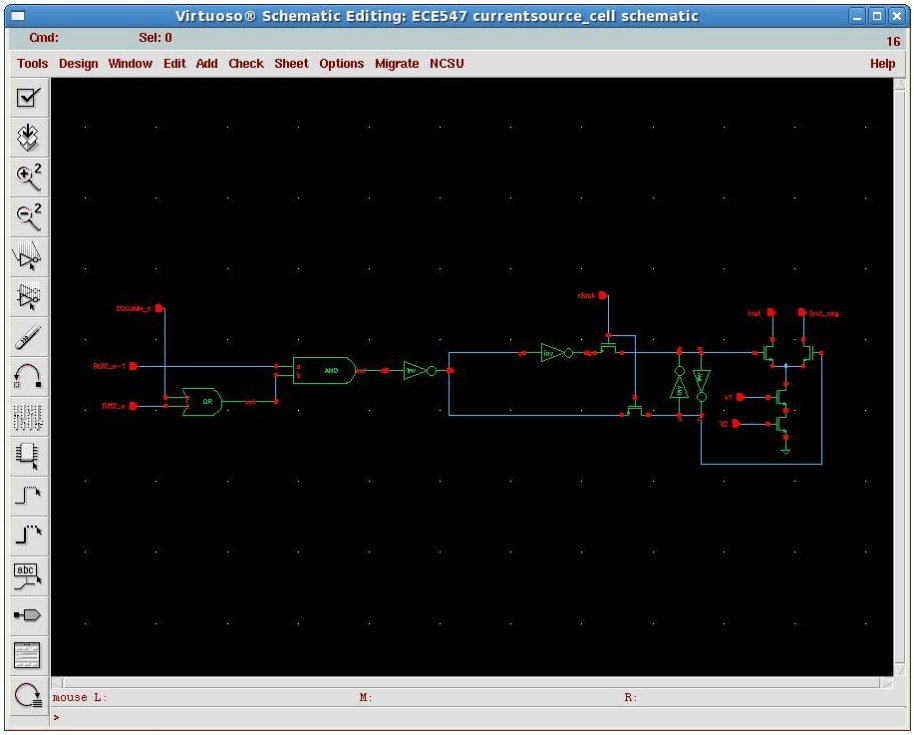

Fig.4. 4 Schematic of the current cell

The current source can be separated into bias and source. Although other parts in a current cell must repeat 256 times for a 16*16 array, the bias is only needed once and can be separated from other parts to minimize chip area and power dissipation.

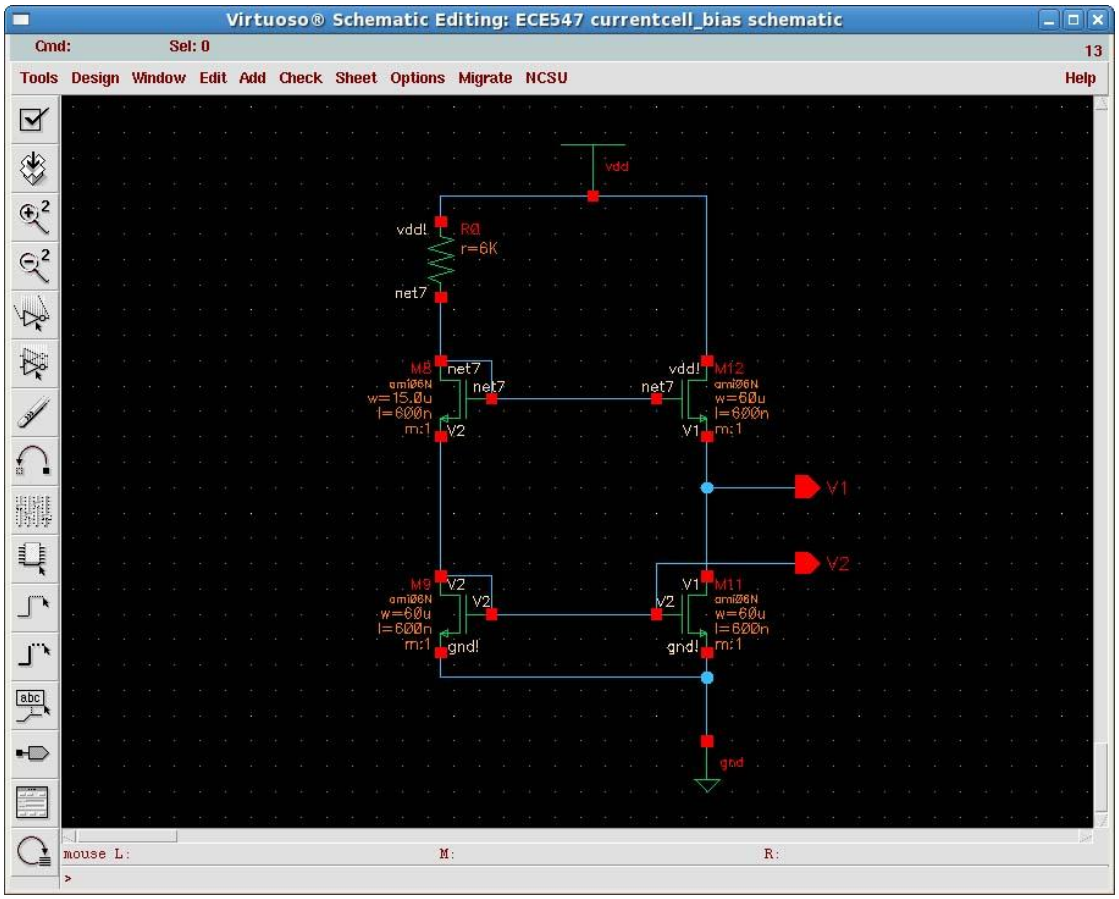

Fig.4. 5 Schematic of the current cell bias

4.4 Current cell array

Fig 4.6 shows the overall schematic of the current cell array. The small rectangular on the top is the symbol of the bias and 16*16 array is consisted of identical current cells. All Iout, Iout_neg and clock signals are connected together. Vdd, ground and 15 different thermometer codes need 16 current cells in each row or column. ROW_N are connected to ROW_{N-1} above it and become row input signal; all COL_N signals in some column are connected together to serve as column input signal. Thus, there are 15 row inputs and 15 column inputs.

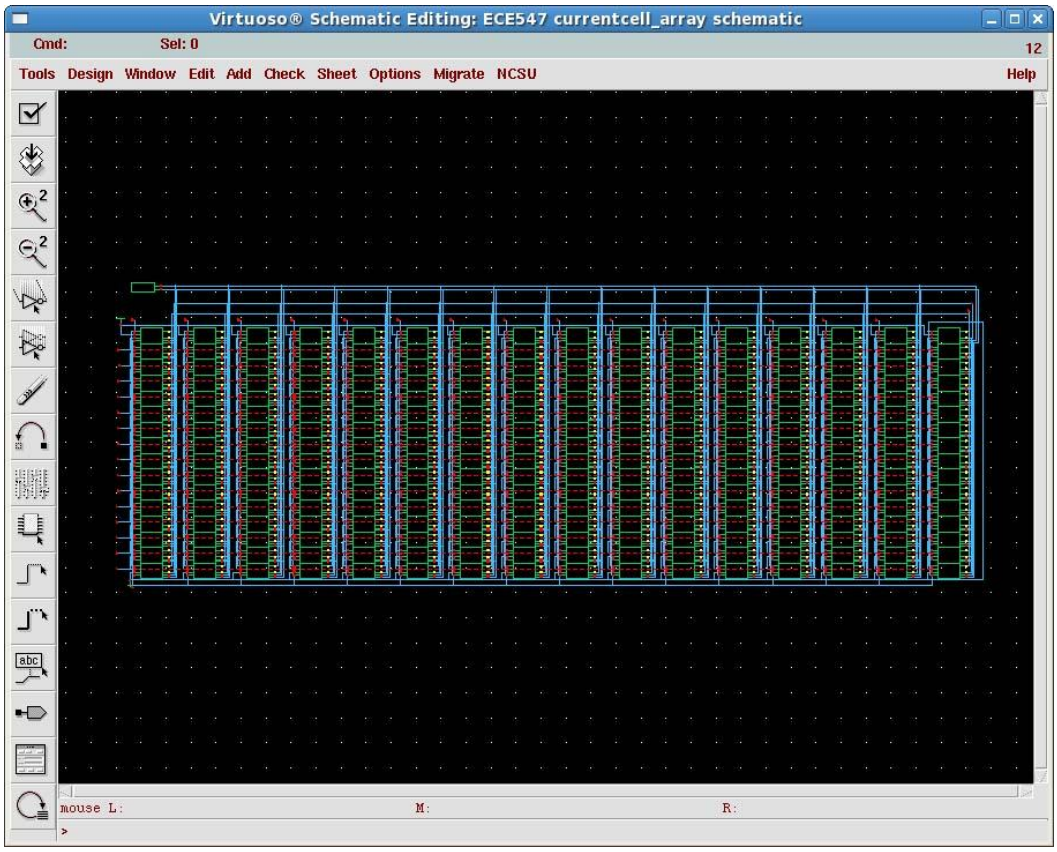

Fig.4. 6 Schematic of the 16*16 current cell array

V Op-amp

5.1 design of the op-amp

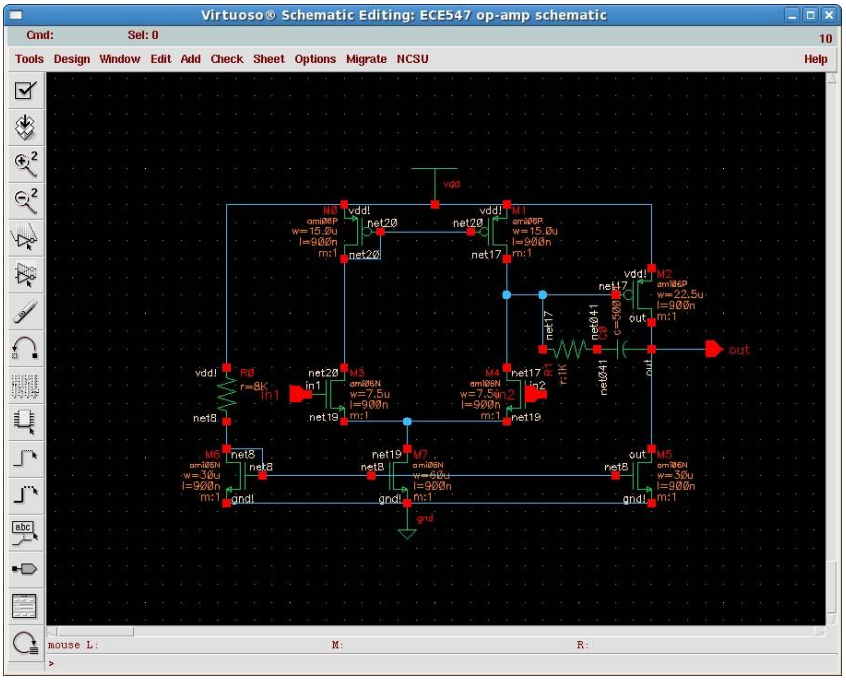

Fig.5. 1 Op-amp Schematic

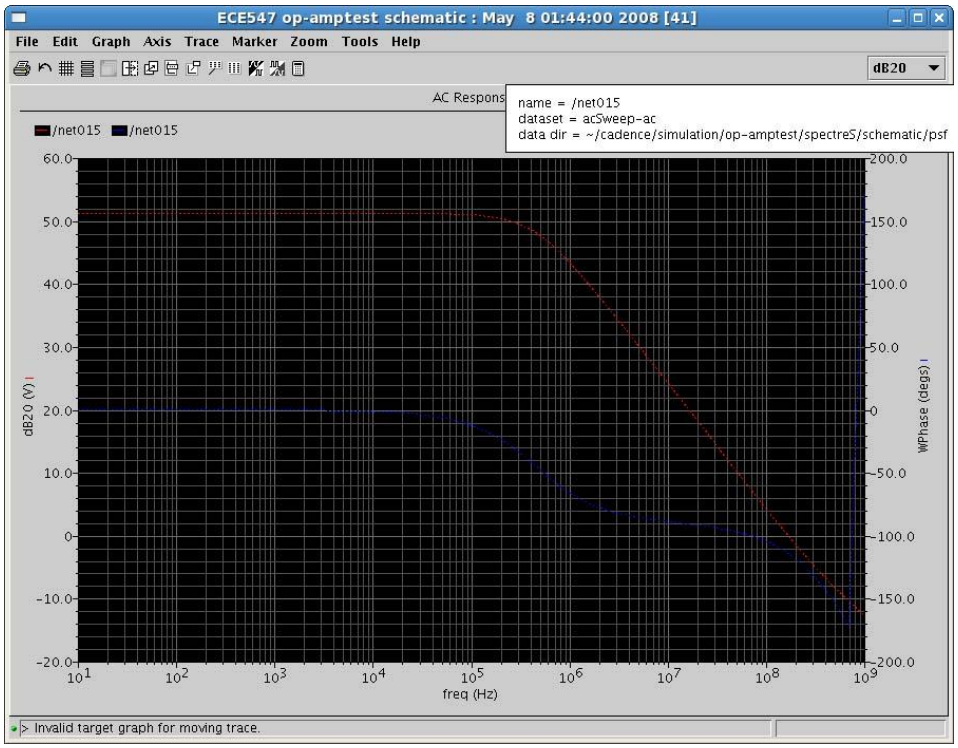

Fig.5. 2 Simulation Result of the op-amp

Fig 5.1 is schematic of op-amp. In1 is inverting input and in2 is non-inverting input. It uses an NMOS diff-amp and a PMOS common-source amplifier. The compensating network consists of a compensation capacitance and a zero-nulling resistor. They are used to make the op-amp stable. It is desirable that the open loop gain of the op-amp is much less than unity when the phase shift is 180^{o}. [8]

The simulation result displays this op-amp is stable, though its bandwidth is only around 10MHz. That's the reason why the whole DAC cannot work well in the estimated clock frequency (50MHz).

5.2 Differential Op-amp

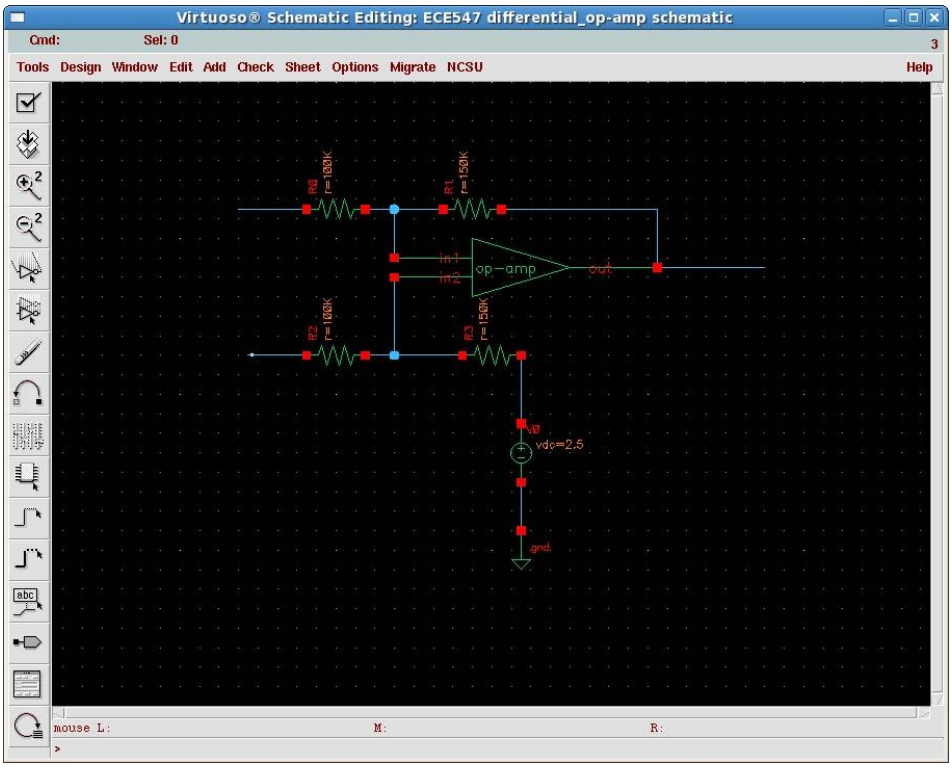

Fig.5. 3 Differential Op-amp

The outputs of current cell array are Iout and Iout_neg, their sum is always a constant. Small resistors (off chip) are used to transform current difference to voltage difference as inputs of the differential op-amp. Then the voltage difference is amplified, whose gain is the ratio of two resistances. Since here the gain here is not a critical parameter, we set it to 1.5 (Resistors are 150KOhm and 100KOhm separately).

5.3 Buffer

Since the output of the op-amp is to be off chip, it's better to add a buffer after the last op-amp to isolate it from a large load capacitance. The buffer is used to avoid oscillation and keep stable. Source follower is a choice for the buffer. However, it limits the output swing of the op-amp. Class AB buffer is another option. The simulation result shows that it can drive 20pF large capacitance and the output of DAC still performs well. 20pF capacitance is an estimate of off-chip capacitance including pad capacitance and capacitance produced in the manufacturing process.

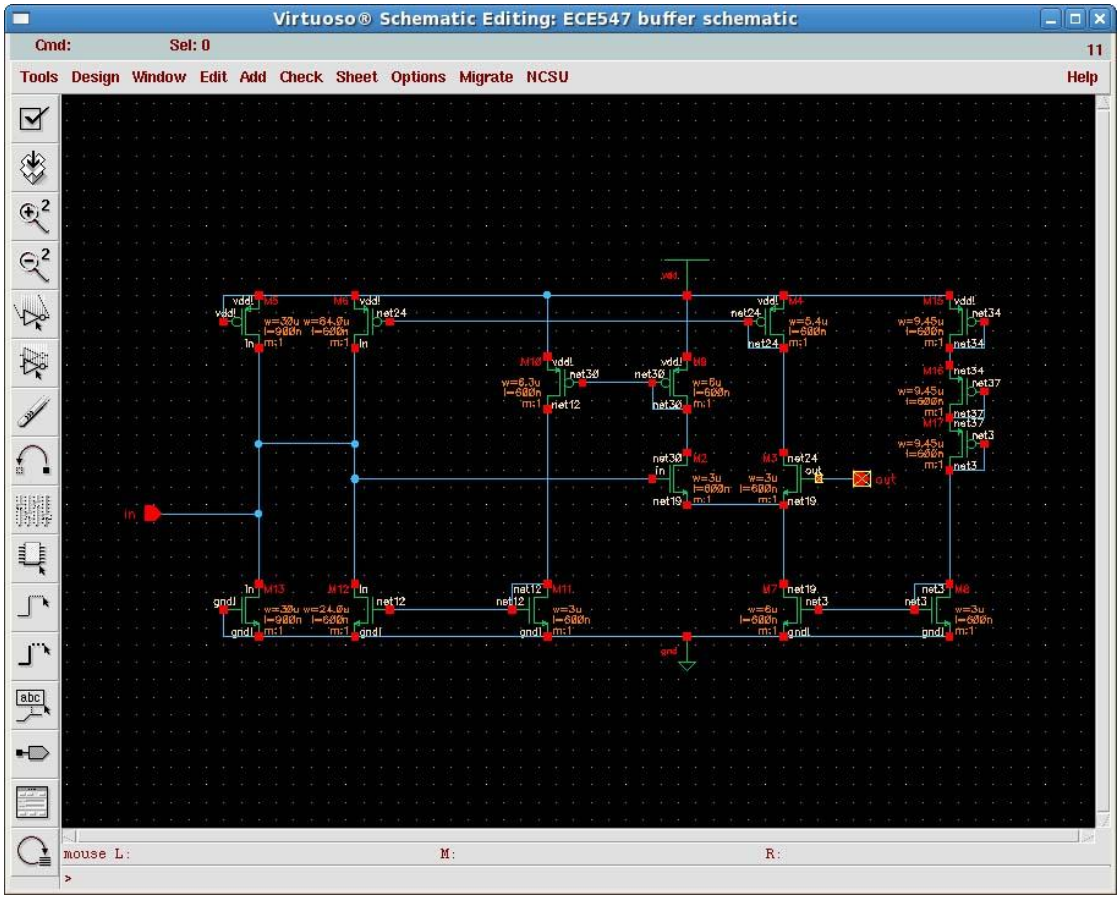

Fig.5. 4 Buffer Schematic

VI The overall design

6.1 Schematic

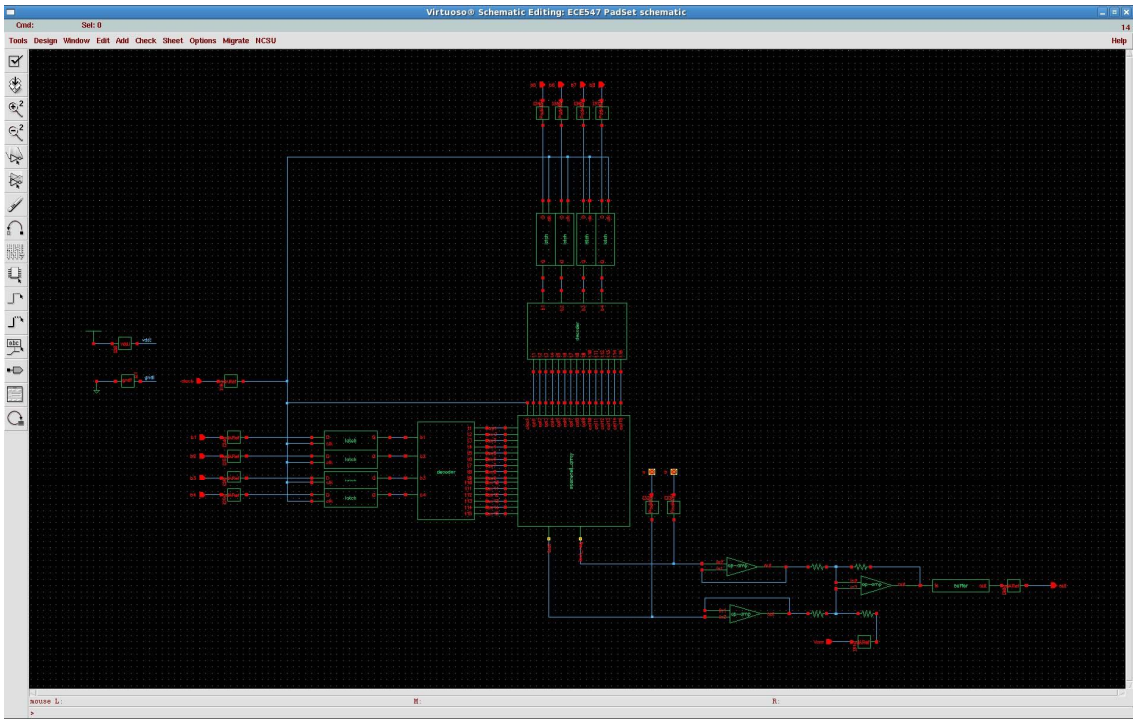

Fig.6. 1 Overall DAC Schematic

Fig 6.1 is the overall schematic of the DAC. It has 15 pins, including Vdd! And gnd!, 8 digital input, 1 analog output, clock, 2.5V common mode input voltage, and bias “a” and “b”. The gain of two op-amps between the current cell array and the output op-amp is approximately unity when their open loop gain is much greater than 1. Pin “a” and “b” are connected to small resistors (off chip) which are connected to an adjustable voltage which is flexible in controlling the output.

6.2 Simulation

The simulation result is shown in Fig 6.2. It behaves well except that there is a huge glitch in the middle of the output. It may come from superposition of glitches from different sources, such as decoders, current cells and op-amp since simulation results are fine for each separate part.

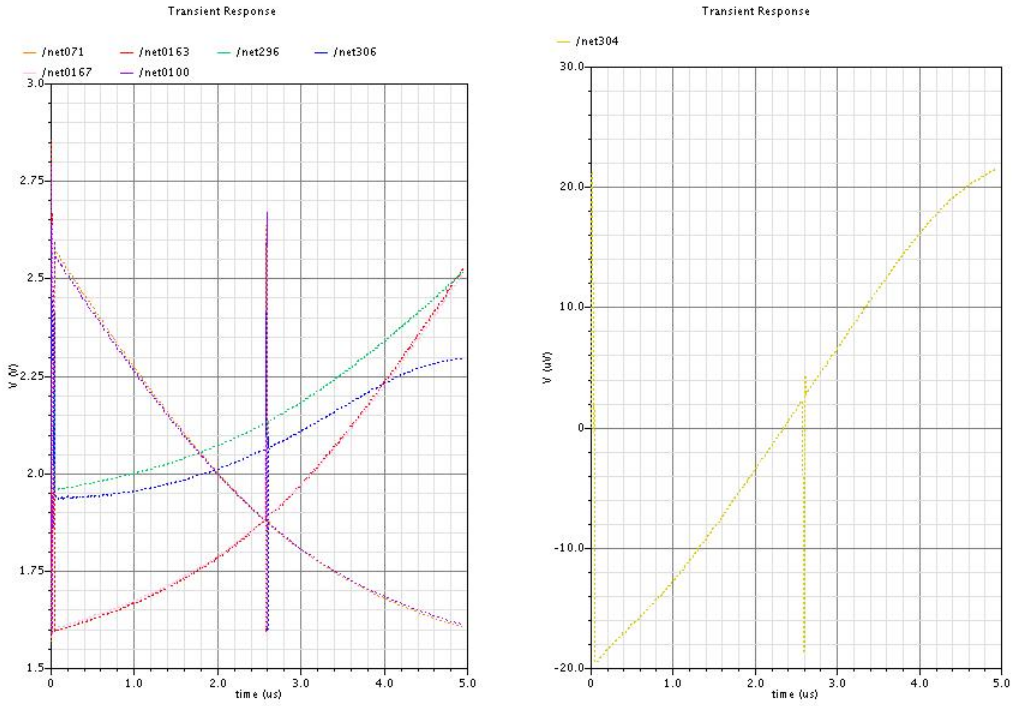

Fig.6. 2 DAC simulation result

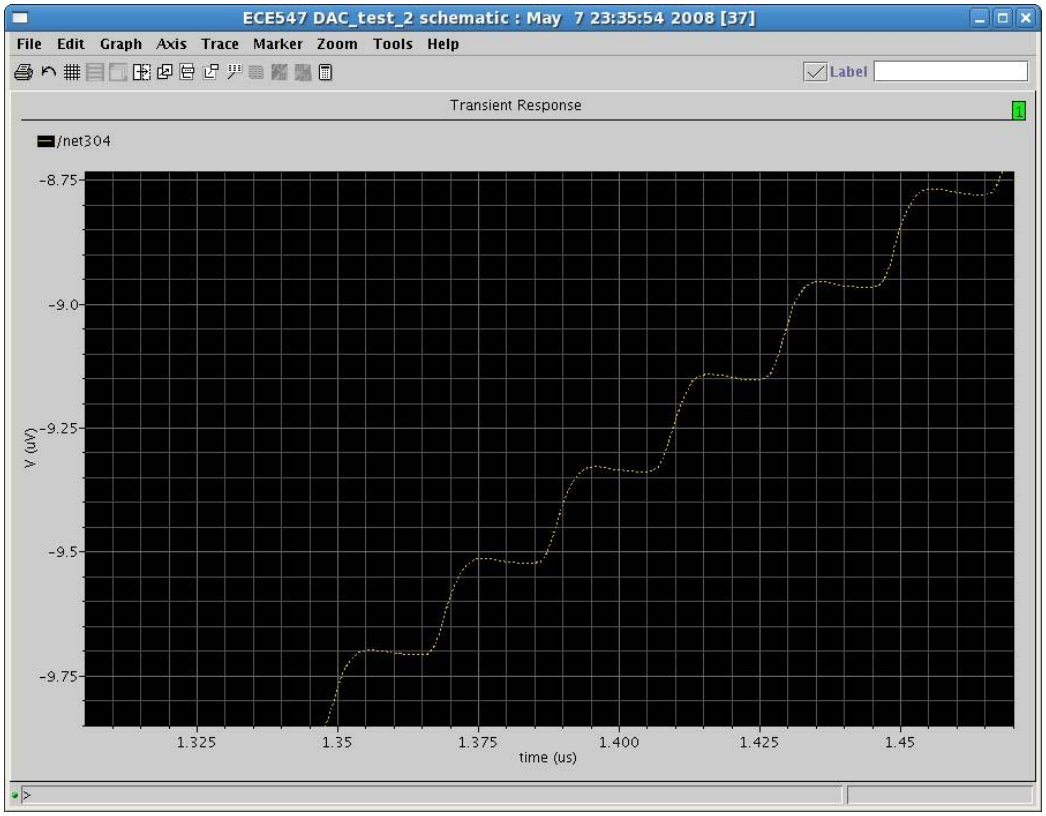

Fig.6. 3 Enlarged output at 50MHz

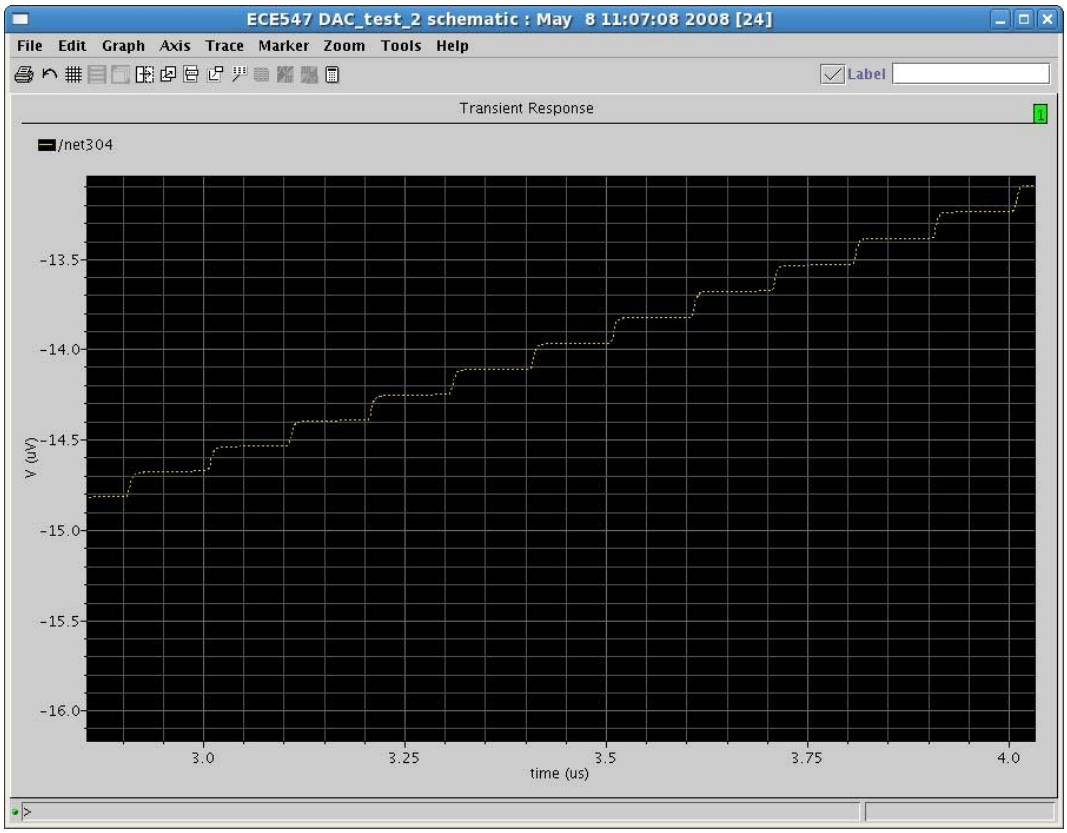

Fig.6. 4 Enlarged output at 10MHz

Enlarged output results of 50MHz and 10MHz (clock frequency) are shown in Fig 6.3 and Fig 6.4 separately. In comparison, DAC at 10MHz performs better than that at 50MHz in that the output voltage in every step keeps a constant at 10MHz, while it has small glitch at 50MHz. This stems from the problem of short settling time and needs to be improved later.

VII Pad

7.1 Choice of pins

All pins have parasitic resistance, capacitance and inductance but they are not totally identical for all pins. Pins which have the least parasitic parameters should be used for the most sensitive pins, in this design, such as a, b, out. Vdd and gnd should keep constant and thus be connected with the pins with largest parasitic parameters. From Table 7.1, it is obvious that pin 10, 11,30,31 should be used in most sensitive pins, if ran out, pin 9,12,29,32 are secondary choice. While pin 1,20, 21 and 40 are suitable for Vdd and gnd. Notice here b1 is MSB and b8 is LSB.

This layout has 15 pins including Vdd! connected to "padvdd" and gnd! connected to "padgnd". Other 13 pins are connected to "padaref", 25 pins which hasn't been used are "padnc" or "padfc"(in the corner). Pin 21 is used for Vdd!, pin 40 is used for gnd!, pin 30 for clock, pin 31 for out, pin 11 for a, pin 10 for b, and pin 8, 9, 12, 13, 28, 29, 32, 33 for eight digital inputs.

Table 3 Electrical Characteristics

Pin	R (Ohm)	L (nH)	C (pF)	t_{of} (ps)
1, 20, 21, 40	0.217	8.18	5.32	209
2, 19, 22, 39	0.177	7.92	4.39	187
3, 18, 23, 38	0.154	7.34	3.37	157
4, 17, 24, 37	0.110	6.48	2.34	123
5, 16, 25, 36	0.103	5.69	2.16	111
6, 15, 26, 35	0.0661	4.37	1.43	79.0
7, 14, 27, 34	0.0646	4.54	1.48	81.9
8, 13, 28, 33	0.0498	3.69	1.05	62.3
9, 12, 29, 32	0.0378	3.54	0.863	55.3
10, 11, 30, 31	0.0247	3.15	0.660	45.6

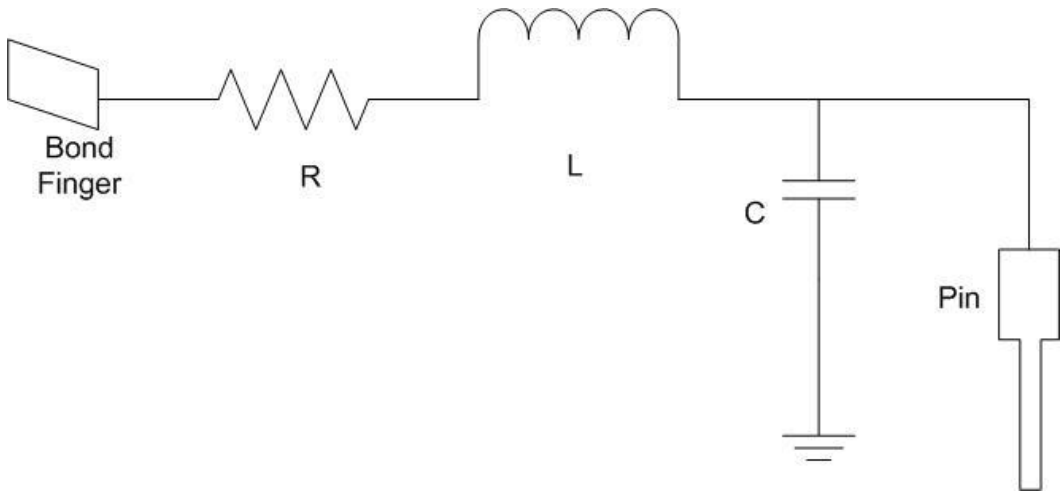

Fig.7. 1 Package Trace

7.2 Simulation with pad

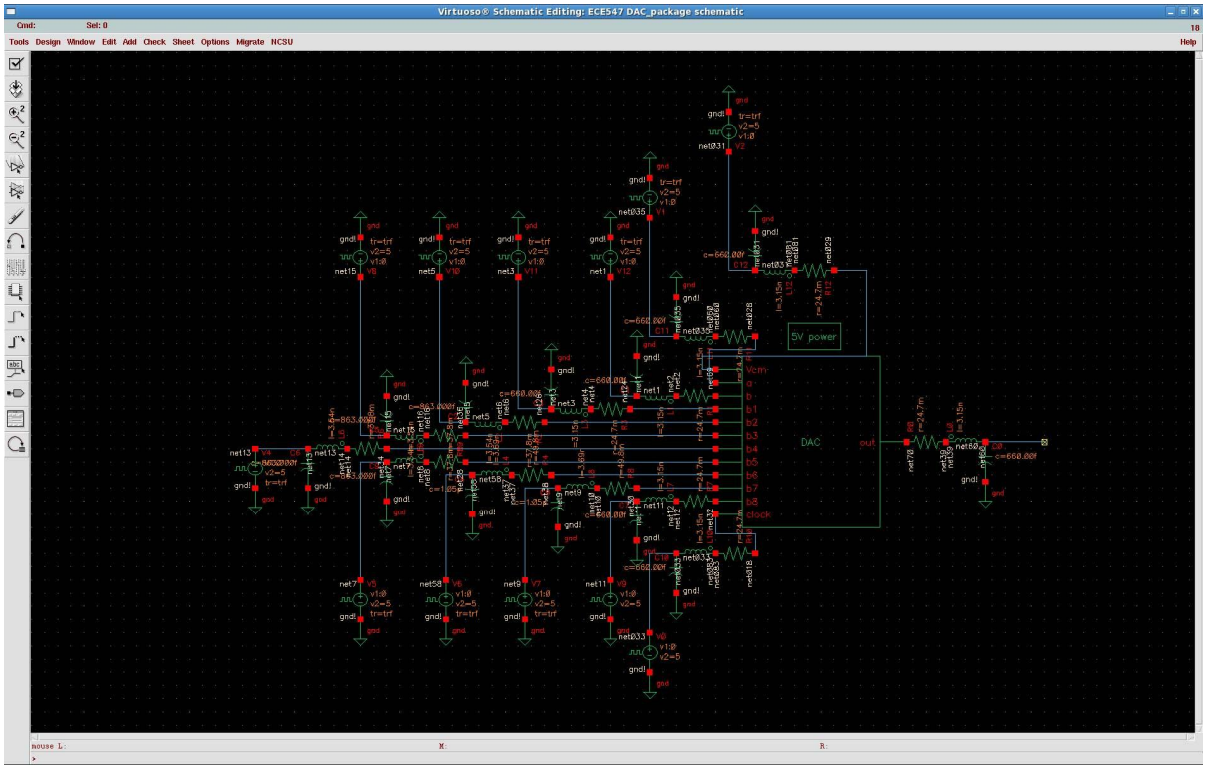

Fig.7. 2 DAC Schematic with pad

Simulation result with schematic is shown in Fig 7.3. It encounters the same problem as that of simulation without pad.

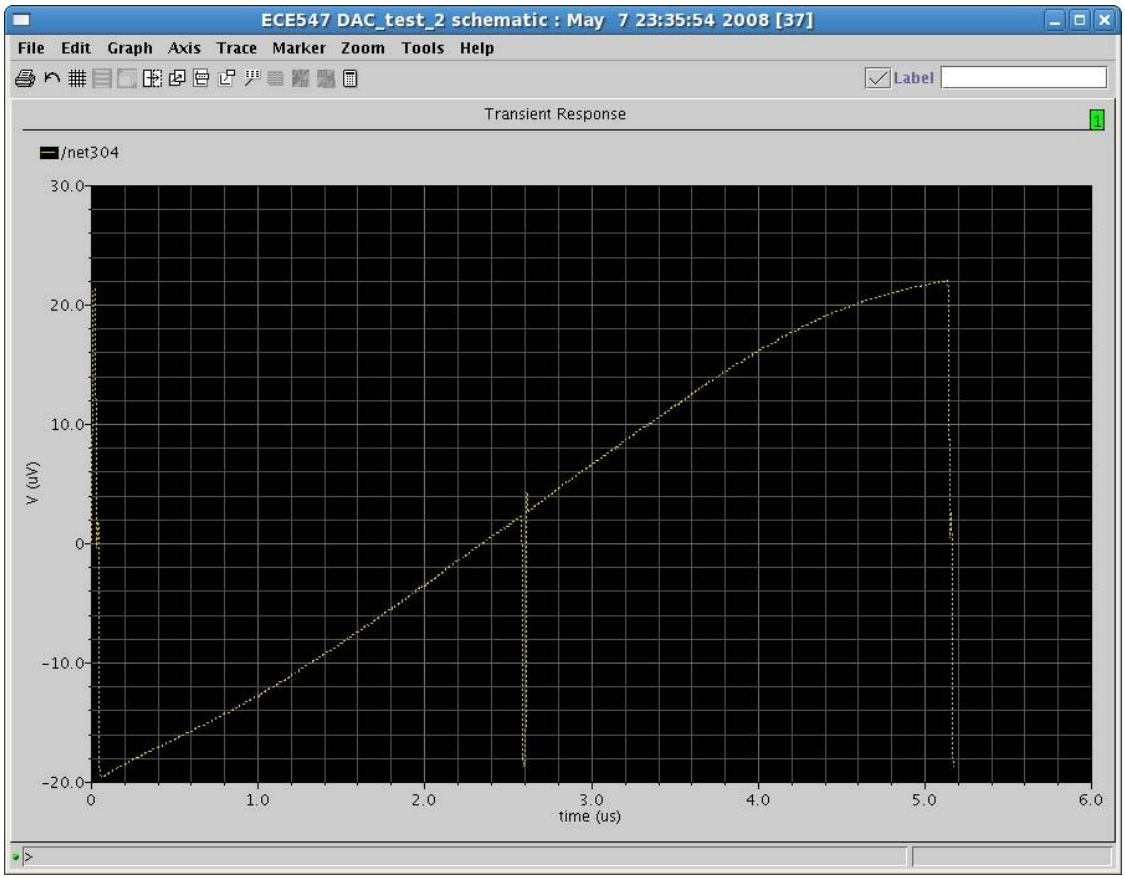

Fig.7. 3 Simulation result of DAC with pad

VIII Layout

8.1 Simulation result with layout

Drawing the layout is quite straightforward but time-consuming. It was used full custom method to minimize area of the layout. It's important to make parasitic parameters in the layout small and parameters in the layout close to that in the schematic. Separate layout for each part in shown in appendix A2.

Parasitic capacitance and resistance are always inevitable. Usually they make the performance worse compared to ideal models, but the op-amp here is an exception.

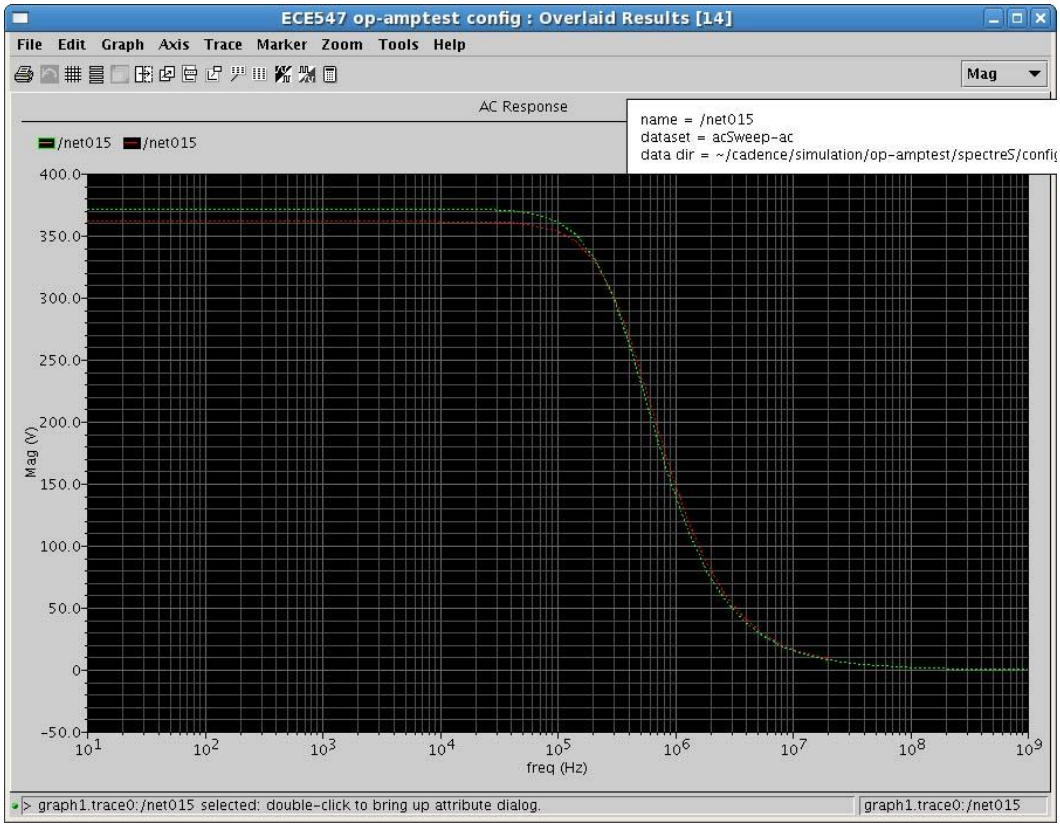

Fig.8. 1 Comparison between simulation with layout and with schematic

Fig 8.1 displays the comparison between the simulations of op-amp with schematic and layout. The green line is the result with layout. In the figure, the simulation result with layout is better than that with schematic. It may stem from the fact that parasitic capacitance between lines in the layout also serves as the compensation capacitance which is in parallel with the original one, makes the overall capacitance smaller, and therefore improves the gain.

8.2 Layout and taping out

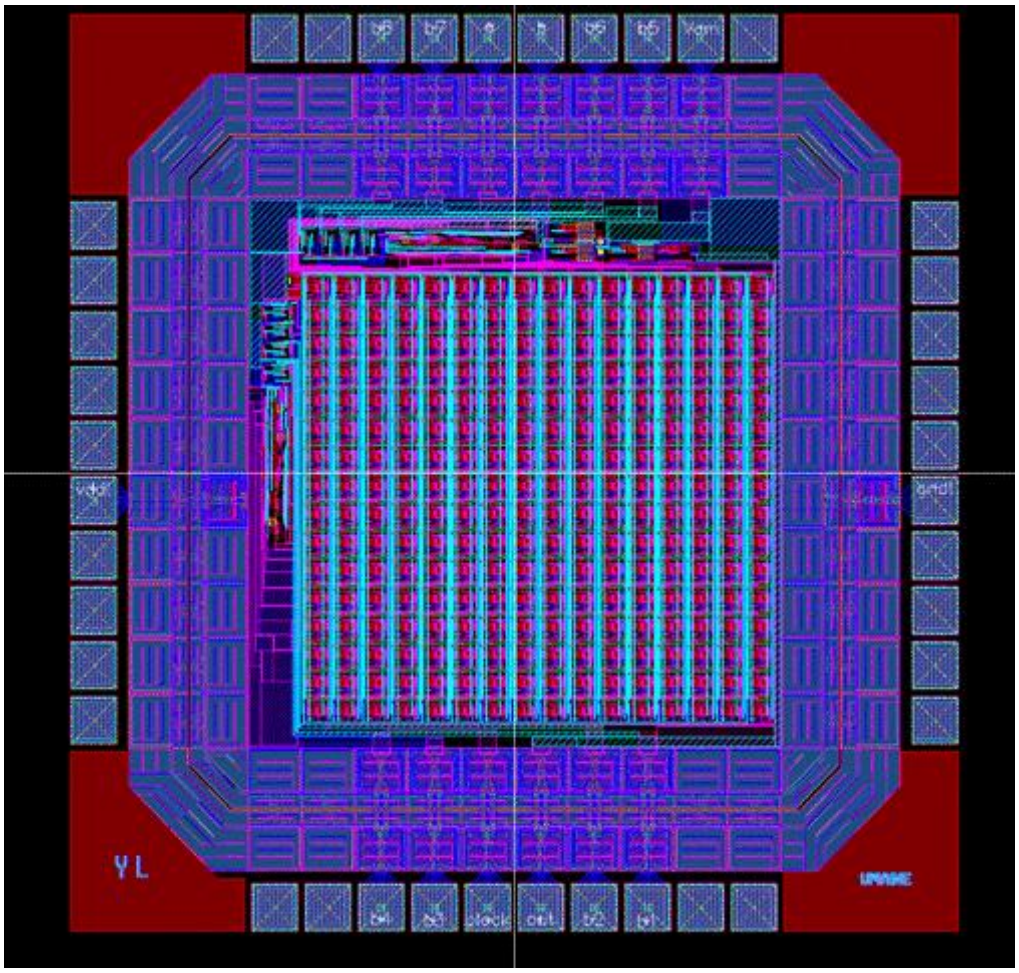

Fig.8. 2 Layout of the overall design

After streaming out, it is shown that overall layout has 16.3% ploy, 57.6% metal1, 53.0% metal 2 and this has achieved the minimum limit of percentage of area. Thus, it has been accepted and will be fabricated on the AMI_C5F run using C5N or C5F or C5T.

It is obvious that majority of this layout is occupied by the 16*16 current cell array.

IX Conclusion and Future Development

9.1 Tradeoff between power dissipation and speed

It is clear that the current cell array takes up the major part in the layout. Therefore, the majority portion of power consumption stems from it. It is estimated that the total power is approximately $V_{DD}*I_{REF}*2^N$. N equals to 8 here. When V_{DD} is a constant, lower I_{REF} is desirable to reduce power consumption. But if I_{REF} decreases, the speed of the DAC will reduce simultaneously. Thus, trade-off between power and speed is a must according to different applications.

9.2 Issues regarding this project

This design can work well at 10MHz but have difficulties at 50MHz mainly because of the performance of op-amp limits the overall performance of DAC. Future work is to increase the bandwidth of the op-amp to get better performance of DAC in higher frequency. In addition, it's critical to figure out the reasons of the huge glitch in the middle of the output and fix it. Finally, calculating DNL and INL of the DAC is necessary in determining overall performance of the DAC which has not been done yet.

9.3 Future development

In this design, full unit-element current-steering topology is used and therefore it needs a large amount of area. The 16*16 current cell array occupies an area of 798.3um*738.3um in this process. If higher resolution, the architecture is not suitable since it takes four times of the original area as the bit increases 2. For example, a 10-bit current-steering DAC needs a 32*32 current cell array which occupies 4 times the original area. In this case, it is necessary to combine different topologies to take advantage of their advantages and avoid their drawbacks. For example, it's desirable to combine unit-element and binary current-steering architectures. This can obtain higher speed compared to full binary architecture, at the same time occupy less area and power consumption compared to full unit-element topology. For instance, when designing a 10-bit current-steering DAC, using unit-element current-steering as 6-bit MSBs and binary current-steering as 4-bit LSBs is attractive since the chip is relatively small and fast.

Future research can also focus on scaling, that is to reduce supply voltage to lower power consumption. Also it can be emphasized on area scaling. Currently, the main design constraint on the size and power consumption is the amount of current to drive the following stage, and is simply a function of the load capacitance on the output. As devices become smaller, this load capacitance will shrink quickly, become negligible and not a concern for speed requirements. Instead, the noise and matching requirements and will be the limiting factor in how small the DAC can be and what kind of power it will require.

References

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[5] Digital Integrated Circuits, Jan M. Rabaey, pp 333-334

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[7] Analysis and design of analog integrated circuits (4^{th} edition), Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, pp269-270, 408-409

[8] CMOS circuit Design, Layout, and Simulation (2nd Edition), R.J. Baker, 2005, pp 773-795

Appendix A: Schematic of gates in the decoder

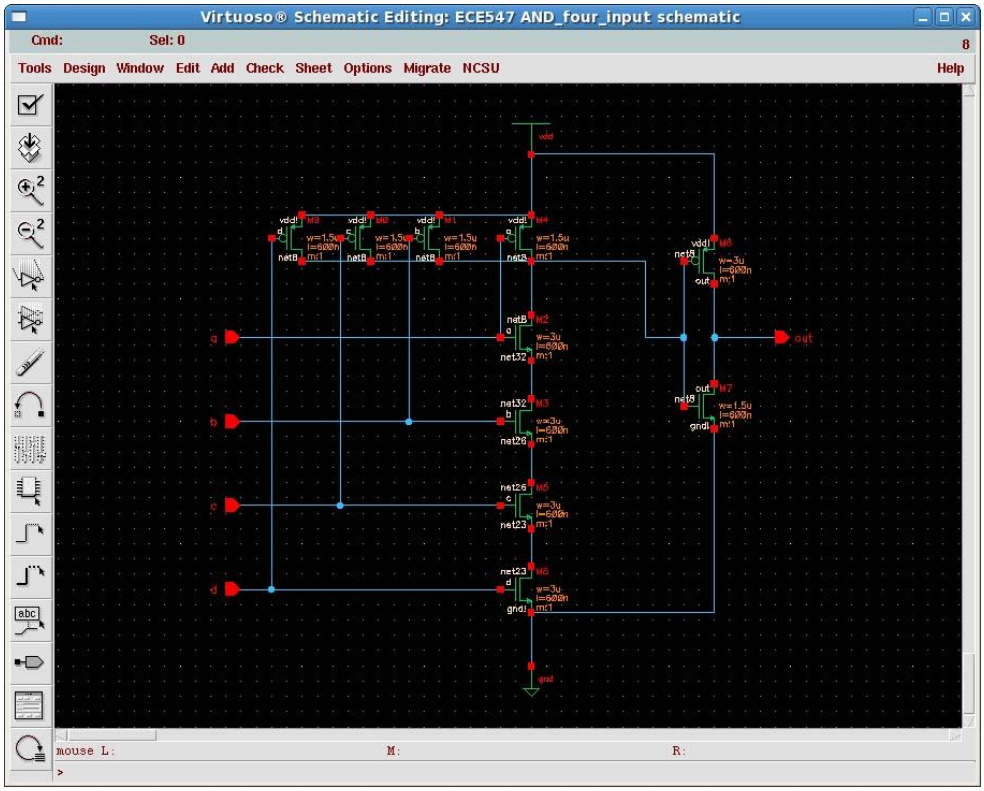

Fig A. 1 Four input AND gate

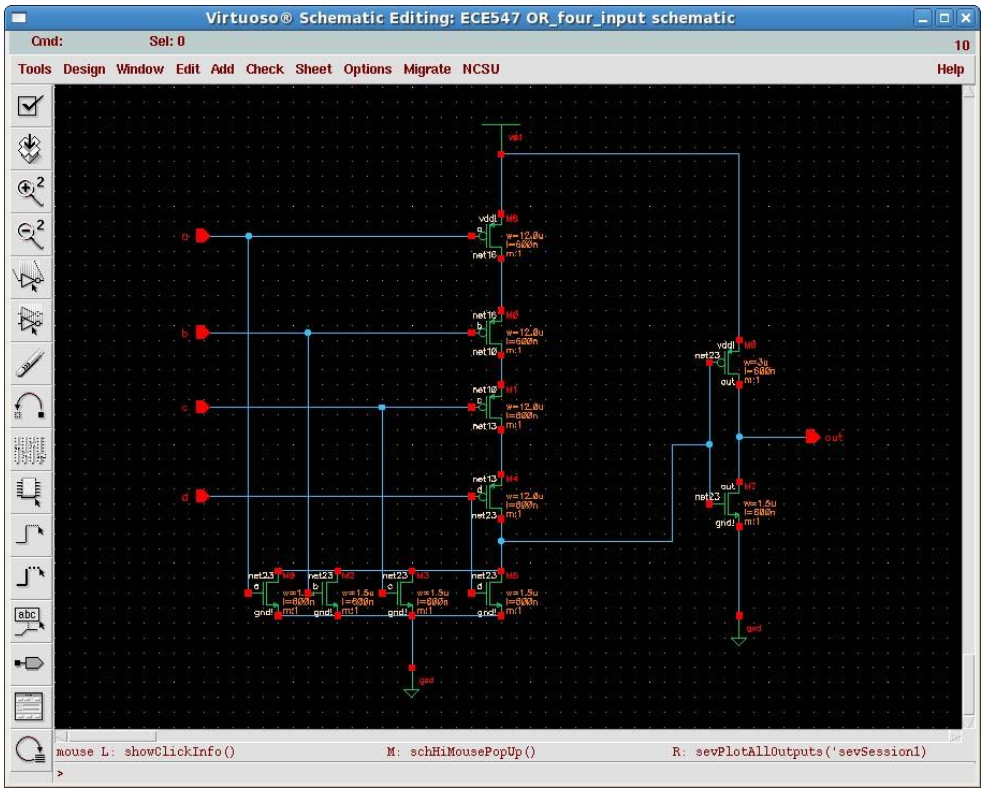

Fig A. 2 Four input OR gate

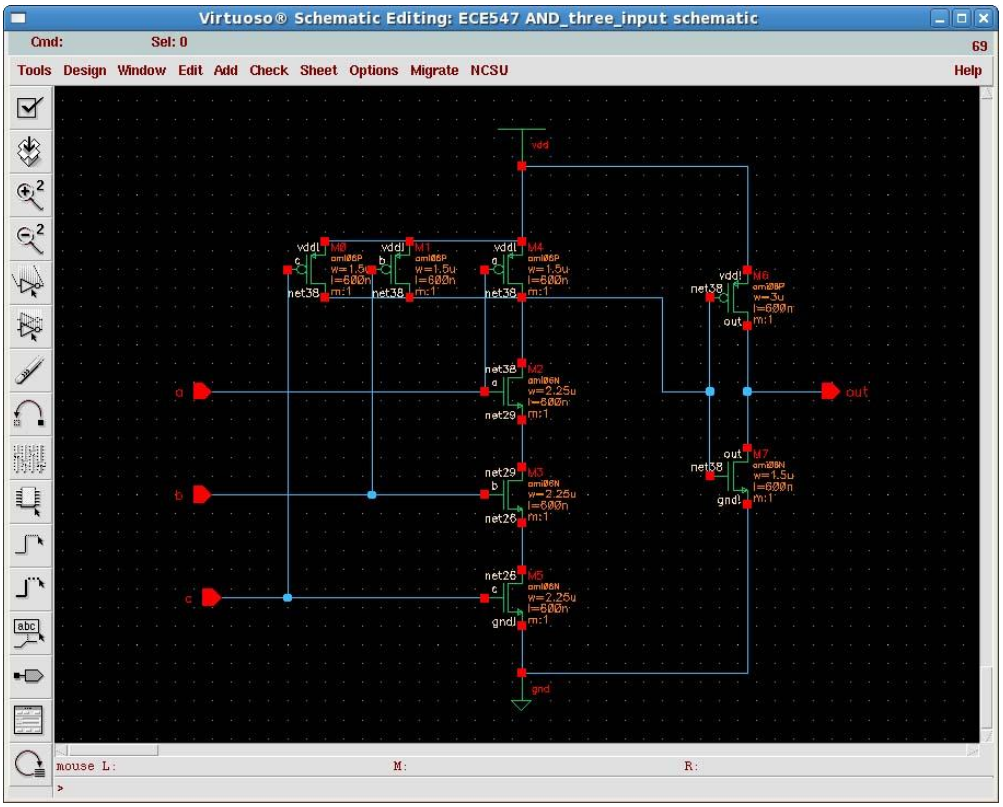

Fig A. 3 Three input AND gate

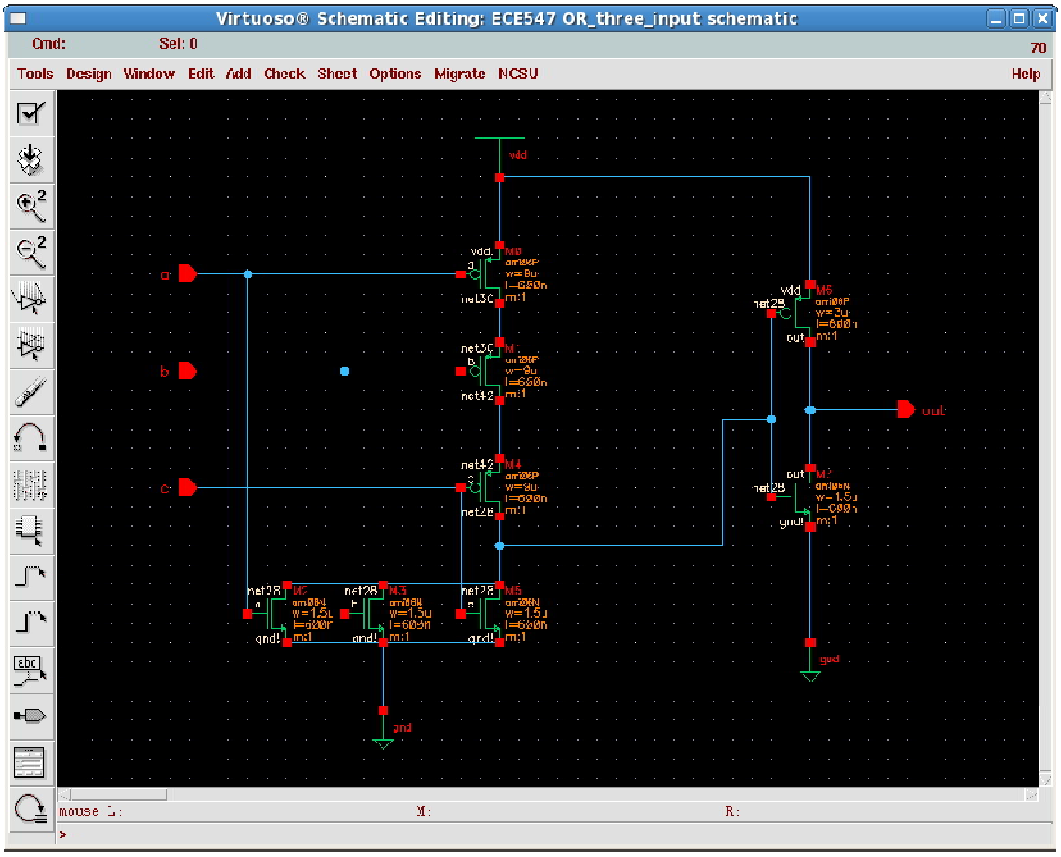

Fig A. 4 Three input OR gate

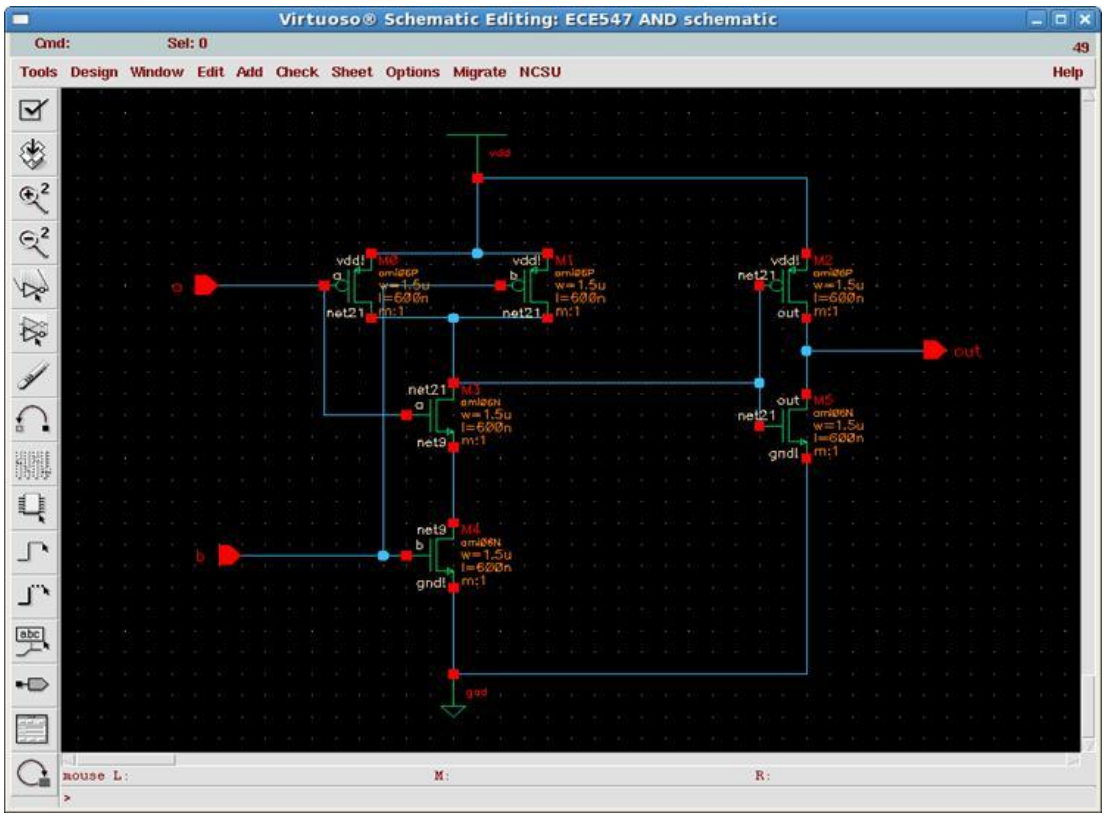

Fig A. 5 Two input AND gate

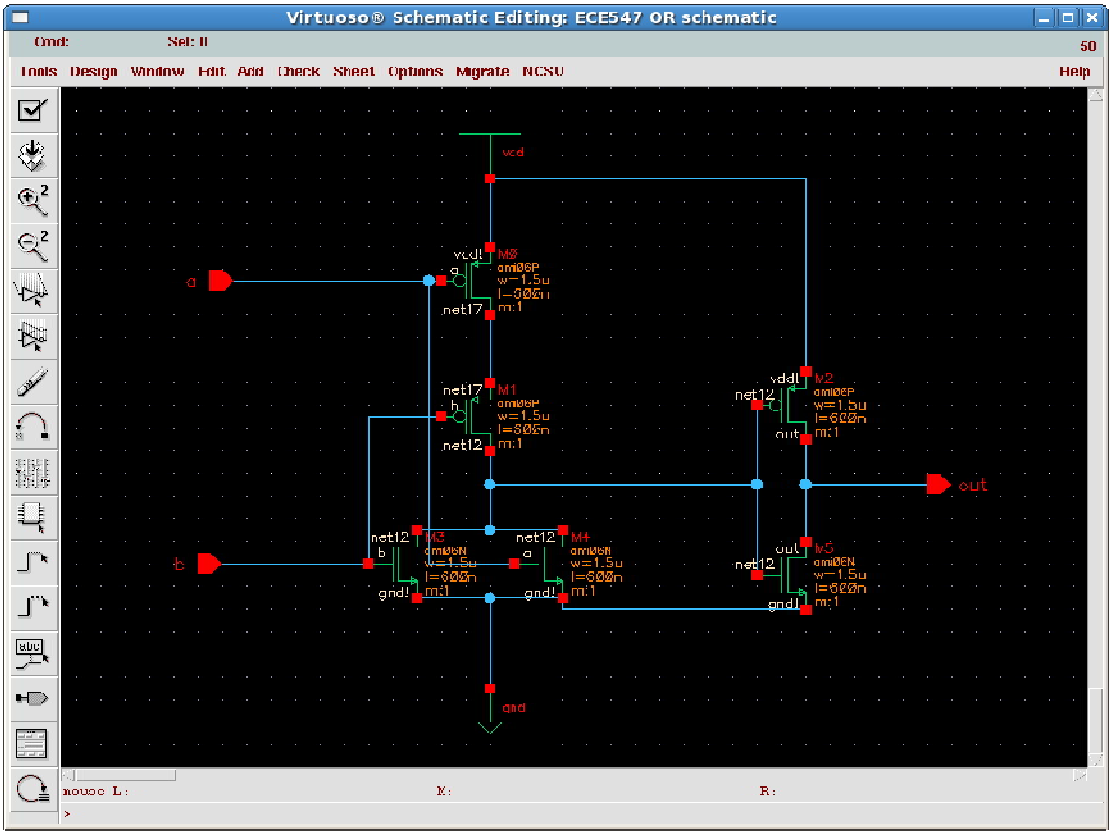

Fig A. 6 Two input OR gate

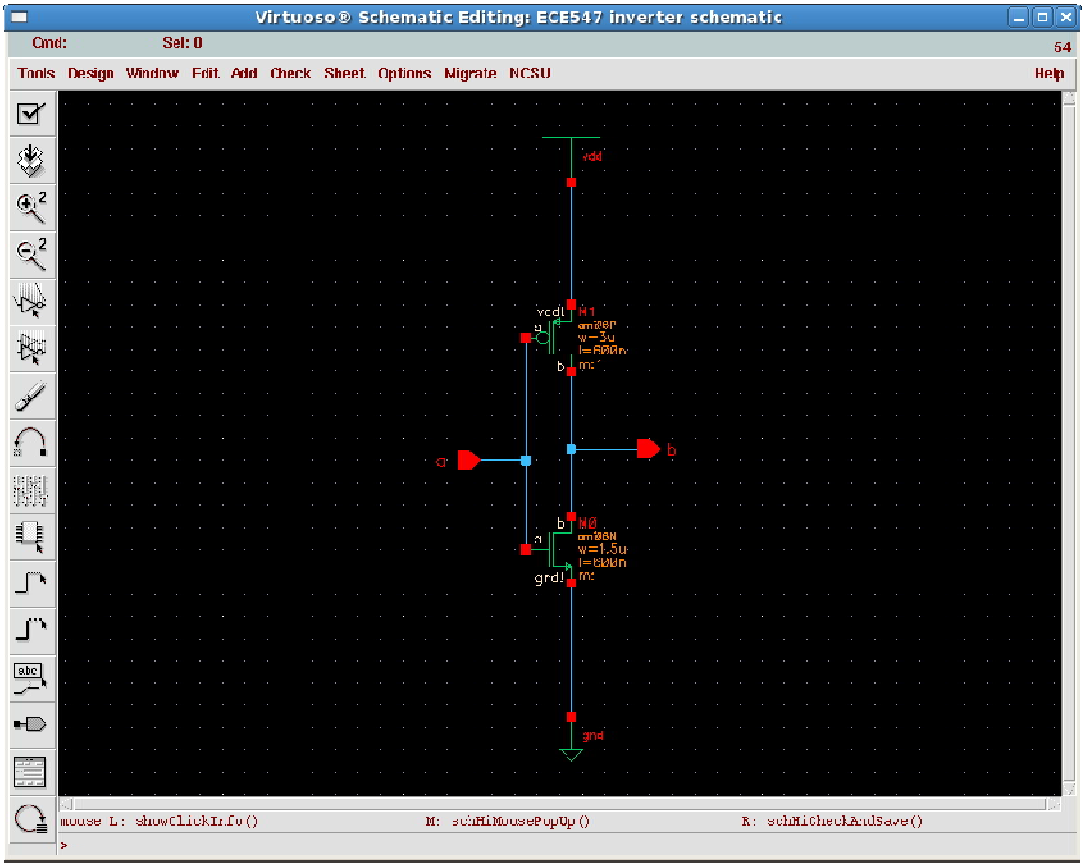

Fig A. 7 Inverter

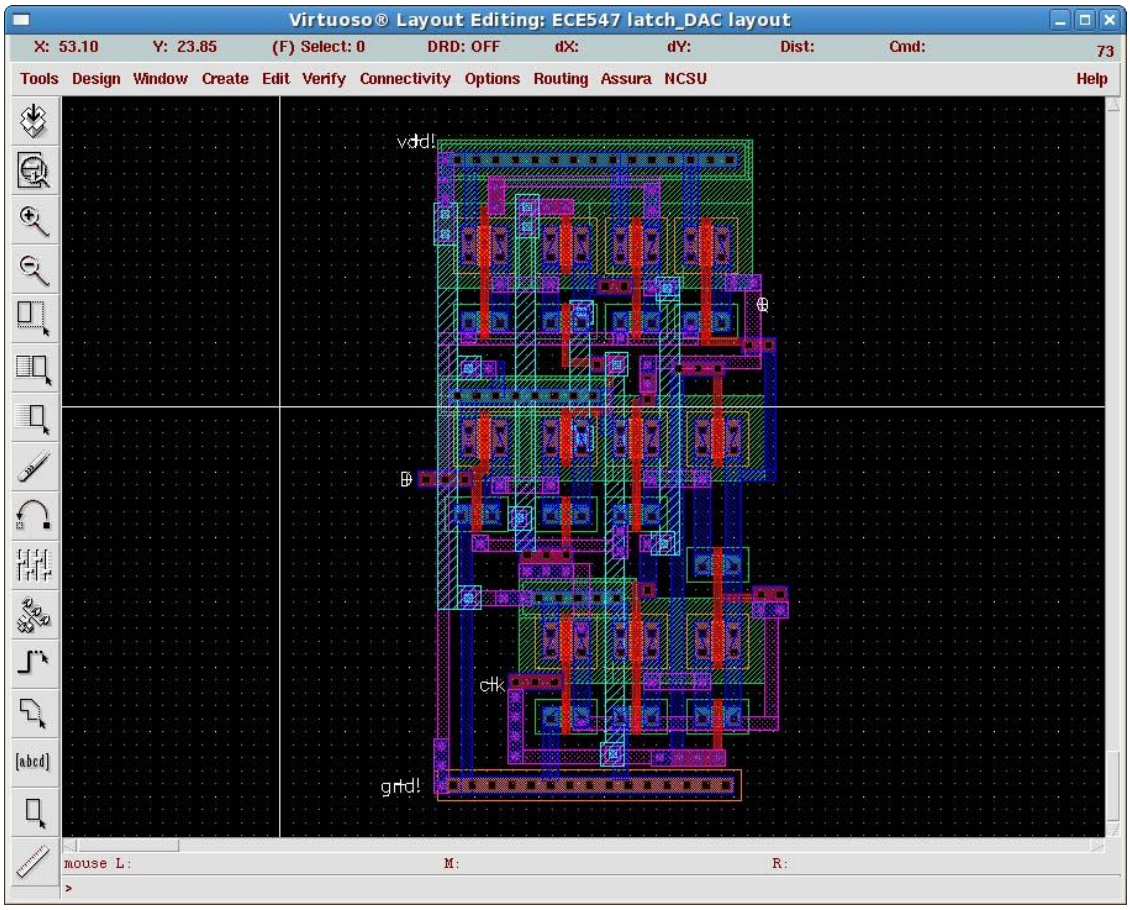

Fig B. 1 Register

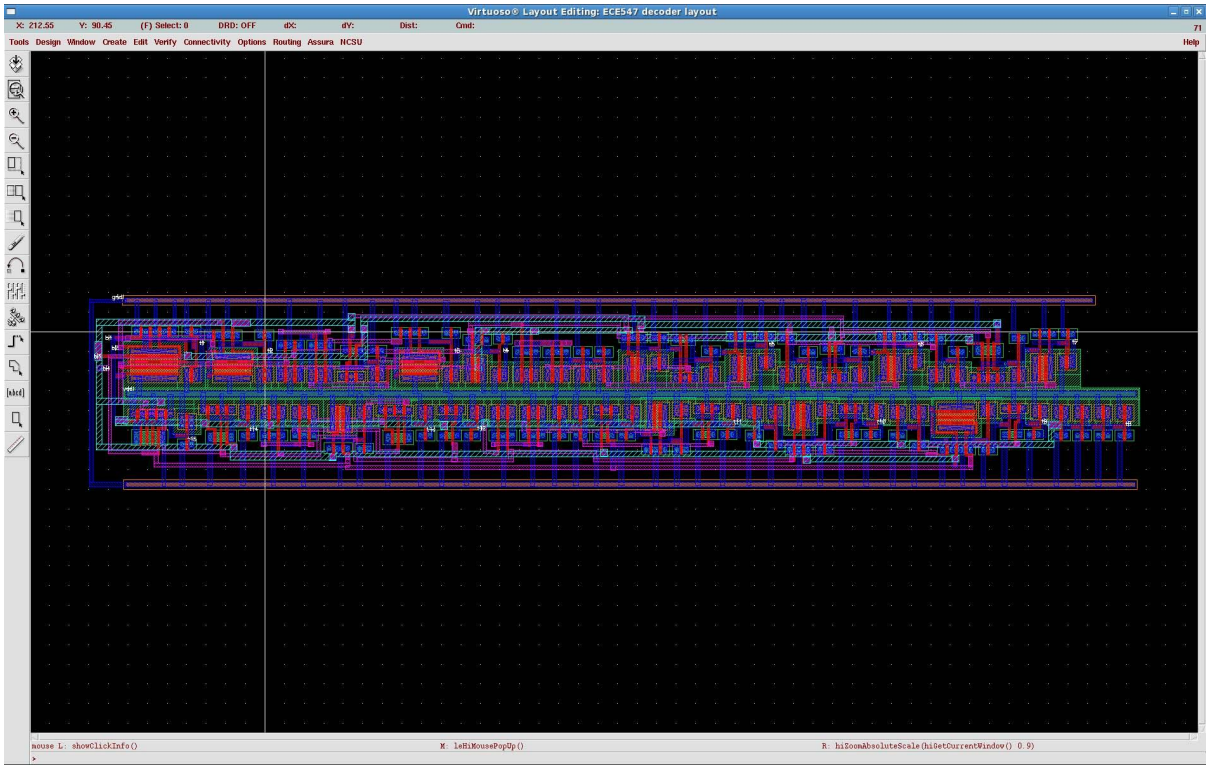

Fig B. 2 Decoder

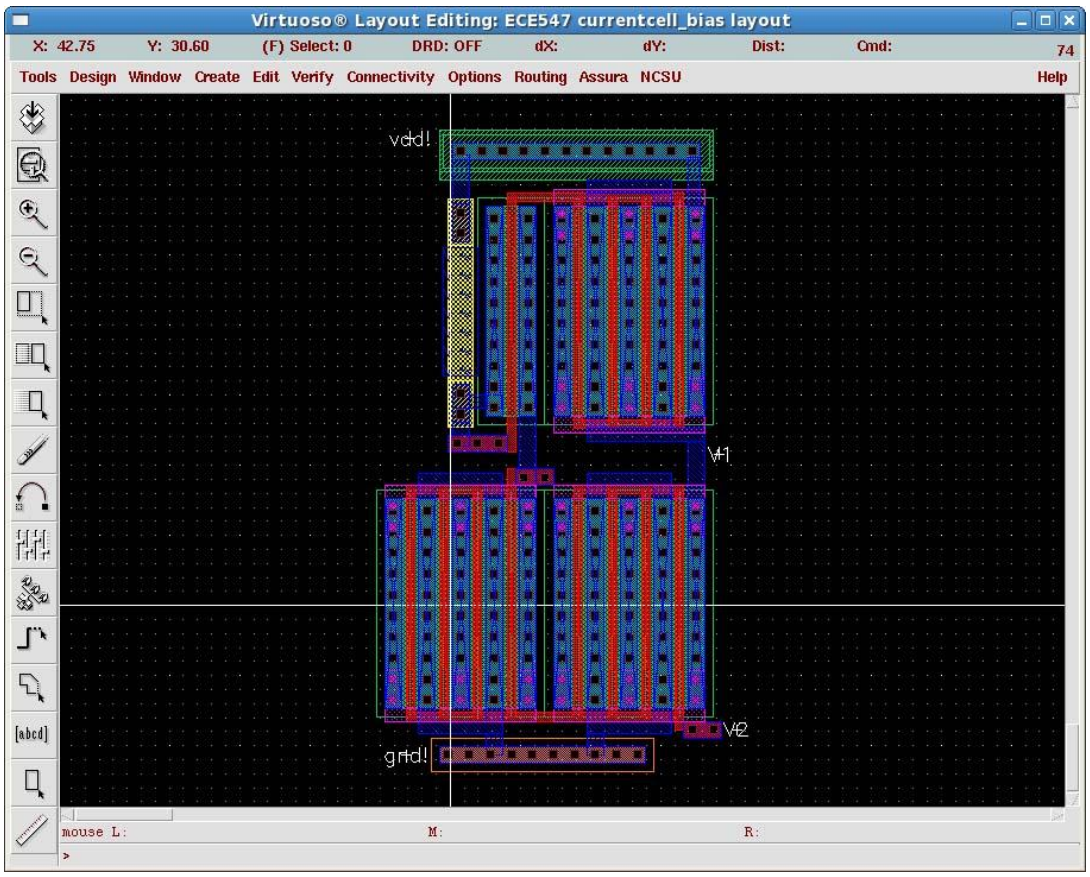

Fig B. 3 Current Cell Bias

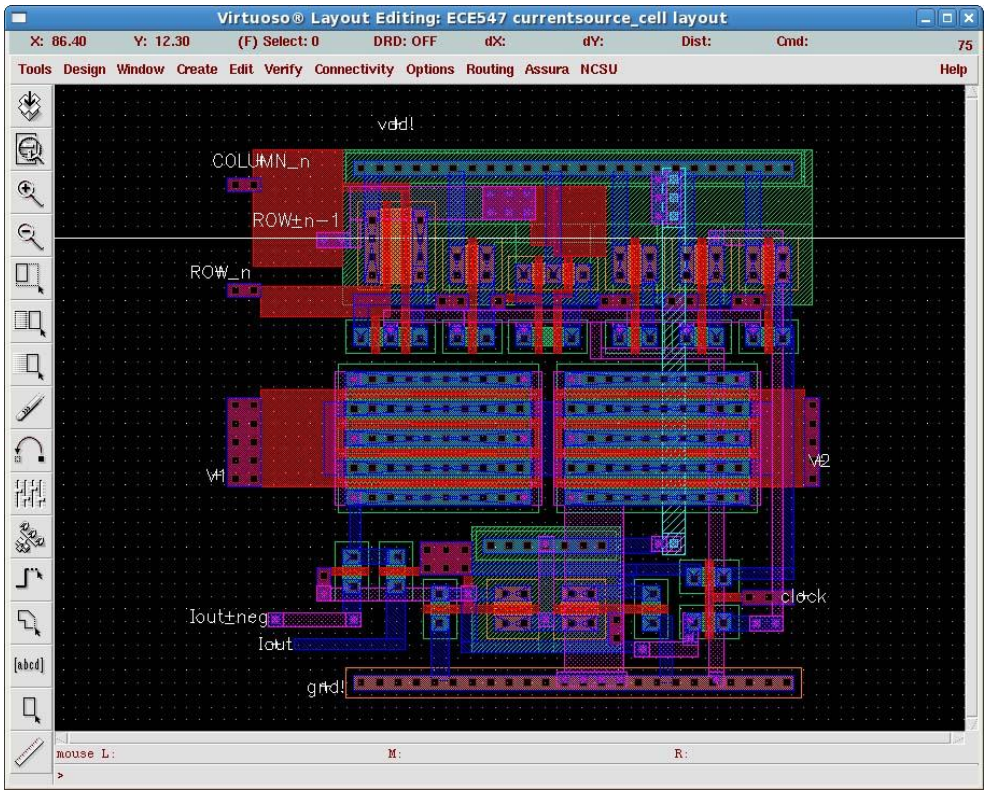

Fig B. 4 Current cell

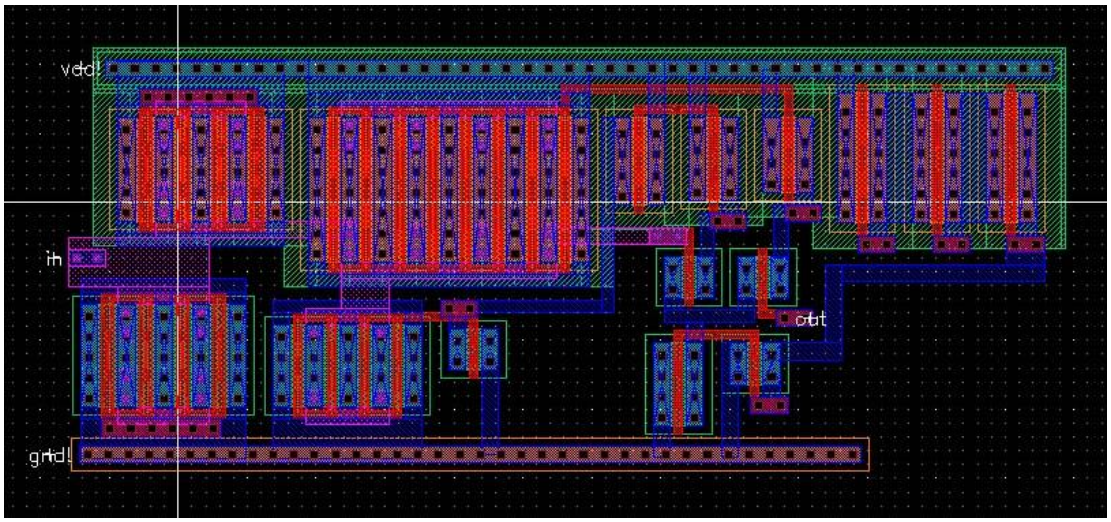

Fig B. 5 Buffer

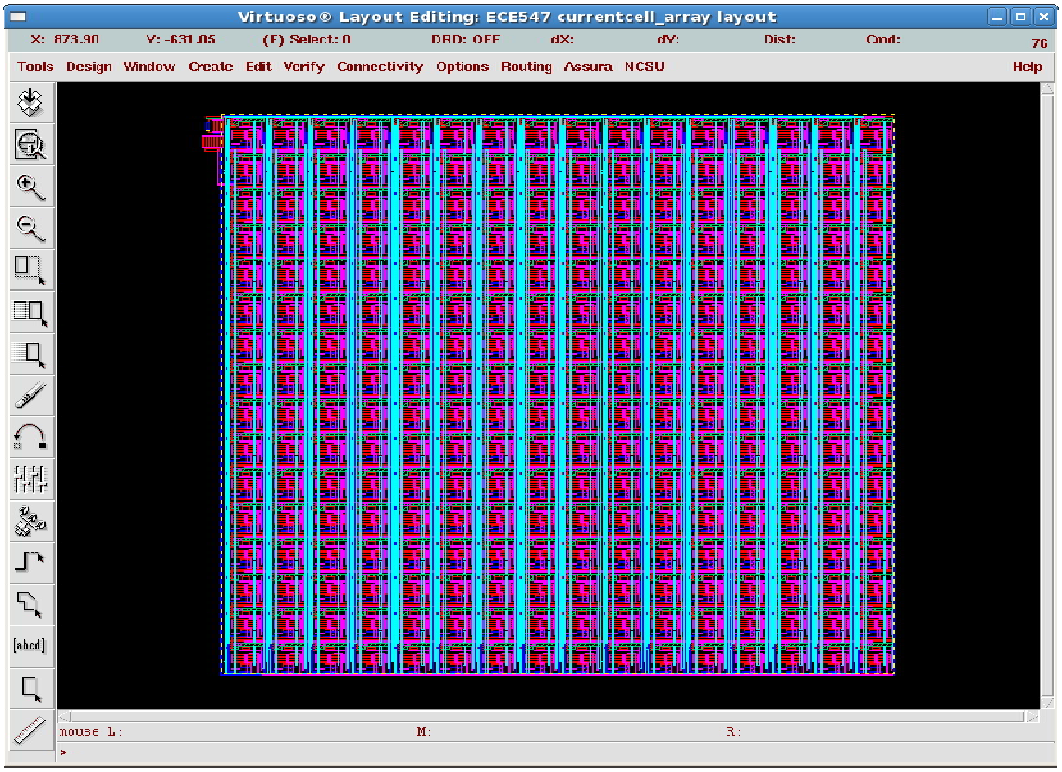

Fig B. 6 Current Cell Array

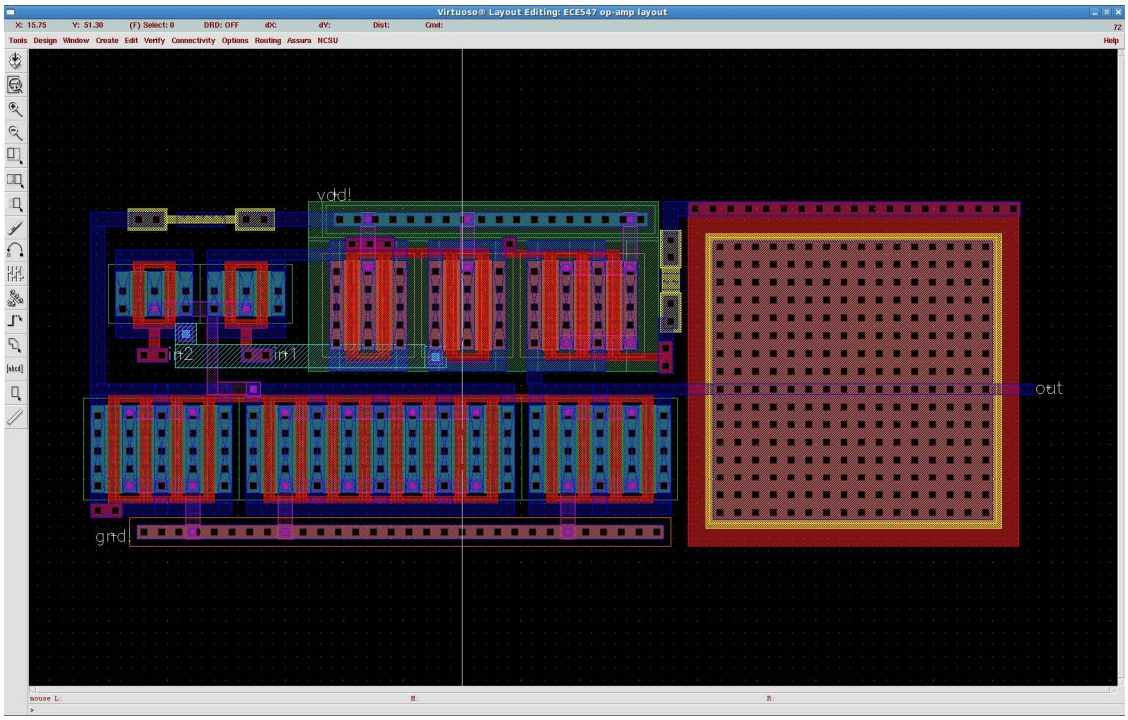
Virtuoso® Layout Editing: ECE547 op-amp layout
vdd!
in2
in1
out
gnd!

Fig B. 7 Op-amp