Design and Layout of a Telescopic Operational Transconductance Amplifier

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Contents

List of Tables

List of Figures

Chapter 1

Abstract

This paper presents a high speed Operational Transconductance Amplifier (OTA) that was designed to be used in a pipeline A/D converter. The design improves on the OTA used in a previous design by a University of Maine student[1]. It uses a telescopic architecture as well as gain-boosting to improve its settling time and DC gain. The design of the OTA was done as a summer research project sponsored by the National Science Foundation Research Experience for Undergraduates (NSFREU) program. The layout was done in Fall, 2002 with a graduate level course in VLSI design and layout (ECE 547). The OTA improved on the previous design and achieves very fast settling times in simulation (about 4.4ns for 10-bit accuracy level). It is currently used in a new Pipeline A/D Converter design by a University of Maine student [2].

Chapter 2

Introduction

2.1 Project Overview

The ECE 547 VLSI design presented in this paper is an Operational Transconductance Amplifier (OTA) to be used in an A/D Converter. The OTA was designed to have a fast settling time in a switched-capacitor application. A telescopic architecture was used, with gain boosting to improve DC gain and settling behavior. The Cadence software environment was used for all design, layout, and simulation. The final layout will be implemented through MOSIS, with AMI's C5N process. The minimum gate length in this technology is 0.6μm. The device will be packaged in a 40-pin ceramic DIP and tested in the spring of 2003.

2.2 Background

Operational Transconductance Amplifiers (OTA's) are used in microelectronics applications to drive small capacitive loads at high frequencies. An OTA is basically an op-amp without any output buffer, preventing it from driving resistive or large capacitive loads. They are preferred over op-amps mainly because of their smaller size and simplicity.

The OTA is based on a differential amplifier at the input. If the inputs are equal, the transistors in the differential pair conduct equal currents. When they change, the current changes through the pair. The purpose of an OTA is to generate a current proportional to an input voltage difference. This paper is concerned with the design of a fully differential OTA, meaning there are two outputs. The difference in the output currents should be proportional to the difference in the input voltages.

The problem of building a high speed OTA with the capability to settle to 10 bits came up as a result of a pipeline analog to digital converter (ADC) designed by two graduate students, Kannan Sockalingam and Rick Thibodeau [1]. Their design employed a folded-cascode OTA which operated at 5MHz. Its speed was a limiting factor in the performance of the ADC. Research was needed to investigate ways to improve the performance of this particular part of the converter circuit.

2.3 Objectives

The main objectives of the OTA design were 1) to make it capable of moving charge onto and off of 500fF capacitors with a settling time of less than 5μsec, 2) to make it fit in the same footprint as the folded cascode OTA designed by Kannan Sockalingam and Rick Thibodeau, and 3) to measure and compare open loop gain and bandwidth characteristics of a few different designs and layouts.

Chapter 3

Design Considerations

A telescopic OTA was used because of its simplicity over other designs, allowing for higher-speed operation. In a folded-cascode design, such as the one used by Sockalingam and Thibodeau, there is an input differential pair and two separate current branches for the differential output. The input currents are mirrored with a cascoded configuration to produce the output currents. The telescopic architecture puts both the input differential pair and the output on the same two current branches. This approach eliminates the noise problems caused by the current mirrors and also leads to a more direct signal path, which allows for higher speed. Another advantage of the telescopic architecture is that it uses half the bias current of a folded-cascode design because it has two fewer branches for current.

This chapter gives an overview of the circuit in four main sections: telescopic OTA architecture, gain-boosting, wide-swing cascode biasing, and common-mode feedback. Several articles have been published with telescopic OTA designs. The information on telescopic OTA's is gathered mostly from an IEEE publication by Mrinal Das of Texas Instruments [3]. CMOS Integrated Circuits by Baker [4] was also used as a general reference.

3.1 Telescopic OTA Architecture

The telescopic OTA used as a final design is shown in Figure 3.1. Input and output pins represent connections to nodes in the circuit (complete schematic in Figure 3.5). A differential pair is used to sense the input voltage difference. If the pair is operating in saturation, when one transistor is turned on, the other will turn off. The current through one leg will be sourced to the output while the other leg will sink current from the load. The input transistors were sized with a very large W/L ratio to provide the high transconductance required to quickly move charge onto the test capacitors.

Special care must be taken to ensure that the input differential pair is operating in saturation and not in the triode region. Operation in the triode region will cause the behavior of the OTA to be nonlinear and will result in poor transient response as well as a loss in DC gain. The telescopic architecture differs from other approaches because

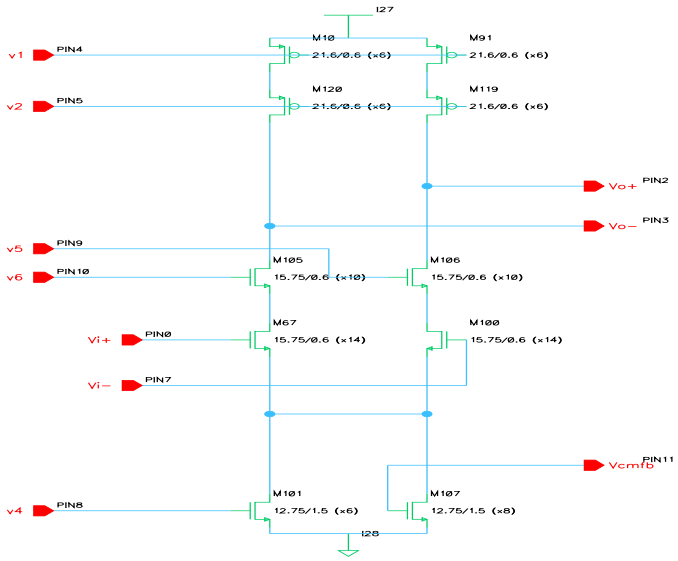

Figure 3.1: Telescopic OTA Architecture

it requires the common mode of the input to be different from the common mode of the output for the input differential pair to be in saturation and operate linearly. This will have to be taken into consideration before the telescopic design is used in a larger circuit. If the outputs are to be used as inputs to another OTA, their common mode must first be adjusted.

Transistors M105 and M106 buffer the output from the input. Both are operating in the triode region, causing them to act as small resistors. They are biased by the gain-boosting section of the OTA, which will be discussed in the next section.

3.2 Gain-Boosting

The idea of gain-boosting is shown in Figure 3.2. Essentially transistors M110 and M111 are acting as simple common-source NMOS amplifiers with current loads. The output of these auxiliary amplifiers is providing an output voltage to bias the gates of M105 and M106. The gain of this auxiliary amplifier is multiplied by the gain of the telescopic section to provide a much higher DC gain. The result is better settling accuracy without affecting the speed of the circuit, since it does not add gates into the signal path.

There has been research done to show that gain-boosting also improves settling time [3]. Increasing the current through the auxiliary amplifiers moves the non-dominant poles of the circuit to the imaginary axis, as was shown by Mrinal Das [3]. This also has the effect of increasing the unity gain bandwidth of the circuit. At some point, the

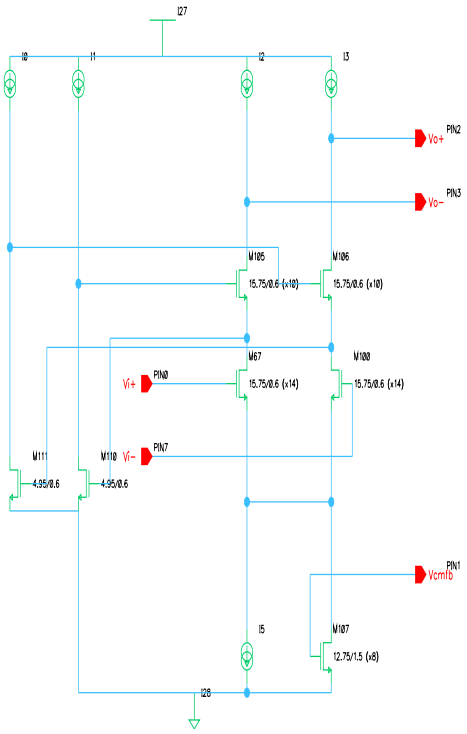

Figure 3.2: Gain-Boosting Section

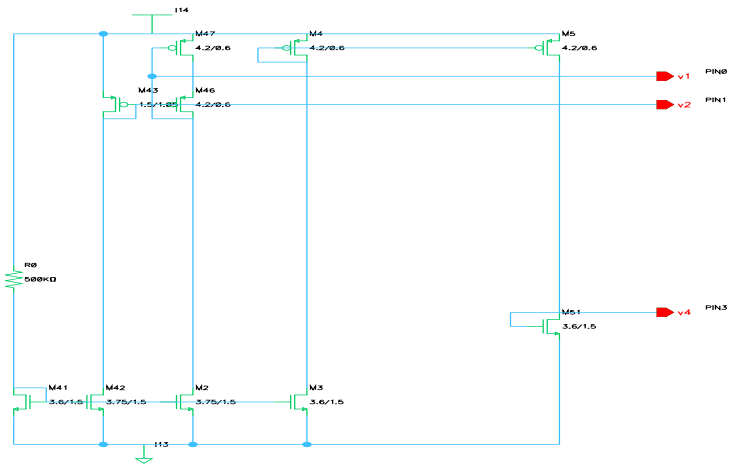

Figure 3.3: Wide-Swing Cascode Bias Circuit

gain of the auxiliary amplifiers is reduced to the point where the circuit does not settle to the desired accuracy. Too much increase in current will also lead to instability.

3.3 Wide-Swing Cascode Bias Network

The biasing network shown in Figure 3.3 is based on wide-swing cascode current mirrors as presented by Baker [4]. Cascode sources were chosen because it was necessary to keep the bias currents in the top half of the telescopic amplifier as constant as possible to ensure accurate settling. One transistor in the cascode configuration mirrors the current while the other basically acts as a buffer between the current source and changing voltages in the circuit. The wide-swing configuration reduces signal swing limitations encountered with normal cascode biasing. Cascode biasing was not necessary in the bottom half of the circuit because the common-mode feedback circuit works to adjust the bias current to keep the outputs from drifting. Common-mode feedback is discussed further in the next section.

3.4 Common-Mode Feedback

Common-mode feedback is necessary in a fully differential OTA to keep the outputs from drifting high or low out of the range where the amplifier provides plenty of gain.

The common-mode feedback (CMFB) circuit shown in Figure 3.4 is based on a design found in Baker's book [4]. It uses two differential pairs to sense the difference

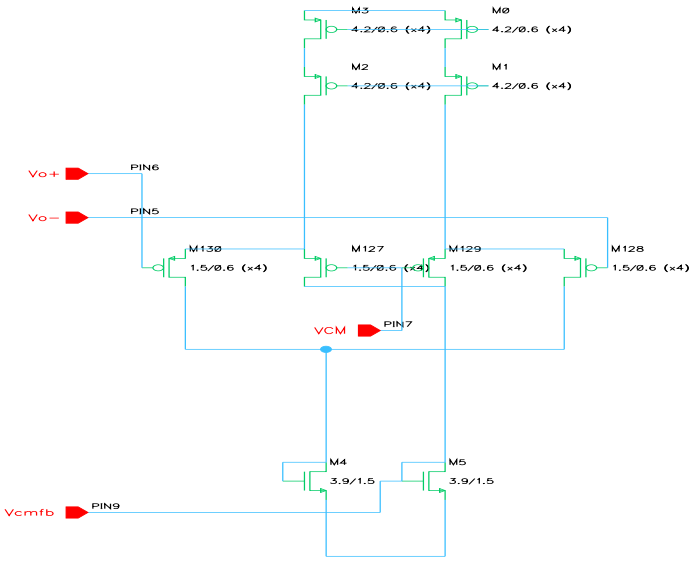

Figure 3.4: Common-Mode Feedback Circuit

between the average output voltage and a common mode voltage VCM which is supplied externally. Vcmfb is used to bias a transistor that adds to the bias current and keeps the common mode from drifting up. The current in the CMFB circuit does not need to be large as long as the currents through the top and bottom of the OTA are fairly well balanced. Since the common-mode feedback circuit only adds to the bias current in the bottom of the circuit, it is expected that the bias currents in the top half will be slightly higher. In this design, the total current through the CMFB section is about 20 μA.

3.5 Complete Circuit

Three different designs were included in the layout. The circuit design shown in Figure 3.5 is the design used in the A/D Converter (Design B). This replaced a previous design (Design A) which is also included for testing. The sizing of the common mode feedback and gain boosting sections is smaller in Design A. The schematics of both designs are included in Appendix A, and the layouts in Appendix B. The simulated DC gain of Design A was slightly lower, but still enough to satisfy the 10 bit accuracy requirement. Its transistor sizes are noticeably smaller than the first design, so it is of interest to see if comparable results can be achieved. The third design included for testing is the folded cascode OTA used in the A/D Converter designed by Sockalingam/Thibodeau [1].

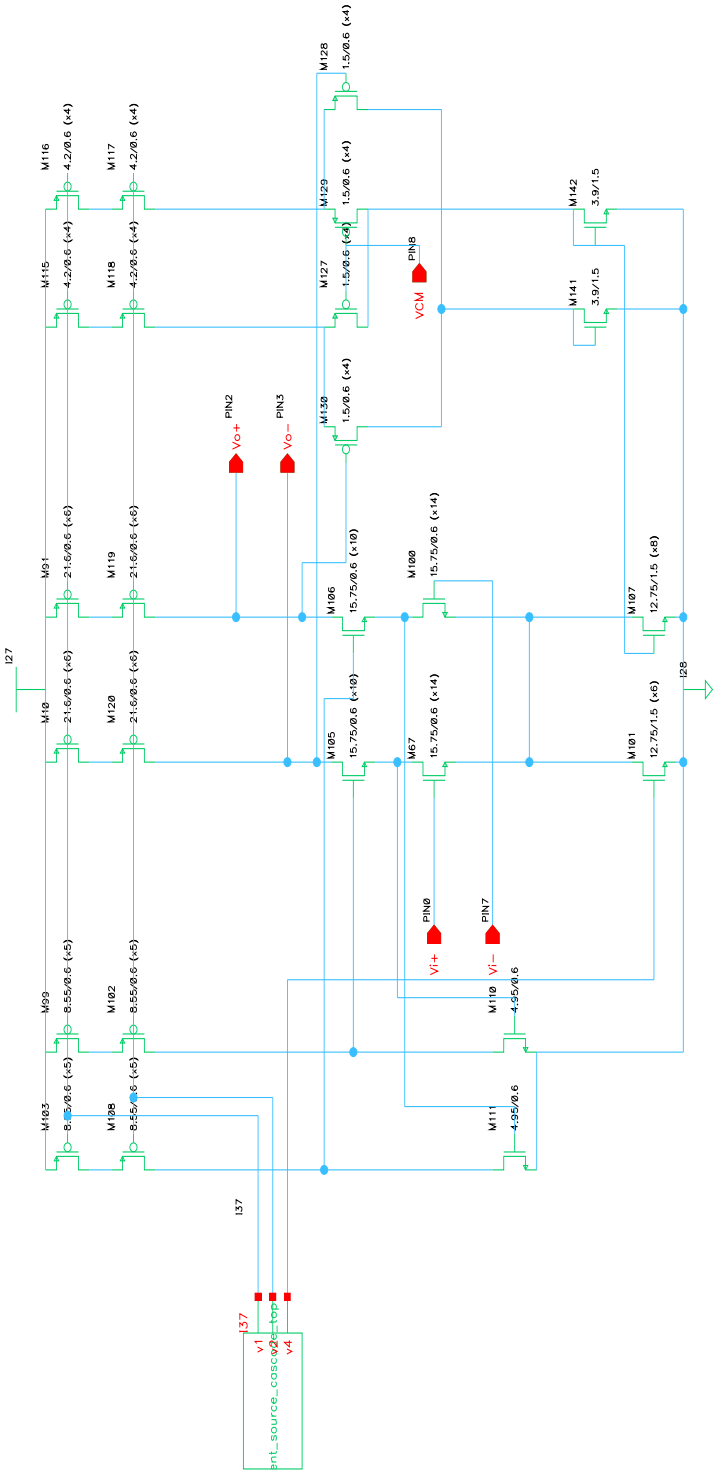

Figure 3.5: Completed Circuit Schematic

Chapter 4

Performance of the Telescopic OTA

This section will evaluate the performance of the OTA design in several different simulated tests, including transient and frequency response measurements.

4.1 Test Circuits

The test circuit used to evaluate the transient response of the OTA is shown in Figure 4.1. One volt difference is applied to the inputs via two 500fF capacitors. The charge on these capacitors is then transferred onto the feedback capacitors to produce a voltage difference of one volt at the output. The inputs are pulled together by the virtual short. The rise time of the step input to the circuit was chosen to be 2ns. A shorter rise time increases the speed of the step response slightly.

The circuit in Figure 4.2 was used to simulate the open-loop gain of the telescopic OTA with AC analysis in the Cadence software.

Inverting and non-inverting op-amp configurations were also included for testing the OTA. Figure 4.3 shows the inverting configuration. The input has an 880mV DC offset and the negative output is left open so the OTA acts as a single output rather than differential output amplifier. The resistors are included to give the OTA a feedback path and the output should have a finite gain.

Figure 4.4 shows the non-inverting configuration. In this test, the differential output is measured and compared to the differential input. The circuit should have a positive nonzero gain depending on the values of the resistors.

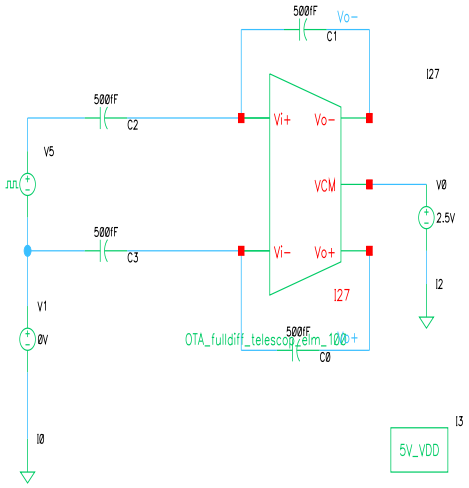

Figure 4.1: Test Circuit for Transient Response

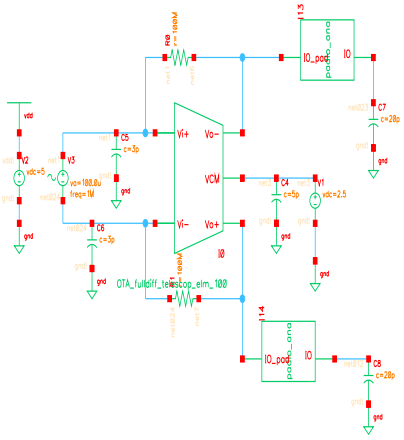

Figure 4.2: Test Circuit for Open-Loop Gain

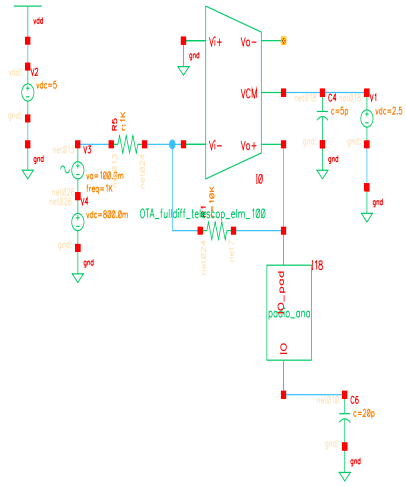

Figure 4.3: Test Circuit for Inverting Amplifier

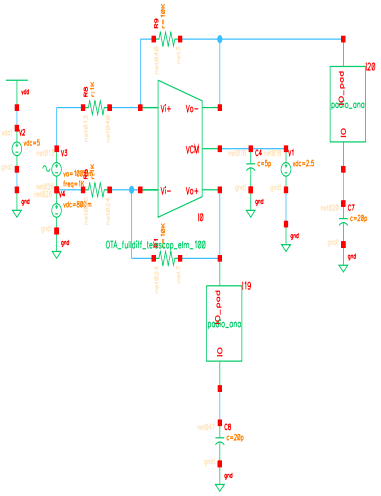

Figure 4.4: Test Circuit for Non-inverting Amplifier

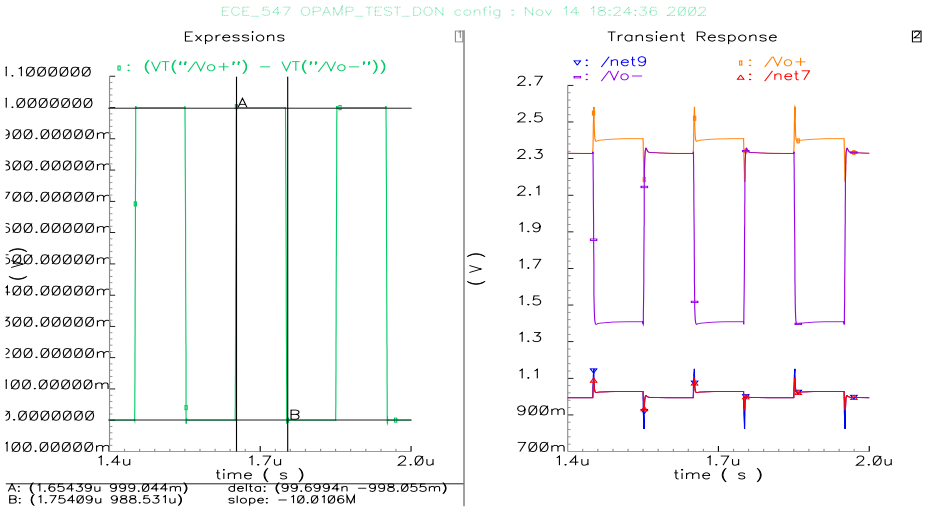

Figure 4.5: Simulated Transient Response

4.2 Simulated Results

The transient response of the test circuit is shown in Figure 4.5. The plot on the right shows the input and output of the OTA while the plot on the left shows the differential output voltage. The goal is to achieve a difference of 1V after settling between the outputs, with at least 10 bits accuracy. Notice that the common mode of the input signal is well below the output common mode to keep the input differential pair in the saturation region as discussed in section 3.1. The OTA achieves 10 bits as long as the output difference settles to within 2^{-10} V or approximately 1 mV. Figure 4.6 shows a typical settling time measurement. The differential output settles to 999mV in 4.4ns, and back down to less than 1mV in 4.1ns.

Figure 4.7 shows the simulated open loop gain. The simulated circuit had a DC gain of 67.8dB and a -3dB bandwidth of 865kHz. The plot also illustrates the frequency response of the output buffer compared to that of the OTA. The simulated unity gain frequency was above 1 GHz, however the analog output buffer makes high frequency measurements above 10MHz impossible. The buffer is required to drive the large capacitance added by a test probe.

Figure 4.8 shows the input and output of the inverting op-amp configuration. The measured gain is about -6V/V. The simulation shown uses design B with parasitic capacitances extracted.

Figure 4.9 shows the differential input and output of the non-inverting configuration to be tested on the chip. The results are shown for Design B with parasitic capacitances

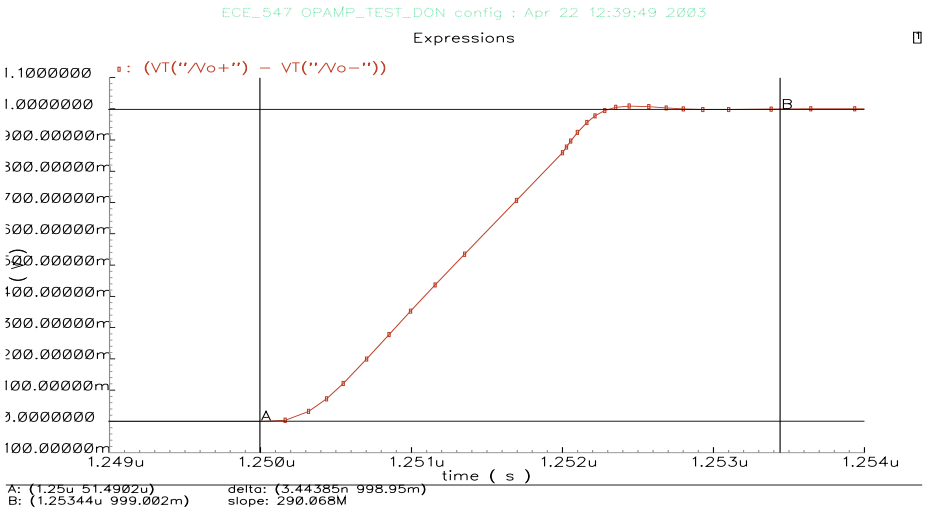

Figure 4.6: Settling Time Measurement for Rising Edge

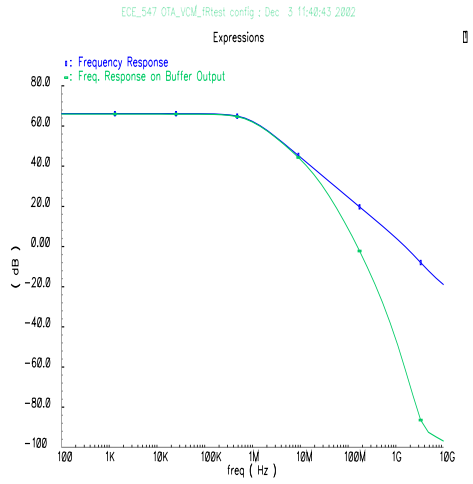

Figure 4.7: Simulated Frequency Characteristic

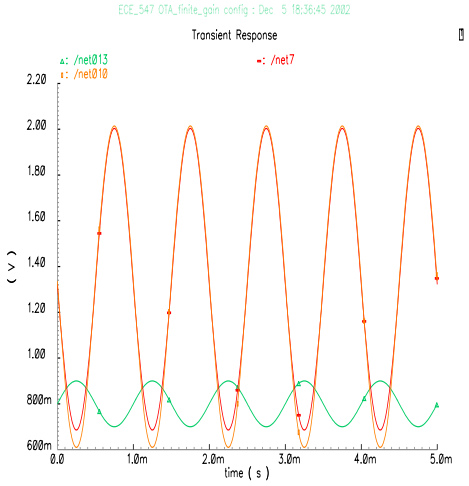

Figure 4.8: Inverting Op-Amp Test

extracted. The actual output voltages are shown on the right and the differential input and output waveforms are on the left.

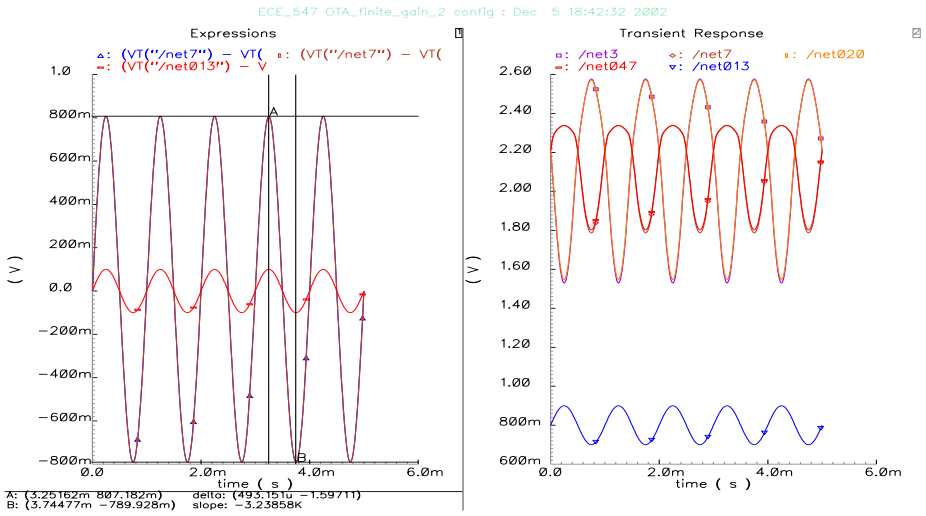

Figure 4.9: Non-inverting Differential Op-Amp Test

Chapter 5

Layout Considerations

The biggest goal with layout was to make the size of the OTA comparable to the OTA used in Sockalingham and Thibodeau's design, so that it could be used in their ADC with a minimum of modifications to the original layout. A complete set of layouts is in Appendix B. It was also a goal to keep the design somewhat symmetric, and avoid capacitive coupling, especially over the large differential input transistors. Improperly placing a wire directly over an input transistor showed a dramatic effect on the DC gain of the circuit due to coupling from parasitic capacitance. Figure B.3 shows a layout with such a connection to the Common Mode Feedback Section on the right side of the layout. This caused a loss of 4 to 5 dB of DC gain in simulation.

The final layout contains a total of 9 OTA's and one ring oscillator with digital buffer. Since the OTA's did not take up much space, fill was required on the chip to satisfy the fill rules used by MOSIS. Five large bypass capacitors were added to the layout with all three metal layers on top of them.

5.1 OTA Designs

The 9 OTA's included on the chip represent three different designs. The first is the OTA originally designed (design A) for use in the ADC. The second (design B) has a slightly larger CMFB section to address problems encountered with the original design in the ADC simulations. A design that is nearly identical to design A is also included, with the only difference being a wire routed over a large input transistor. This layout had a feedback problem that caused a considerable loss in DC gain during simulation. Moving the wire down a few microns fixed the problem. The bad layout was included to illustrate the importance of parasitic capacitances. Also included for testing is the folded-cascode OTA used by Kannan Sockalingam and Rick Thibodeau in their A/D Converter Design.

5.2 Ring Oscillator

The ring oscillator and buffer was designed to drive a 40pF load at 250MHz. With parasitics extracted the oscillator frequency dropped to about 214MHz.

5.3 Pinout Table

The pinout was chosen so that the pins with the least capacitance were OTA outputs, and those with high capacitance were power supply and inputs to the OTA.

Table 5.1: Pinout Table

PIN NO.	NAME	DESCRIPTION
1	GND	Ground
2	OTA Input	Input Vi- of OTA with feedback problem
3	OTA Input	Input Vi+ of OTA with feedback problem
4	OTA Input	Input Vi- of non-inverting op-amp (design B)
5	OTA Input	Input Vi+ of non-inverting op-amp (design B)
6	OTA Output	Output Vo- of non-inverting op-amp (design B)
7	OTA Output	Output Vo+ of non-inverting op-amp (design B)
8	OTA Output	Output Vo- of OTA with feedback problem
9	OTA Output	Output Vo+ of OTA with feedback problem
10	OTA Output	Output Vo- of OTA for Open Loop Gain measurement (design B)
11	OTA Output	Output Vo+ of OTA for Open Loop Gain measurement (design B)
12	OTA Output	Output Vo- of inverting op-amp (design B)
13	OTA Output	Output Vo+ of inverting op-amp (design B)
14	OTA Input	Input Vi- of inverting op-amp (design B)
15	OTA Input	Input Vi+ of inverting op-amp (design B)
16	OTA Input	Input Vi- of OTA for Open Loop Gain measurement (design B)

(Continued on next page)

Table 5.1: (continued)

PIN NUMBER	PIN NAME	DESCRIPTION
17	OTA Input	Input Vi+ of OTA for Open Loop Gain measurement (design B)
18	OTA Input	Input Vi- of OTA for Open Loop Gain measurement (design A)
19	OTA Input	Input Vi+ of OTA for Open Loop Gain measurement (design A)
20	VCM	Output Common Mode Voltage (Normally 2.5V)
21	VDD	Supply Voltage (Normally 5V)
22	OTA Input	Input Vi- of non-inverting op-amp (design A)
23	OTA Input	Input Vi+ of non-inverting op-amp (design A)
24	OTA Input	Input Vi- of inverting op-amp (design A)
25	OTA Input	Input Vi+ of inverting op-amp (design A)
26	OTA Output	Output Vo- of inverting op-amp (design A)
27	OTA Output	Output Vo+ of inverting op-amp (design A)
28	OTA Output	Output Vo- of non-inverting op-amp (design A)
29	OTA Output	Output Vo+ of non-inverting op-amp (design A)
30	OTA Output	Output Vo- of OTA for Open Loop Gain measurement (design A)
31	OTA Output	Output Vo+ of OTA for Open Loop Gain measurement (design A)
32	OTA Output	Output Vo+ of OTA for Open Loop Gain measurement (cascoded OTA)
33	OTA Output	Output Vo- of OTA for Open Loop Gain measurement (cascoded OTA)
34	OTA Output	Output Vo+ of OTA (design A)
35	OTA Output	Output Vo- of OTA (design A)
36	OTA Input	Input Vi+ of OTA (design A)
37	OTA Input	Input Vi- of OTA (design A)
38	OTA Input	Input Vi+ of OTA for Open Loop Gain measurement (cascoded OTA)
39	OTA Input	Input Vi- of OTA for Open Loop Gain measurement (cascoded OTA)

(Continued on next page)

Table 5.1: (continued)

PIN NUMBER	PIN NAME	DESCRIPTION
40	Ring Oscillator	Output of ring oscillator designed for 250 MHz operation

Chapter 6

Verification

The top level layout was verified with both Design Rule Check (DRC) and Layout Versus Schematic (LVS).

6.1 LVS Summary

Net-list summary for /usr/students/emccarth/NSFREU2002/LVS/layout/netlist
count
395 nets
40 terminals
21 res
5 cap
1335 pmos
1295 nmos
The net-lists match.

Chapter 7

Testing Procedure

This chapter describes the testing procedure and results of testing on the completed chip done in Spring 2003. Design A is the original OTA design. Design B has a larger CMFB section to improve performance. The folded-cascode OTA is the design used in the pipeline A/D converter designed by Sockalingam and Thibodeau [1].

A Yokogawa DL7100 digitizing oscilloscope with 500MHz bandwidth and 1Gs/sec sampling rate was used for all measurements. The test signal was provided by an Agilent 33250A signal generator.

Five chips were made and each was at least powered up, although one chip was chose for the most extensive testing. There was some variation between them that was evident at power up. Two of the chips drew a current of between 170 and 180mA, while the other three drew 300-400mA, a substantial difference in power consumption. The ring oscillator output seemed to correspond somewhat to the current draw, discussed in section 7.5.

7.1 Open Loop Gain

The open loop gain of each OTA was measured by connecting a low frequency (1kHz) 2mV_{pp} sine wave to the inputs. The oscilloscope measured both outputs and the difference signal. The negative input V- was referenced to a DC voltage, which was adjusted until the gain of the OTA was at its highest. In all cases this was found to be about 1.8V. The common mode reference voltage was 2.5V.

7.1.1 Designs A and B

Design A had a measured open-loop gain of 1000V/V or 60dB. The simulated open loop gain was about 69dB. Design B had a measured gain of about 450V/V, only 53dB. This was much lower than the expected value and also much lower than the gain for design A, which was a surprise. Figures 7.1 and 7.2 (page 24) show the open loop gain measurements for Designs A and B. The output difference (CH1-CH2) is measured. All tests have a 2V_{pp} input signal. The wiring problem that caused a small loss in OL

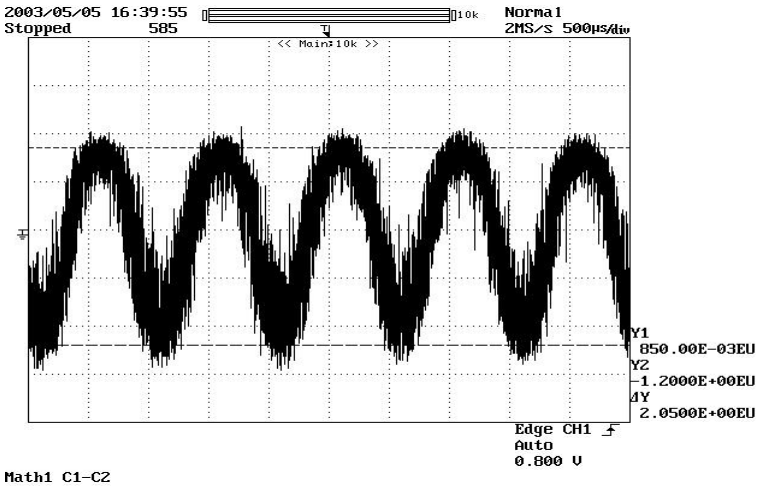

Figure 7.1: Open Loop Gain Measurement - Design A

gain in simulation did not seem to have a large effect in testing. This measurement is included in Figure 7.3 (page 24).

7.1.2 Folded-Cascode OTA

The folded-cascode OTA had a measured open-loop gain of 300V/V or 50dB. The difference signal is shown in Figure 7.4 (page 25).

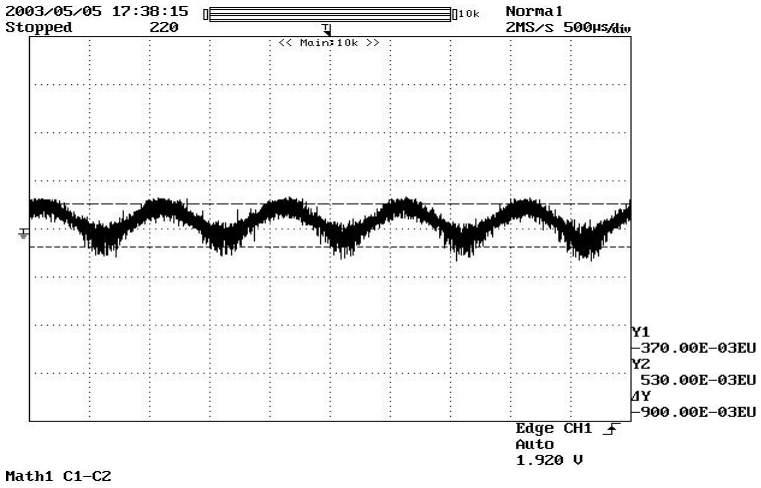

Figure 7.2: Open Loop Gain Measurement - Design B

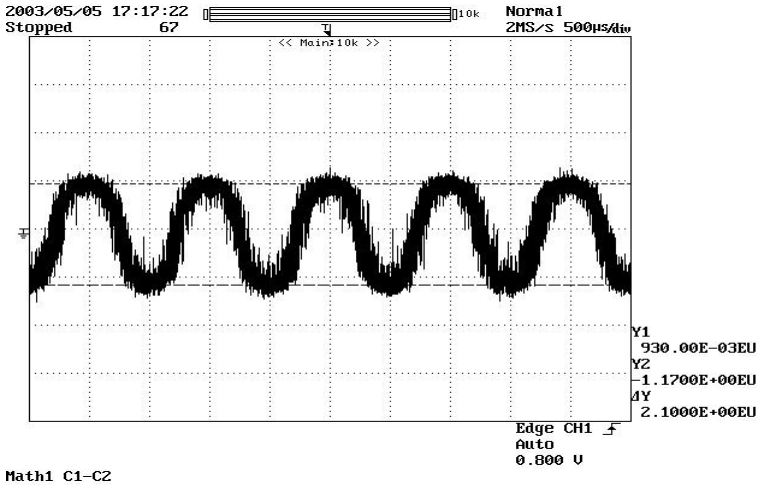

Figure 7.3: Open Loop Gain Measurement - Design A With Feedback Problem

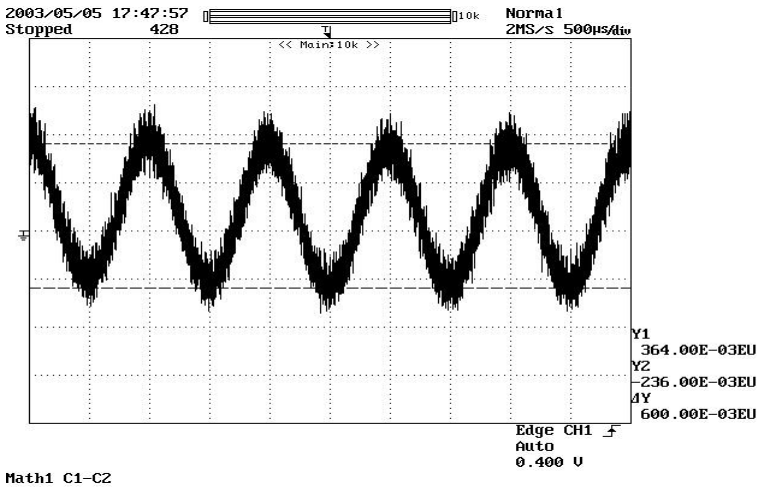

Figure 7.4: Open Loop Gain Measurement - Cascoded OTA

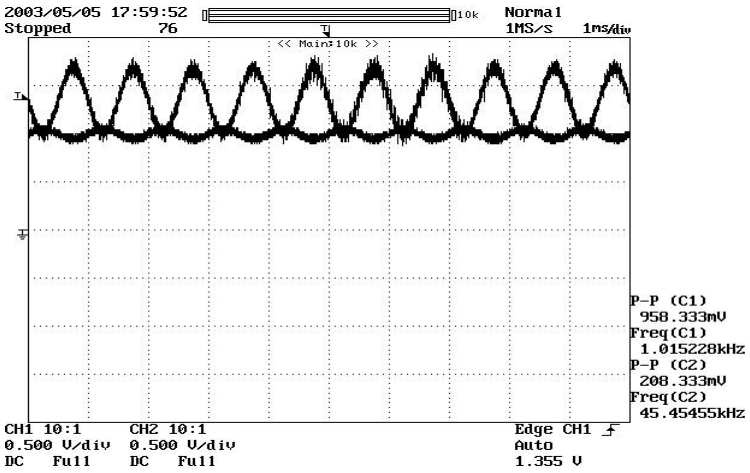

Figure 7.5: Typical Inverting Op-Amp Output (DC Coupled)

7.2 Bandwidth

Bandwidth was measured by adjusting the frequency of the input signal until the open-loop gain of the OTA had decreased by 3dB from its low-frequency value.

Design A had a measured -3dB bandwidth of 1.5MHz. This was slightly higher than expected. In simulation, it had seemed that the output buffer would limit the bandwidth to under 1MHz. The OTA with an improperly placed wire had the same bandwidth as Design A. This was consistent with simulation.

The folded-cascode OTA had a measured -3dB bandwidth of about 1MHz. It is expected that the bandwidth measured was really the bandwidth of the output buffer and not the bandwidth of the OTA in all of these measurements.

7.3 Inverting Op-Amp

The inverting op-amp was tested by connecting Vi+ to ground, and the input signal to Vi-. A DC offset of about 1V was necessary to operate the op-amp properly. The output was measured at the positive output and the negative output was left floating. Figure 7.5 shows a typical input and output with DC coupling.

7.3.1 Designs A and B

Both op-amps had close to the simulated gain (about 7V/V). Figures 7.6 and 7.7 show the gain measurements for Designs A and B, respectively.

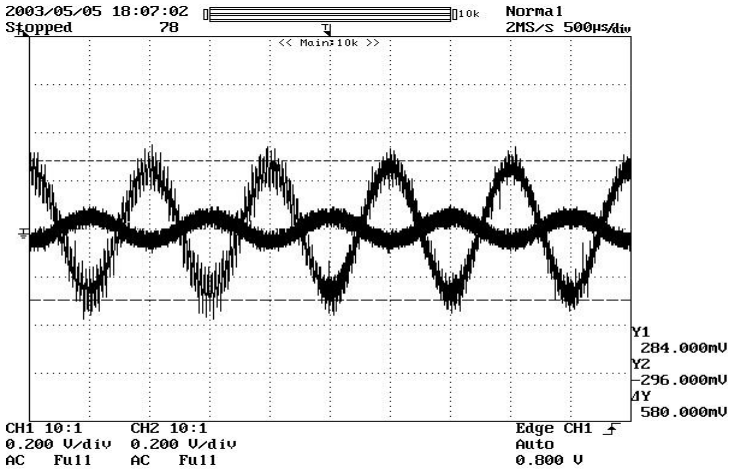

Figure 7.6: Design A Inverting Op-amp Test - Gain Measurement

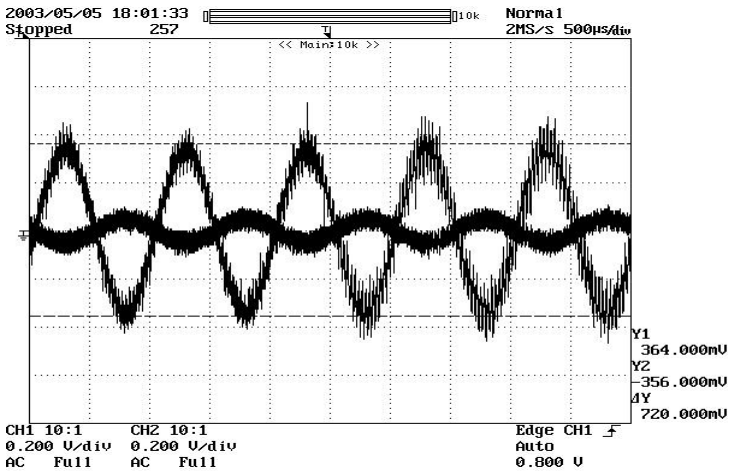

Figure 7.7: Design B Inverting Op-amp Test - Gain Measurement

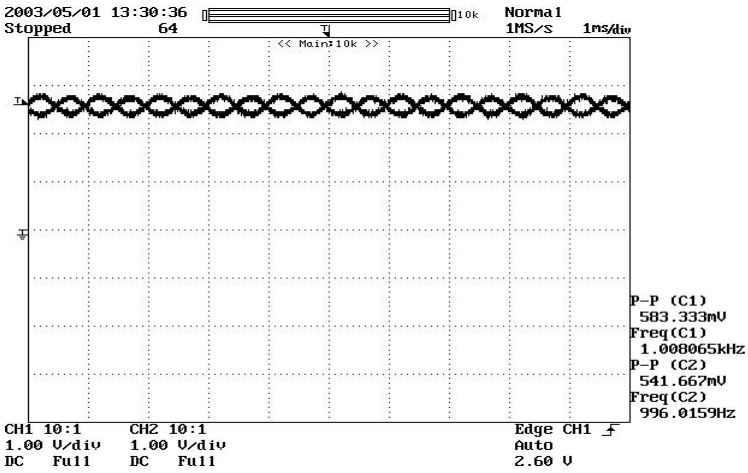

Figure 7.8: Design A Non-inverting Op-amp Test - Output Voltages

7.4 Non-inverting Op-Amp

7.4.1 Design A

The non-inverting op-amp was tested by applying a 1kHz, 100mV_{pp} sine wave to the differential inputs. The Vi- input was referenced to 1.8V DC and the outputs were measured. The output waveforms looked very similar to simulation. For Design A, the differential voltage gain at 1 kHz was measured to be about 7V/V. Figure 7.8 shows the positions of Vo+ and Vo- and Figure 7.9 shows the differential output voltage measurement.

Design B was tested in the same way, using a 100mV_{pp} input signal. Figures 7.10 and 7.11 (pages 29,30) show the resulting outputs for design B.

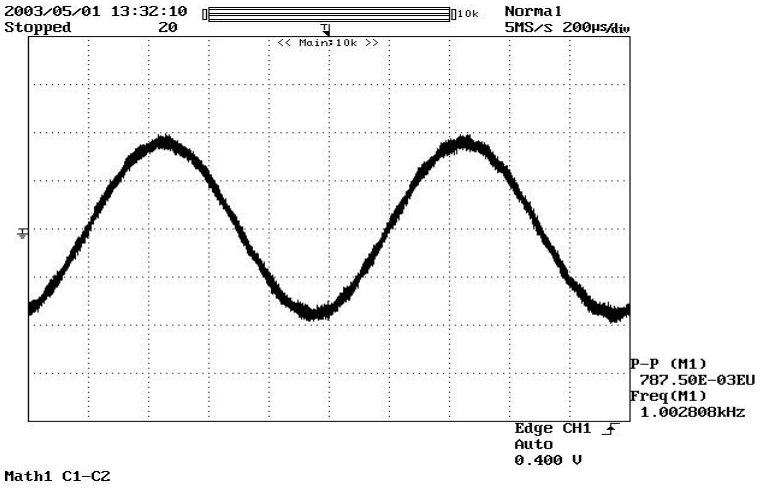

Figure 7.9: Design A Non-inverting Op-amp Test - Differential Output Measurement

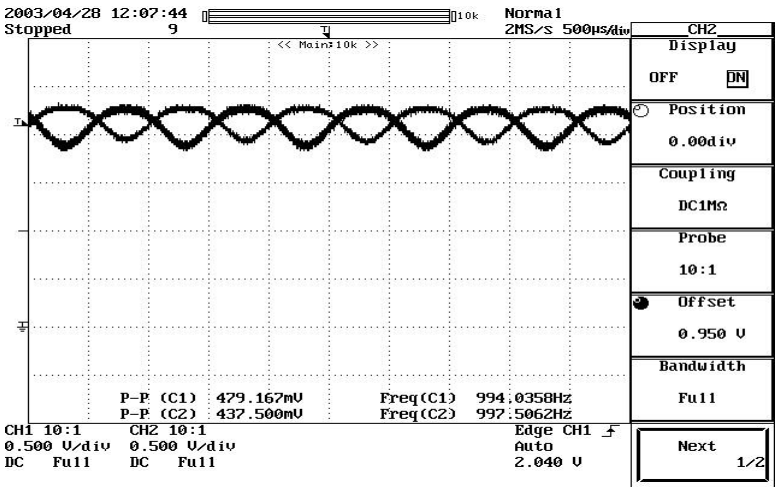

Figure 7.10: Design B Non-inverting Op-amp Test - Output Voltages

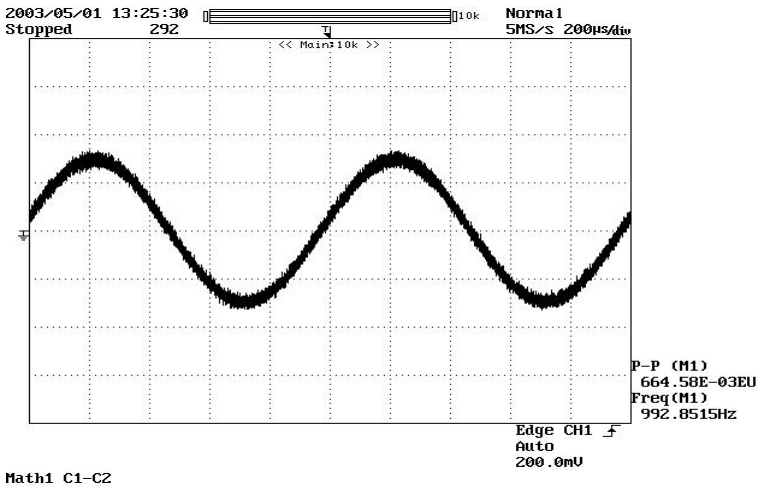

Figure 7.11: Design B Non-inverting Op-amp Test - Differential Output Measurement

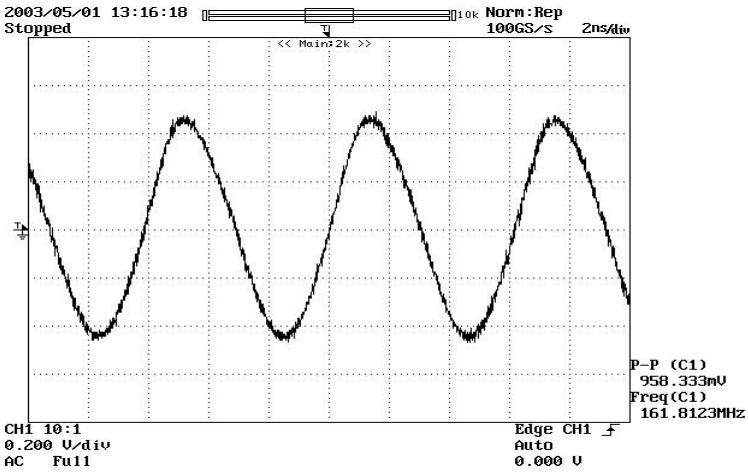

Figure 7.12: Ring Oscillator Output - Chip #1

7.5 Ring Oscillator

The ring oscillator did not perform up to its expected frequency or voltage swing. With a 5V power supply, the frequency of oscillation was only 160MHz, and the voltage swing was about 1V. Figure 7.12 shows the output of the ring oscillator with a +5V power supply. Decreasing the power supply did improve the shape of the waveform, but also decreased the frequency further. Since the ring oscillator is on pin 40, it has a long bond wire to the pin, which adds a lot of inductance and capacitance. It is suspected that the output buffer was not large enough to drive this capacitance, resulting in the low output swing.

There was a chip-to-chip variation in the performance of the ring oscillator. As discussed before, 3 of the 5 chips drew significantly more current than the other two. These three chips seemed to have a slightly greater voltage swing (about 1.5V), but slightly lower oscillation frequencies (120-140MHz). Figure 7.13 shows the measurement from one of these chips.

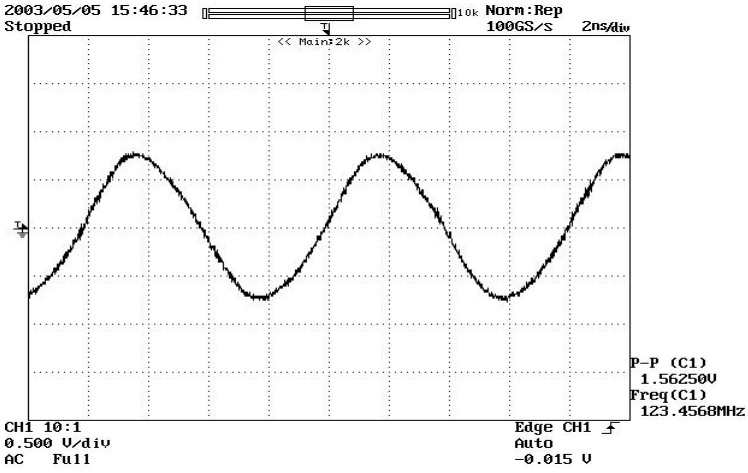

Figure 7.13: Ring Oscillator Output - Chip #3

Chapter 8

Conclusions

An OTA was designed that improved drastically on the folded-cascode method. Speed of the OTA was more than ten times faster than the previous design, with only about twice as much quiescent current. The telescopic OTA was used to provide a simpler structure which facilitated this increase in speed.

The telescopic design presented here also has a higher DC gain than the folded cascode design, allowing it to achieve 10-bit accuracy. Gain boosting contributed to the DC gain of the OTA without reducing the speed.

It is difficult to test the OTA at high frequencies because the tests are limited by the bandwidth of the output buffers. However, simulations show the output is reliable up to about 10MHz, which is sufficient to find the 3dB bandwidth of the OTA. Unfortunately, the output buffers will make Gain-Bandwidth Product measurements impossible. Since OTA's are designed to drive small capacitances very fast, the capacitance of a probe on the unbuffered output would have a severe effect on measurements.

In the A/D Converter, the OTA is used to move charge onto 1-2pF capacitors. A practical transient response test is not used, because probing the terminals of the OTA would make this capacitance seem insignificant and invalidate the results. Instead, simple inverting and non-inverting configurations are used to see if the OTA is operating properly.

8.1 Future Work

The OTA layout could be further optimized to take up less space, and also to get better symmetry. As it is, the OTA does not seem to be slowed down significantly by parasitic capacitances, although there was a slight decrease in gain compared with the schematic simulations.

8.2 Time Commitment

The pace of this course was very fast, and there was a large time commitment. I had the advantage of completing most of the design phase for summer research sponsored by

the National Science Foundation Research Experience for Undergraduates (NSFREU) program. That included research leading up to the selection of a telescopic OTA. The NSFREU program was a full time job for 10 weeks, giving a total of 400 hours on design even before the course began. Layout also took a considerable amount of time to learn, as well as leading to resizing most of my original design.

8.3 Biography of Author

Erik McCarthy is from Greene, Maine. He graduated from Leavitt Area High School in 1999. He is currently a fourth-year electrical engineering major at the University of Maine and will be graduating in May, 2003. He has spent two summers doing research as part of the National Science Foundation Research Experience for Undergraduates (NSFREU) program at the University of Maine and also worked as an intern for Harriman Associates, an architectural engineering firm in Auburn, Maine. His interests include analog circuit design, VLSI, and communications.

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[3] M. Das, “Improved design criteria of gain-boosted cmos ota with high-speed optimizations,” *IEEE Trans. Circuits and Systems*, vol. 49, pp. 204–207, Mar. 2002.

[4] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. New York, NY: Institute of Electrical and Electronics Engineers, Inc., 1998.

Appendix A

Schematics

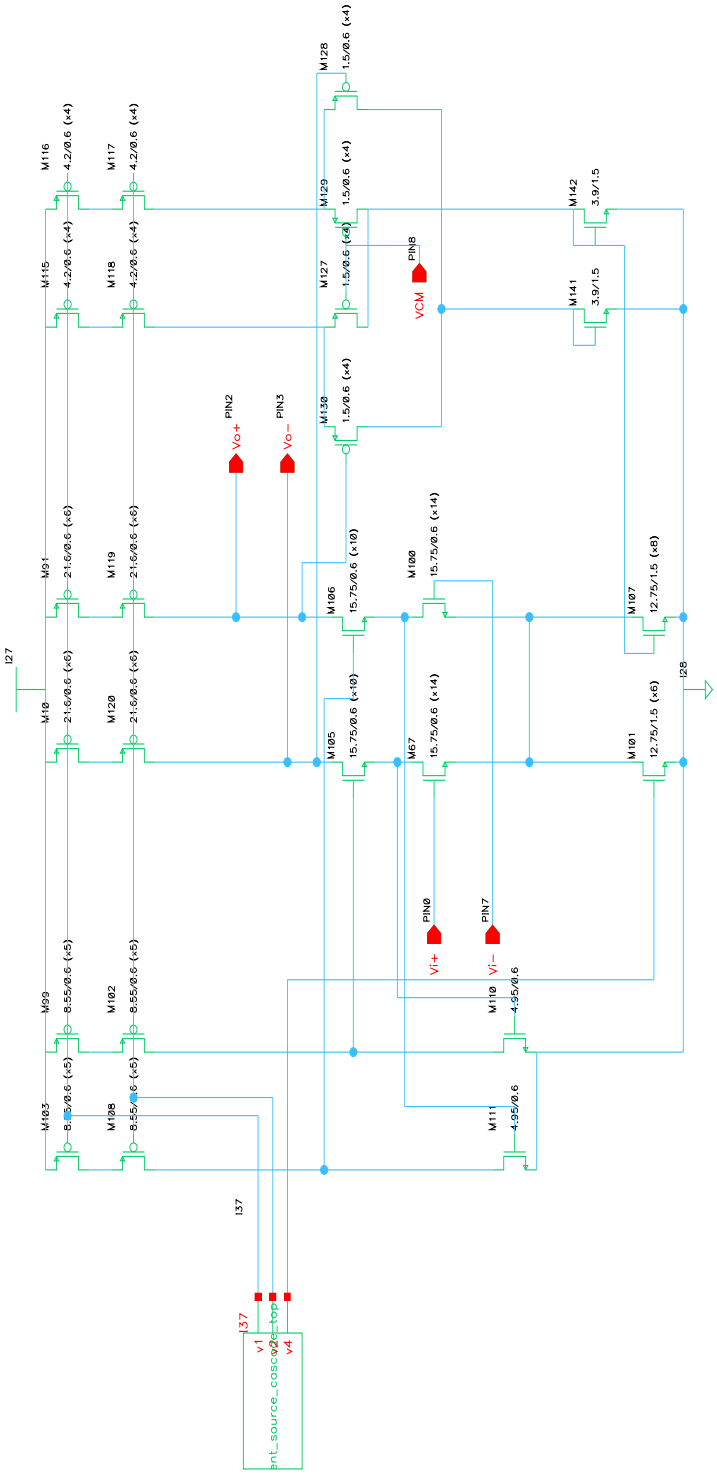

Figure A.1: Primary Design Used In ADC (design B)

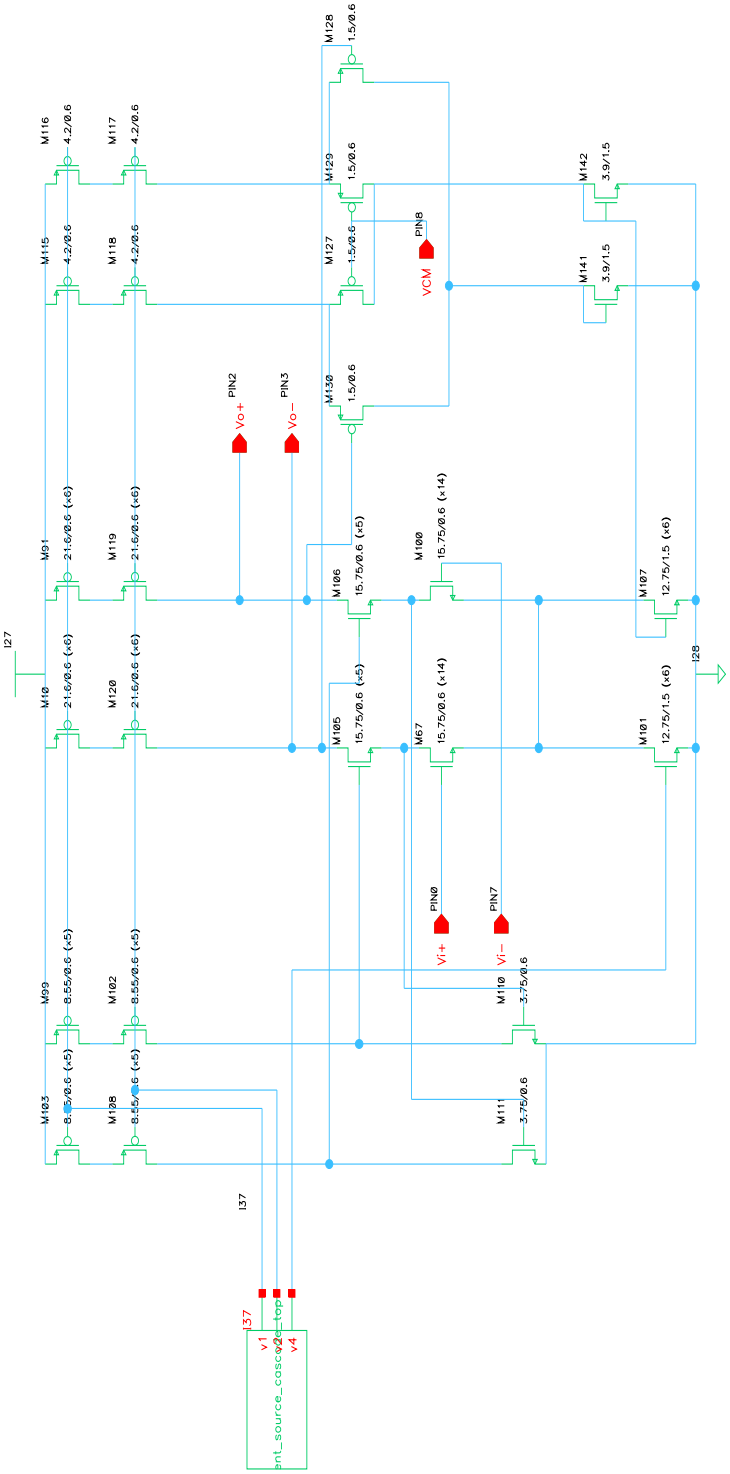

Figure A.2: Design With Smaller CMFB Section (design A)

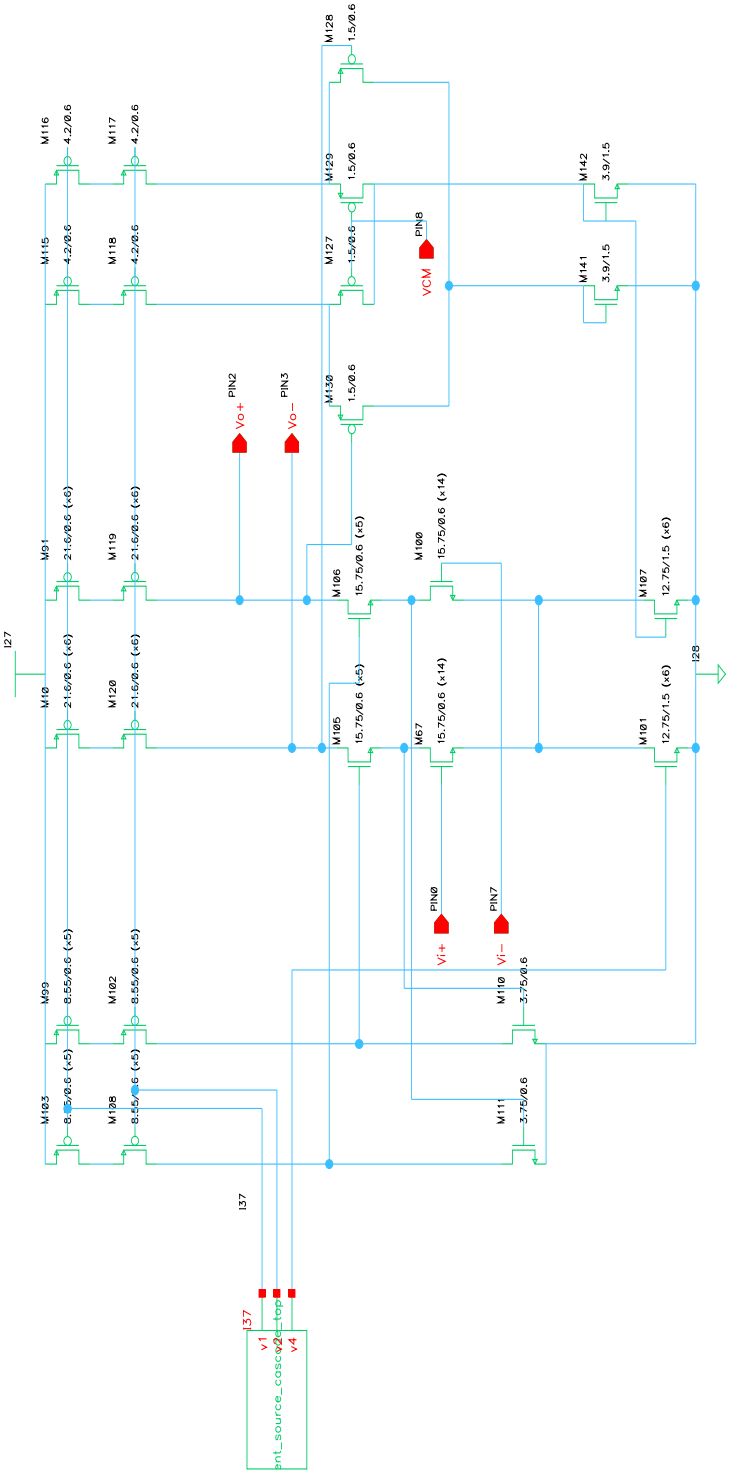

Figure A.3: Design With Wire Over Large Input Transistor

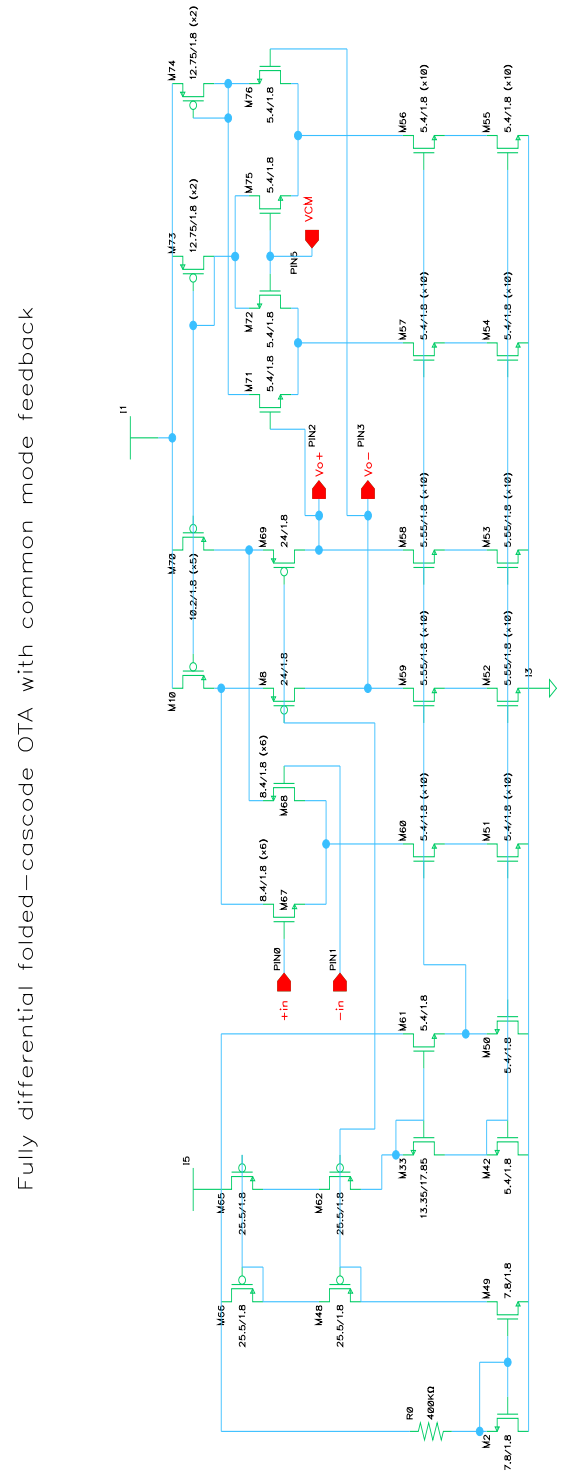

Figure A.4: Cascoded OTA Used In Previous ADC Design

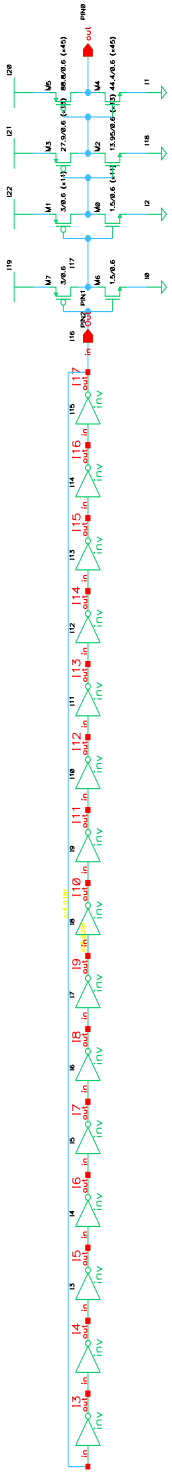

Figure A.5: 250MHz Ring Oscillator

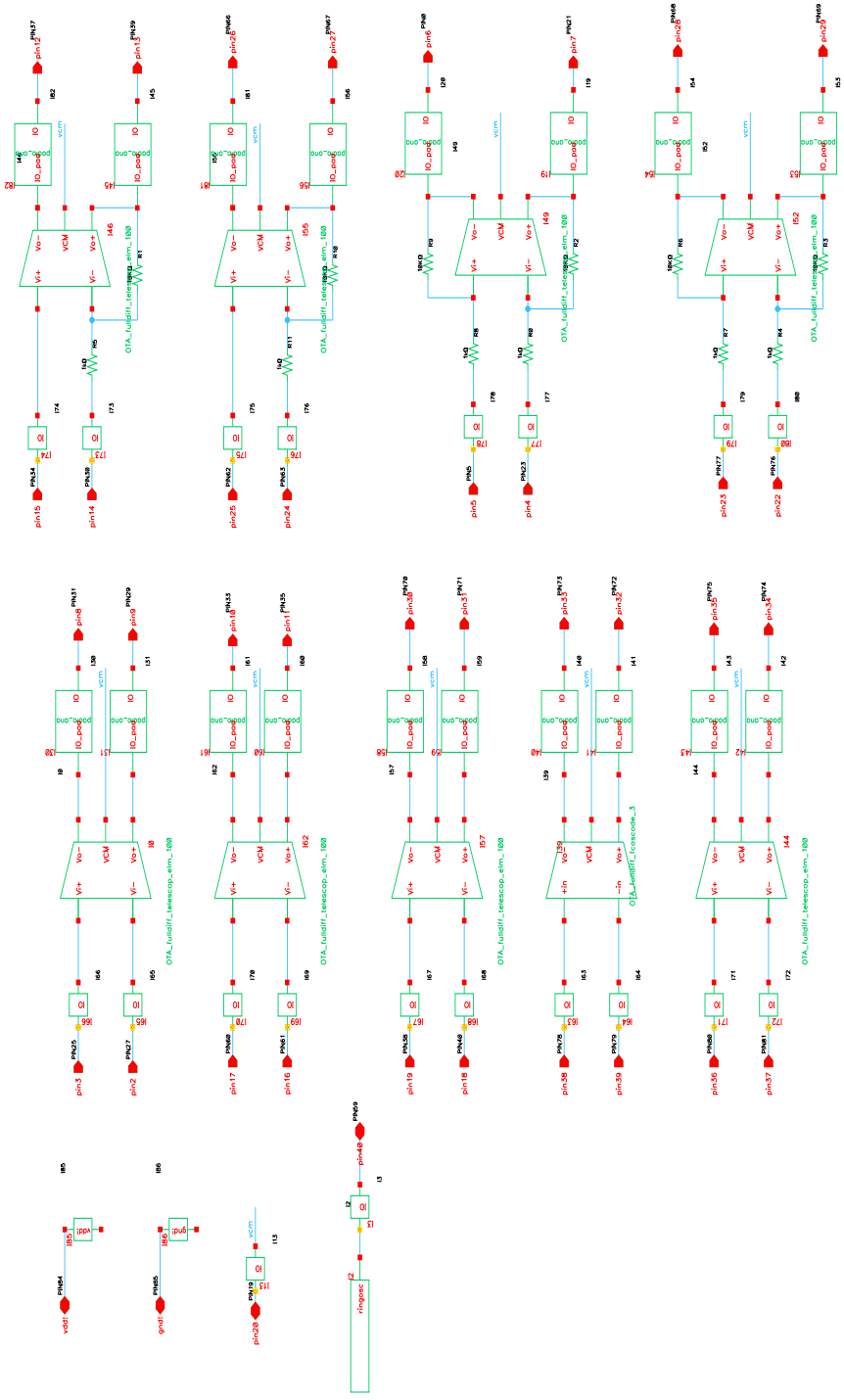

Figure A.6: Top Level Schematic

Appendix B

Physical Designs

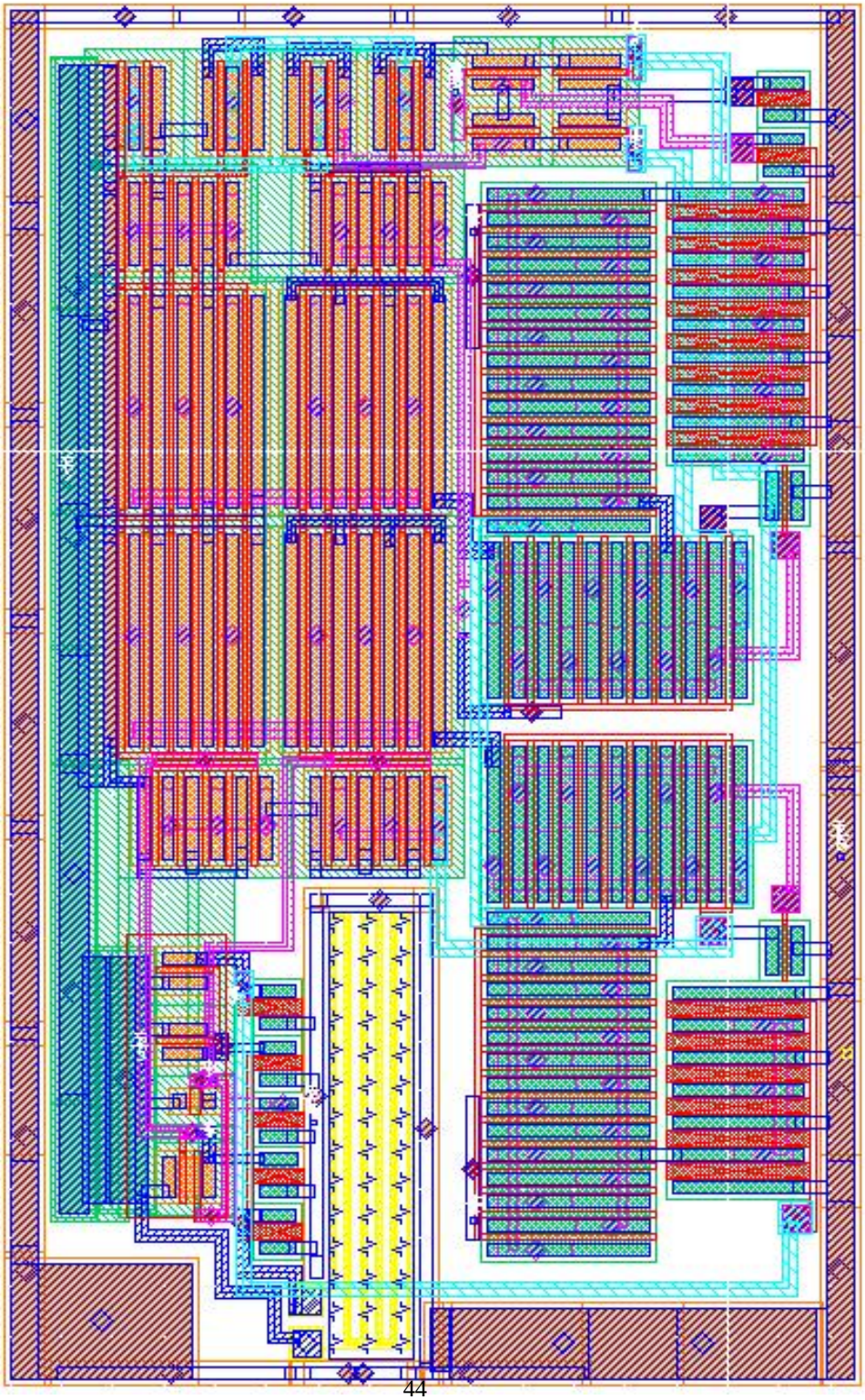

Figure B.1: Primary Layout Used In ADC (design B)

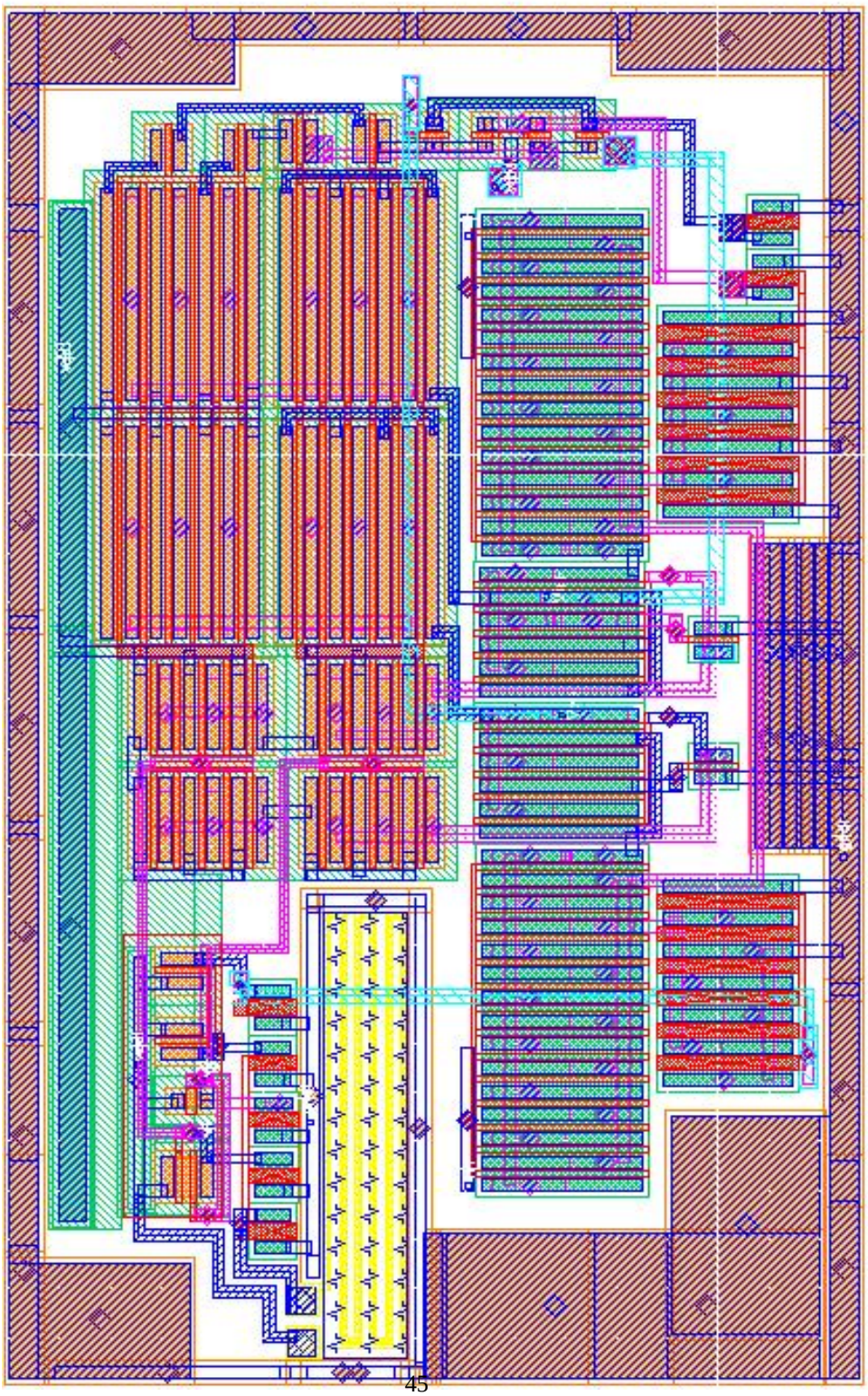

Figure B.2: Layout With Smaller CMFB Section (design A)

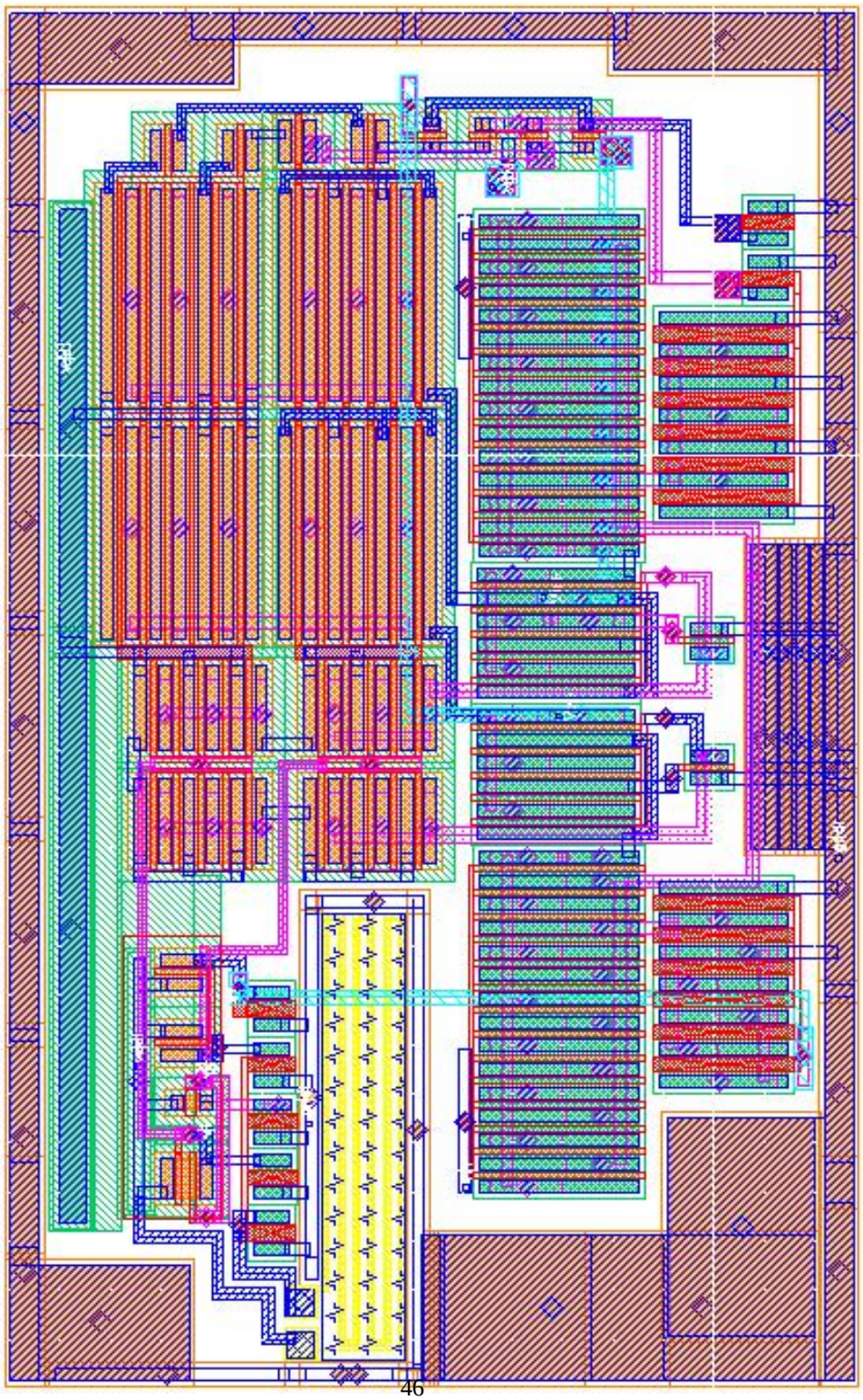

Figure B.3: Layout With Wire Over Large Input Transistor

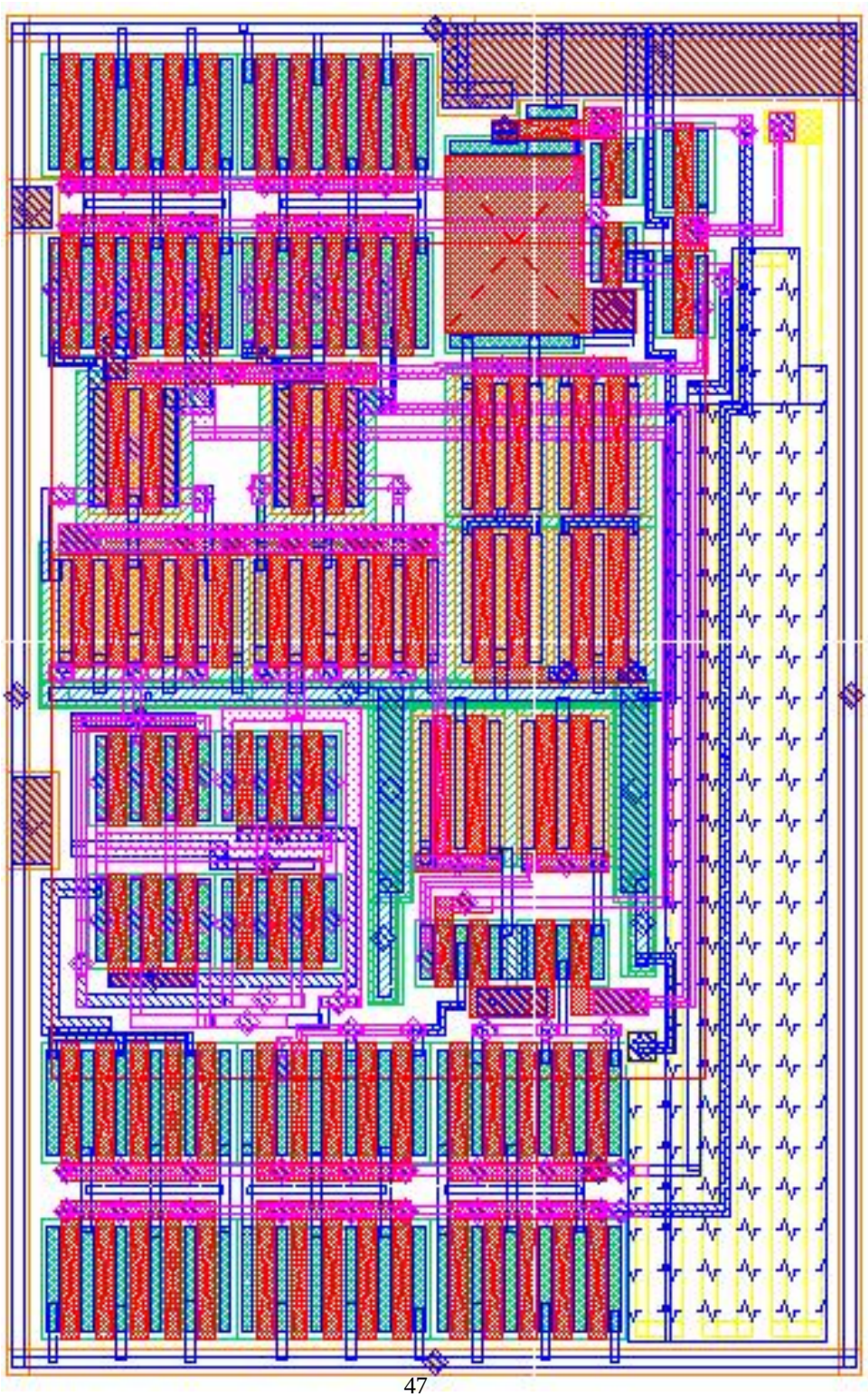

Figure B.4: Cascoded OTA Used In Previous ADC design

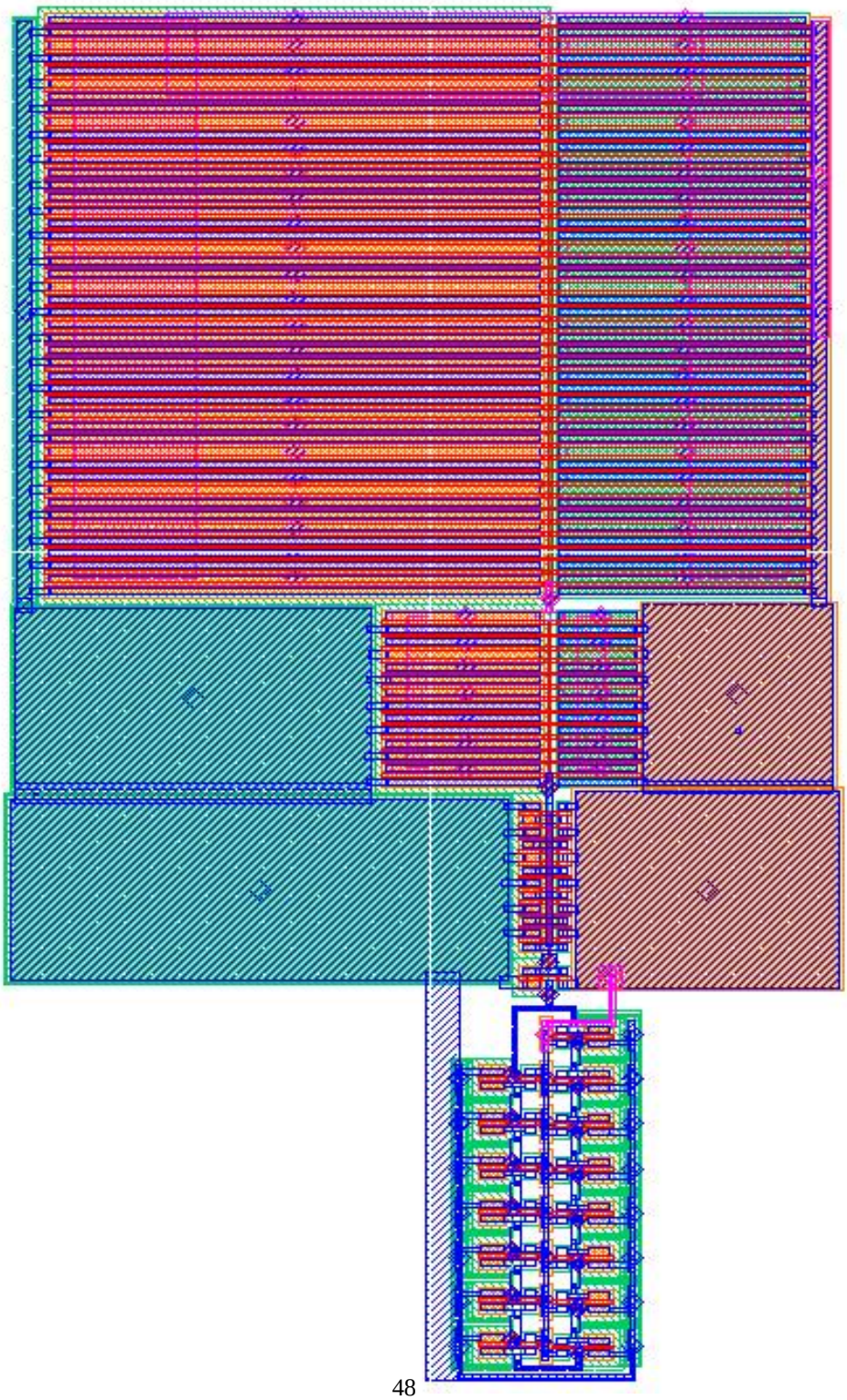

Figure B.5: 250MHz Ring Oscillator With Buffer

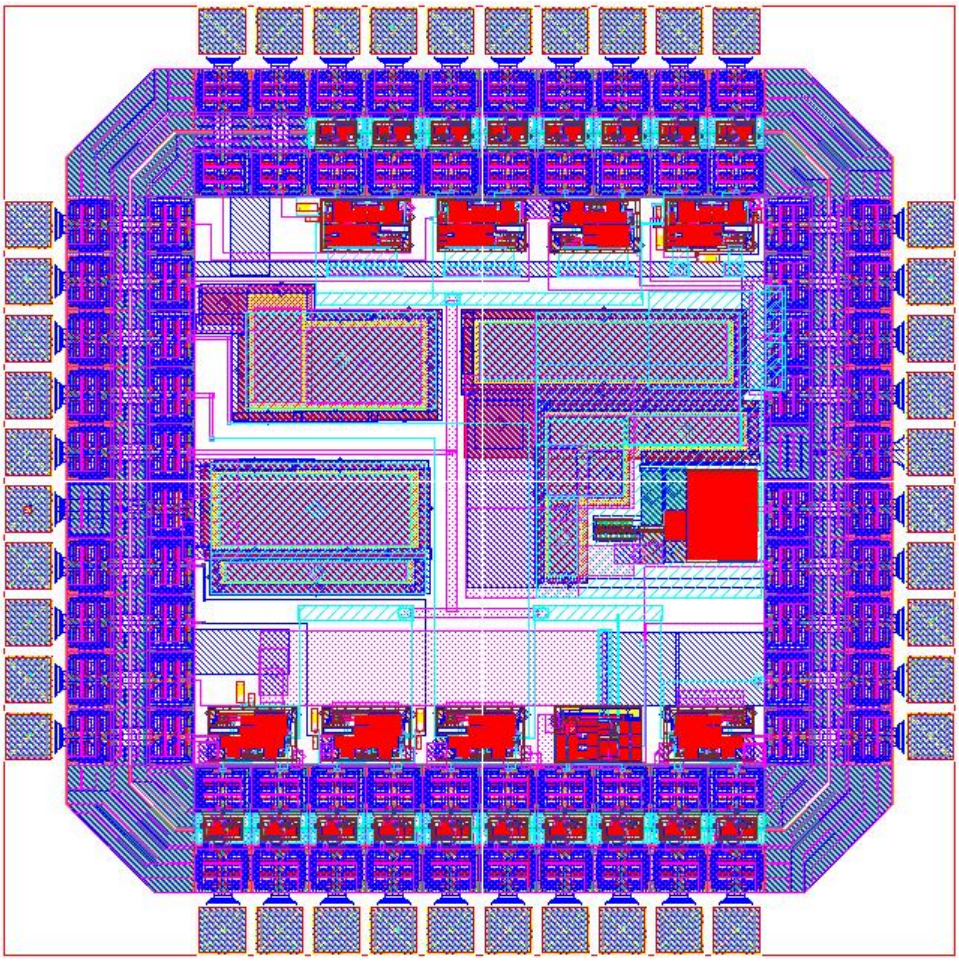

Figure B.6: Top Level Layout