

# **DESIGN OF A 120dB PSEUDO-LOGARITHMIC AMPLIFIER IMPLEMENTED IN THE AMI 0.5 $\mu$ m PROCESS**

By Zachary Richards

Advisor: Dr. David E. Kotecki

An Abstract of the Design Project  
Completed for ECE547:  
VLSI Design and Layout  
May 2007

This paper discusses several design methodologies for achieving logarithmic amplification and focuses on the design, simulation, and layout of a 120dB pseudo-logarithmic amplifier. The overall design consists of two major parts—a cascade of limiting current amplifiers and a difference amplifier. The pseudo-logarithmic amplifier accepts a single-ended current input and produces a single-ended output voltage that is linear-in-dB with the input. The circuit runs on a 5V rail, accepts input currents in the range of 1nA to 1mA, and generates an output voltage in the range of roughly 0V to 4V.

Several test structures have also been included in the overall chip layout, including a single current limiting amplifier and a two-stage operational amplifier. These structures are meant to aid in the testing and characterization of the chip, which will be completed in the fall of 2007.

# TABLE OF CONTENTS

LIST OF TABLES.....	2
LIST OF FIGURES.....	3
1. INTRODUCTION.....	4
1.1. Paper Organization.....	4
1.2. Project Goal and Specifications.....	5
2. METHODS OF LOGARITHMIC AMPLIFICATION.....	6
2.1. Non-linear Feedback.....	6
2.2. Pseudo-logarithmic Approximation.....	9
3. 120dB PSEUDO-LOGARITHMIC AMPLIFIER DESIGN.....	14
3.1. Limiter Cascade.....	14
3.2. Current Limiting Amplifier Design.....	15
3.3. Pseudo-logarithmic Amplifier Architecture.....	21
3.4. Difference Amplifier.....	21
3.5. 120dB Pseudo-logarithmic Amplifier.....	24
4. CONCLUSION.....	29
4.1. System Simulation Results.....	29
4.2. Test Procedures and Protocols.....	32
4.3. Summary and Conclusion.....	33
4.4. Recommendations for Future Work.....	34
REFERENCES.....	36
APPENDICES.....	37
BIOGRAPHY OF THE AUTHOR.....	48

## LIST OF TABLES

Table 1.1: Project Specifications.....	5
Table 2.1: Cascade Current Definitions.....	10
Table 2.2: Current Calculations for Three Stage Cascade Example.....	11
Table 3.1: Cascade Configurations for Achieving 120dB of DIR.....	14
Table 3.2: Pinout of the Completed Chip.....	27

## LIST OF FIGURES

Figure 2.1: Logarithmic Amplifier Utilizing BJT Feedback.....	6
Figure 2.2: Cascade of Current Limiting Amplifiers.....	9
Figure 2.3: Three Stage Current Limiting Cascade.....	11
Figure 3.1: MATLAB Simulation Results for Various Cascade Configurations.....	15
Figure 3.2: Current Limiting Amplifier Design.....	16
Figure 3.3: Simplified View of Current Limiting Amplifier Design.....	17
Figure 3.4: Cascade Power Consumption vs. Number of Stages for 120dB of DIR.....	19
Figure 3.5: Current Limiting Amplifier Layout.....	20
Figure 3.6: Overall Pseudo-logarithmic Amplifier Architecture.....	21
Figure 3.7: Two-Stage Operational Amplifier Schematic.....	22
Figure 3.8: Two-Stage Operational Amplifier Layout.....	23
Figure 3.9: Standard Difference Amplifier Configuration.....	23
Figure 3.10: 120dB Pseudo-logarithmic Amplifier Design.....	24
Figure 3.11: 120dB Pseudo-logarithmic Amplifier Layout.....	26
Figure 4.1: System Simulation Test Bench.....	29
Figure 4.2: Simulated Output Voltage for 120dB Pseudo-logarithmic Amplifier.....	30
Figure 4.3: Simulated Output Voltage and Ideal Linear-in-dB.....	31
Figure 4.4: Error From Ideal Linear-in-dB Output.....	32

# 1. INTRODUCTION

In many applications it is necessary to utilize signals that vary over a large dynamic range, which often becomes problematic when these signals also need to be amplified. If such a signal were to be amplified linearly, the upper end of the dynamic range could be lost through saturation in an attempt to bring the lower end to observable amplitudes. However, by amplifying the signal logarithmically, both problems are solved; the signal can be amplified and the dynamic output range will be greatly reduced. This paper will touch on several methods of achieving logarithmic amplification and focus on the design and implementation of a pseudo-logarithmic amplifier in the AMI 0.5 $\mu\text{m}$  process.

## 1.1: Paper Organization

This paper is organized in four chapters. The first chapter contains introductory information, and the second chapter explains the theory behind the two principle methods of achieving logarithmic amplification. The third chapter describes the circuit topologies and layout techniques used to realize the 120dB pseudo-logarithmic amplifier; and the fourth chapter presents simulation methodologies, the results of overall system simulation, and recommendations for future improvements.

## 1.2: Project Goal and Specifications

The goal of this project is to design and implement a logarithmic amplifier in the AMI 0.5 $\mu$ m process. In addition to traditional specifications, the process itself presents some interesting complications which will be investigated in the next chapter. The specifications and constraints, traditional and process imposed, for the project are shown in Table 1.1 below:

<b>Specification</b>	<b>Type / Constraint</b>	<b>Maximum</b>	<b>Minimum</b>
System Input	Single-ended Current	1mA	1nA
System Output	Single-ended Voltage	$\sim 5V$	$\sim 0V$
Layout Area	—	$\sim 900\mu m \times \sim 900\mu m$	—
Operational Frequency	—	10Hz	DC
Logarithmic Amplification	CMOS only	—	—

Table 1.1: Project Specifications

## 2. METHODS OF LOGARITHMIC AMPLIFICATION

There are several different methods through which logarithmic amplification can be achieved. Two such methods include feedback through a non-linear device, and approximation by summing the outputs of limiting amplifiers. These two topologies will be investigated in sections 2.1 and 2.2 respectively.

### 2.1: Non-linear Feedback

Non-linear feedback is perhaps the most common method used to achieve logarithmic amplification as it is the simplest. This approach places a non-linear device, almost always a BJT, in the feedback loop of an op-amp as illustrated in the Figure 2.1 below:

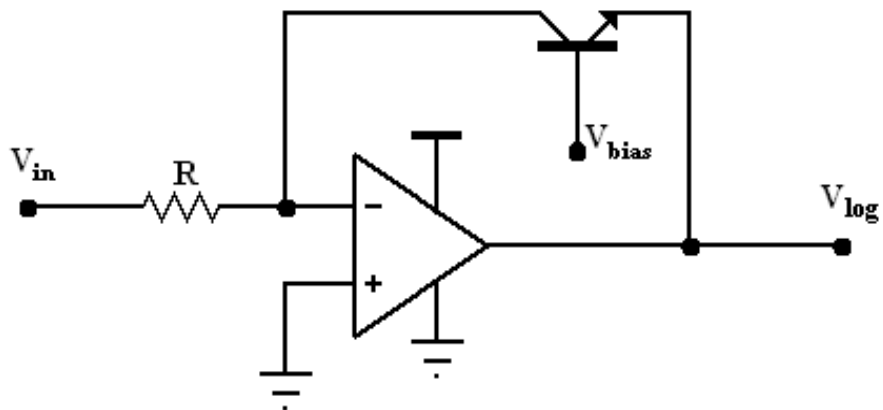


Figure 2.1: Logarithmic Amplifier Utilizing BJT Feedback

Since the circuit in Figure 2.1 contains negative feedback, the voltage at the negative terminal will be virtually shorted to the positive terminal. Applying nodal analysis at this terminal:

$$\frac{0 - V_i}{R} + I_c = 0 \quad (2.1)$$

where the collector current,  $I_c$ , is:

$$I_c = I_s \cdot \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) \quad (2.2)$$

Rearranging Equation 2.1 and substituting Equation 2.2 into it:

$$\frac{V_i}{R} = I_s \cdot \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) \approx I_s \cdot e^{\frac{V_{BE}}{V_T}} \quad (2.3)$$

Taking the natural log of both sides of Equation 2.3 and multiplying through by the thermal voltage,  $V_T$ , gives:

$$V_T \cdot \ln \left( \frac{V_i}{R \cdot I_s} \right) = V_{BE} \quad (2.4)$$

From Figure 1 the base-emitter voltage of the feedback NPN transistor is easily determined as:

$$V_{BE} = V_{bias} - V_{out} \quad (2.5)$$

which can then be substituted into Equation 2.4:

$$V_T \cdot \ln \left( \frac{V_i}{R \cdot I_s} \right) = V_{bias} - V_{out} \quad (2.6)$$



Rearranging the terms of Equation 2.6 and moving the  $RI_S$  term into its own logarithm yields:

$$V_{out} = -V_T \cdot \ln(V_i) + V_T \cdot \ln(R \cdot I_S) + V_{bias} \quad (2.7)$$

Assigning the last two terms on the right-hand side of Equation 2.7 to “b” and assigning  $-V_T$  in the first term to “m” gives:

$$V_{out} = m \cdot \ln(V_i) + b \quad (2.8)$$

which illustrates that the output voltage is clearly a linear function of the natural log of the input voltage. Hence, logarithmic amplification has been achieved.

A subthreshold MOSFET can also be used in feedback in order to realize logarithmic amplification. In this region of operation a non-linear relationship is exhibited between drain current and gate-to-source voltage:

$$I_D = I_{no} \cdot \left( e^{\frac{\kappa_n \cdot q \cdot V_{gs}}{k \cdot T}} \right) \quad (2.9)$$

so long as the following condition is met:

$$V_{ds} \geq \frac{4 \cdot k \cdot T}{q} \quad (2.10)$$

A quick comparison of Equations 2.2 and 2.9 reveals the close similarity between using BJTs and subthreshold MOSFETs in feedback. However, it is important to note that the NPN transistor in Figure 2.1 cannot simply be replaced by an NMOS transistor in order to implement a MOS logarithmic amplifier.

While non-linear feedback is an extremely effective approach in order to produce logarithmic amplification, the AMI 0.5 $\mu$ m process used for this project is unsuited for this option. The process is CMOS only and lateral PNP transistors are not supported, which means that BJT feedback is unavailable. Furthermore, in order to use MOSFET feedback it is necessary for the subthreshold region of operation to be uncommonly well modeled, which is not the case. Thus, another technique must be chosen.

## 2.2: Pseudo-logarithmic Approximation

One of the few alternatives to non-linear feedback is called pseudo-logarithmic approximation. This method develops an approximation of logarithmic behavior by summing the outputs of a cascade of limiting amplifiers. This general idea is depicted in the figure below:

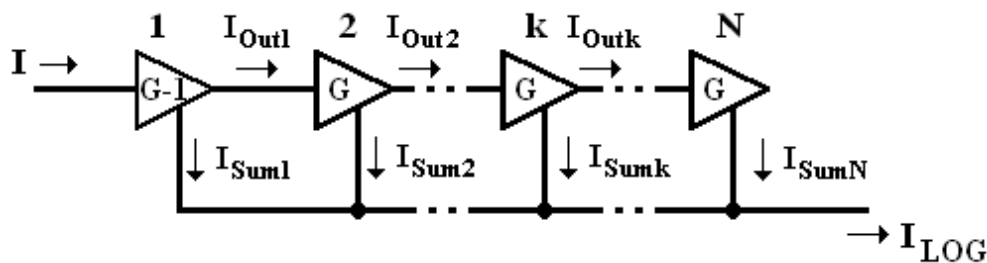


Figure 2.2: Cascade of Current Limiting Amplifiers

Figure 2.2 depicts the topology used for a cascade of current limiting amplifiers; however, voltage limiting amplifiers can be also be used to generate logarithmic behavior in a similar manner. The currents and corresponding stages shown in the cascade in Figure 2.2 are defined in the table on the following page.

Stage	$I_{\text{Out}}$	$I_{\text{Sum}}$
1	$(G-1) \cdot I$	$I$
2	$(G-1) \cdot (G) \cdot I$	$(G-1) \cdot I$
$\vdots$	$\vdots$	$\vdots$
k	$(G-1) \cdot (G)^{(k-1)} \cdot I$	$(G-1) \cdot (G)^{(k-2)} \cdot I$
$\vdots$	$\vdots$	$\vdots$
N	$(G-1) \cdot (G)^{(N-1)} \cdot I$	$(G-1) \cdot (G)^{(N-2)} \cdot I$

Table 2.1: Cascade Current Definitions

As shown in Table 2.1, the output current,  $I_{\text{Out}}$ , at any stage  $k \geq 1$  is:

$$I_{\text{Out}k} = (G-1) \cdot (G)^{(k-1)} \cdot I \quad (2.11)$$

Furthermore, the summing current,  $I_{\text{Sum}}$ , at any stage  $k \geq 2$  (for  $k = 1$ ,  $I_{\text{Sum}} = I$ ) is:

$$I_{\text{Sum}k} = (G-1) \cdot (G)^{(k-2)} \cdot I \quad (2.12)$$

The most important feature of these amplifiers is that they are *limiting*. That is, there is a set value of current that cannot be exceeded by  $I_{\text{Out}}$  or  $I_{\text{Sum}}$  no matter how great the input current is. This property is utilized in conjunction with the gain configuration of the cascade in order to produce logarithmic behavior. This is illustrated in the following example in which a three stage cascade, shown in Figure 2.3 on the next page, is investigated.

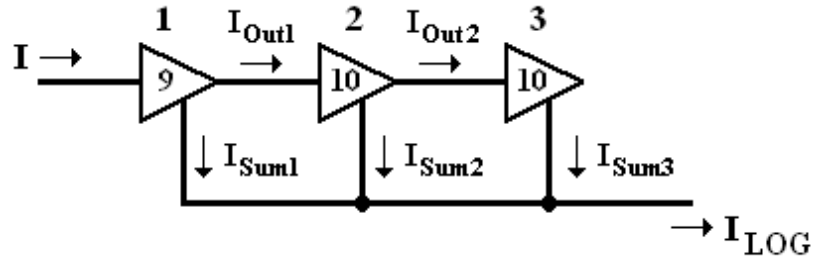


Figure 2.3: Three Stage Current Limiting Cascade

As shown in Figure 2.3, the gain,  $G$ , of the general case cascade has been set to 10. Assuming a limiting current,  $I_{BIAS}$ , of 1mA and an input current that will range over several orders of magnitude the summing currents for each stage and the output current,  $I_{LOG}$ , will be calculated in the following table. The summing currents will be calculated using Equation 2.2 and the output current will be calculated by summing all  $I_{Sum}$  terms.

$I$ (mA)	$I_{Sum1}$ (mA)	$I_{Sum2}$ (mA)	$I_{Sum3}$ (mA)	$I_{LOG}$ (mA)
10	1	1	1	3
1	1	1	1	3
0.1	0.1	0.9	1	2
0.01	0.01	0.09	0.9	1
0.001	0.001	0.009	0.09	0.1

Table 2.2: Current Calculations for Three Stage Cascade Example

As shown in Table 2.2, the output current of the cascade clearly exhibits a linear relationship for the input current range of 0.01mA to 1mA. Thus, the topology has successfully demonstrated its

ability to generate the desired logarithmic characteristic. Notice that for the input current of 10mA, the cascade output characteristic has ceased to follow the linear relationship apparent in the input range of 0.01mA to 1mA. This is due to the fact that it has already limited completely, and thus the output current will always remain constant after the input reaches 1mA. This illustrates the upper bound of the acceptable input range:

$$R_{input}(max) = I_{bias} \quad (2.13)$$

Furthermore, at the input current of 0.001mA the output current has also ceased to be linear. This is because the input current has dropped below the range of the gain provided by the cascade. That is, the overall gain of the cascade,  $G_{cascade}$  (defined below), along with the limiting current, set the lower bound of the input range.

$$G_{cascade} = (G - 1) \cdot (G)^{(N-1)} \quad (2.14)$$

$$R_{input}(min) = \frac{I_{bias}}{G_{cascade}} \quad (2.15)$$

In the three stage example above the total gain of the cascade is 900. Plugging this value into Equation 2.15 gives:  $R_{input}(min) = 0.001111\text{mA}$ , which is greater than 0.001mA, the fifth and final value of input current from Table 2.2. Thus, from equations 2.13 and 2.15 an equation can be written to describe the acceptable dynamic input range, DIR, of the overall cascade:

$$DIR = \frac{I_{bias}}{G_{cascade}} \rightarrow I_{bias} \quad (2.16)$$

Thus, pseudo-logarithmic approximation can be used to realize a logarithmic amplifier so long as

the input range stays within the limits defined in Equation 2.16. However, it is important to remember that this is an *approximation* and there will be some deviation from an ideal linear-in-dB output yielded by this method. This deviation inevitably becomes a design constraint and will be explored in detail in section 3.1.

### 3. 120dB PSEUDO-LOGARITHMIC AMPLIFIER DESIGN

For the reasons outlined in chapter 2, the method of pseudo-logarithmic approximation will be used to realize the logarithmic amplifier. This leads to several important considerations regarding the limiter cascade; the two most prominent of which are the number of stages to be used, and the topology of the individual limiting amplifiers. These issues will be explored in sections 3.1 and 3.2 respectively.

#### 3.1: Limiter Cascade

The following table illustrates possible combinations of gain,  $G$ , and number of limiting stages,  $N$ , that can be utilized to meet the desired dynamic input range, DIR, of 120dB:

<b>N</b>	<b>G</b>	<b>Resultant DIR (dB)</b>
3	102	120.4304
5	16.2	120.3981
7	7.4	120.4314
10	4.1	120.1283
13	3	120.5297

Table 3.1: Cascade Configurations for Achieving 120dB of DIR

These various system configurations were simulated with MATLAB (see Appendices A1 and A2). A bias current of 1mA and an input current range of 1nA to 1mA was assumed for the simulation, and the results are displayed in Figure 3.1 on the next page.

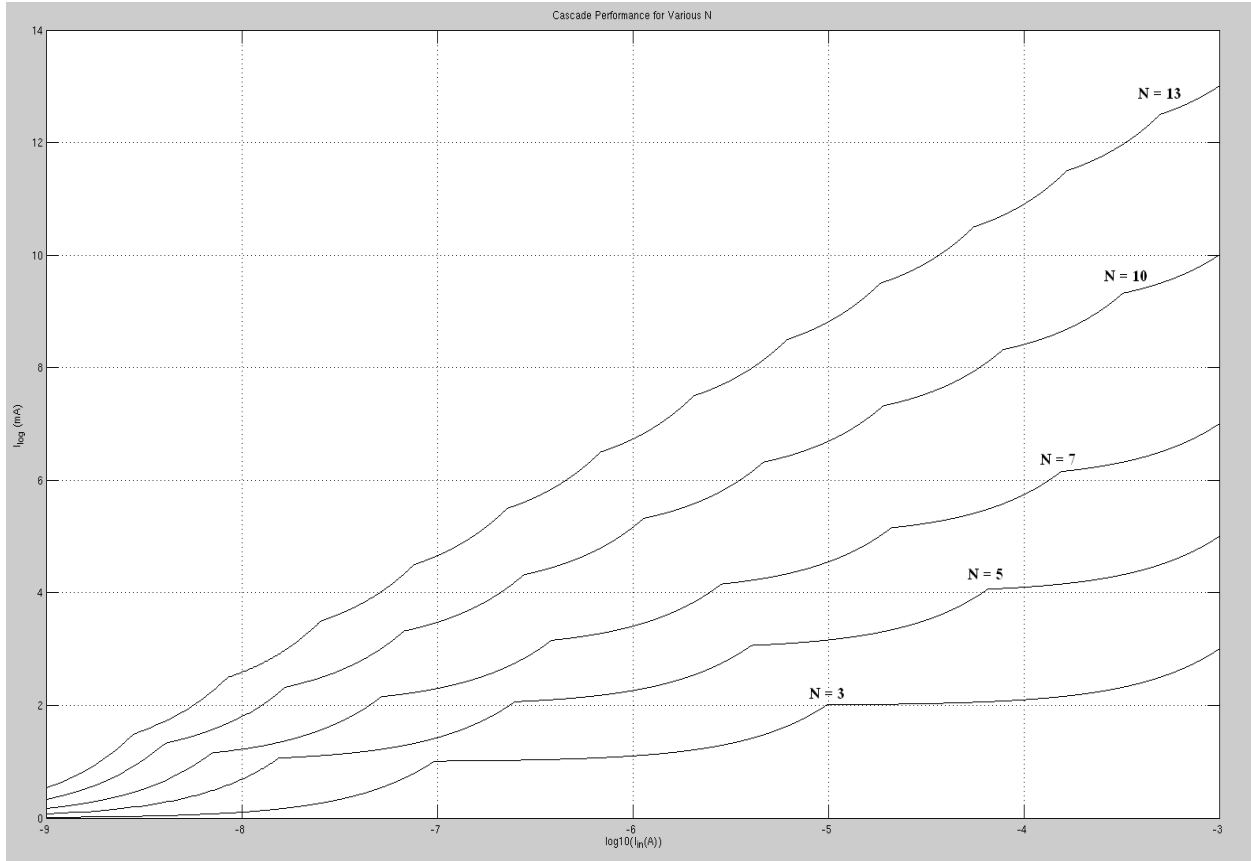


Figure 3.1: MATLAB Simulation Results for Various Cascade Configurations

From the results above it is clear that as the number of stages increases for any fixed DIR that there will be a corresponding decrease in deviation from ideal linear-in-dB behavior. For this reason, and several others that will be explored in the next section, the cascade configuration using 13 stages and a gain of 3 is optimal.

### 3.2: Current Limiting Amplifier Design

The design of the current limiting amplifier was taken from an article appearing in the



IEEE 1997 Custom Integrated Circuits Conference, which utilizes a single input configuration that achieves the desired gain,  $G$ , by sizing the output devices with aspect ratios that are a factor of  $G$  greater than that of the input devices [1]:

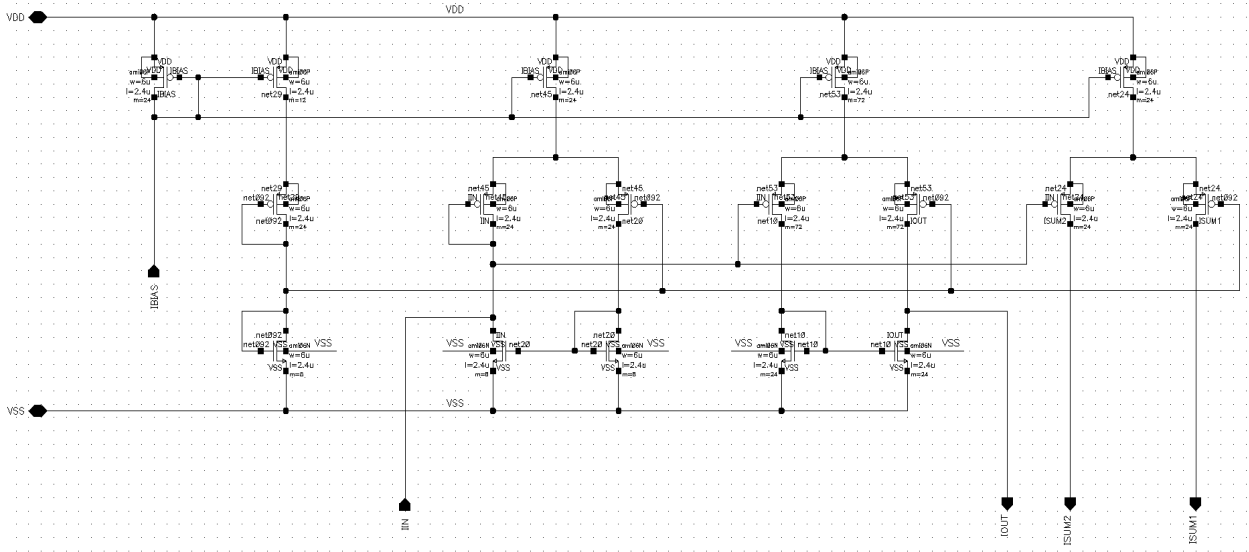


Figure 3.2: Current Limiting Amplifier Design

The article that this design was taken from does not contain a description of the functionality of the circuit, so one has been provided in Appendix A3. For the sake of both simplicity and clarity, the schematic in Figure 3.2 has been redrawn as shown in Figure 3.3 on the next page.

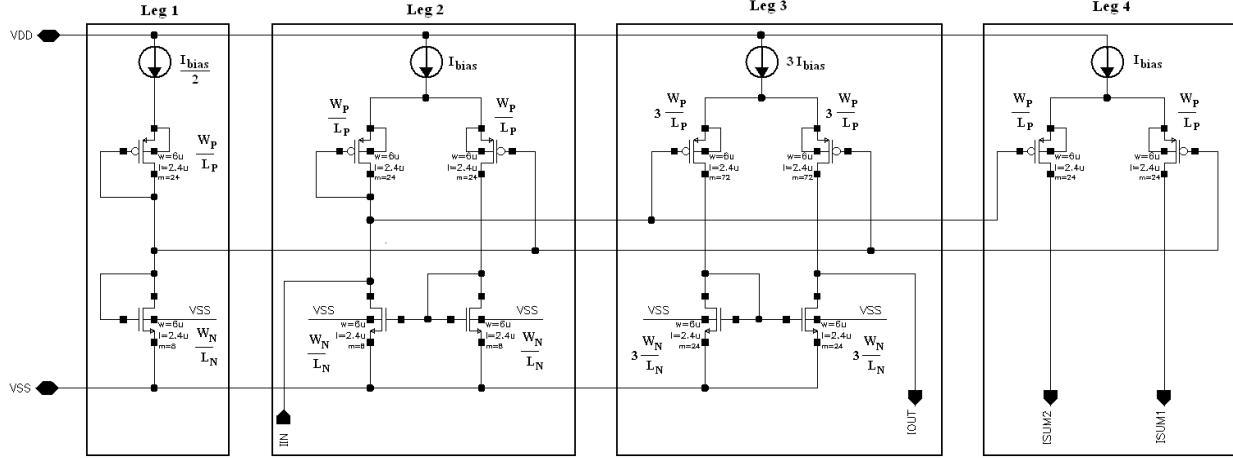


Figure 3.3: Simplified View of Current Limiting Amplifier Design

Figure 3.3 illustrates the various sections of the limiting amplifier, where Leg 1 is a bias block, Leg 2 is the single-ended input block, Leg 3 is the single-ended output block, and Leg 4 is the output summation block. Also, the aspect ratios of the devices in the output block can now be seen clearly as three times larger than those of the input block. Because this design topology is to be used, the cascade configuration using 13 stages is ideal in that the gain is set by aspect ratio multiplication; that is, this configuration allows for an integer multiplier. However, this is not the only reason that the 13-stage configuration is a good choice.

The differences in the combinations shown in Table 3.1 do not stop at stage number and gain; in fact, they also differ greatly in both power consumption and area. Notice that the total current in the circuit in Figure 3.3 will be:

$$I_{TOT} = \frac{I_{bias}}{2} + I_{bias} + 3I_{bias} + I_{bias} = 5.5I_{bias} \quad (3.1)$$

It is important to note that Equation 3.1 neglects the diode connected PMOS device which

mirrors  $I_{bias}$  to the four legs of the amplifier (the device can be seen in Figure 3.2, however). Furthermore, as there are 13 stages, the total current in the entire cascade will be nearly 13 times greater than this—it will be under 13 times greater due to the fact that the first stage will use less current as its gain is  $G-1$ ; or, in this case, 2. Considering the general case with gain and number of stages,  $G$  and  $N$ , and also taking into account the diode connected devices of each stage, Equation 3.1 can be rewritten to find the total cascade current:

$$I_{CASCADE} = ((G-1) + 3.5)I_{bias} + (N-1)(G+3.5)I_{bias} \quad (3.2)$$

Equation 3.2, the typical rail voltage for the AMI 0.5 $\mu$ m process (5V), and the  $G$  and  $N$  combinations shown in Table 3.1 were simulated with MATLAB (see Appendix A3) to calculate the power consumption of each configuration. The plot generated by this simulation is shown in Figure 3.4 on the next page.

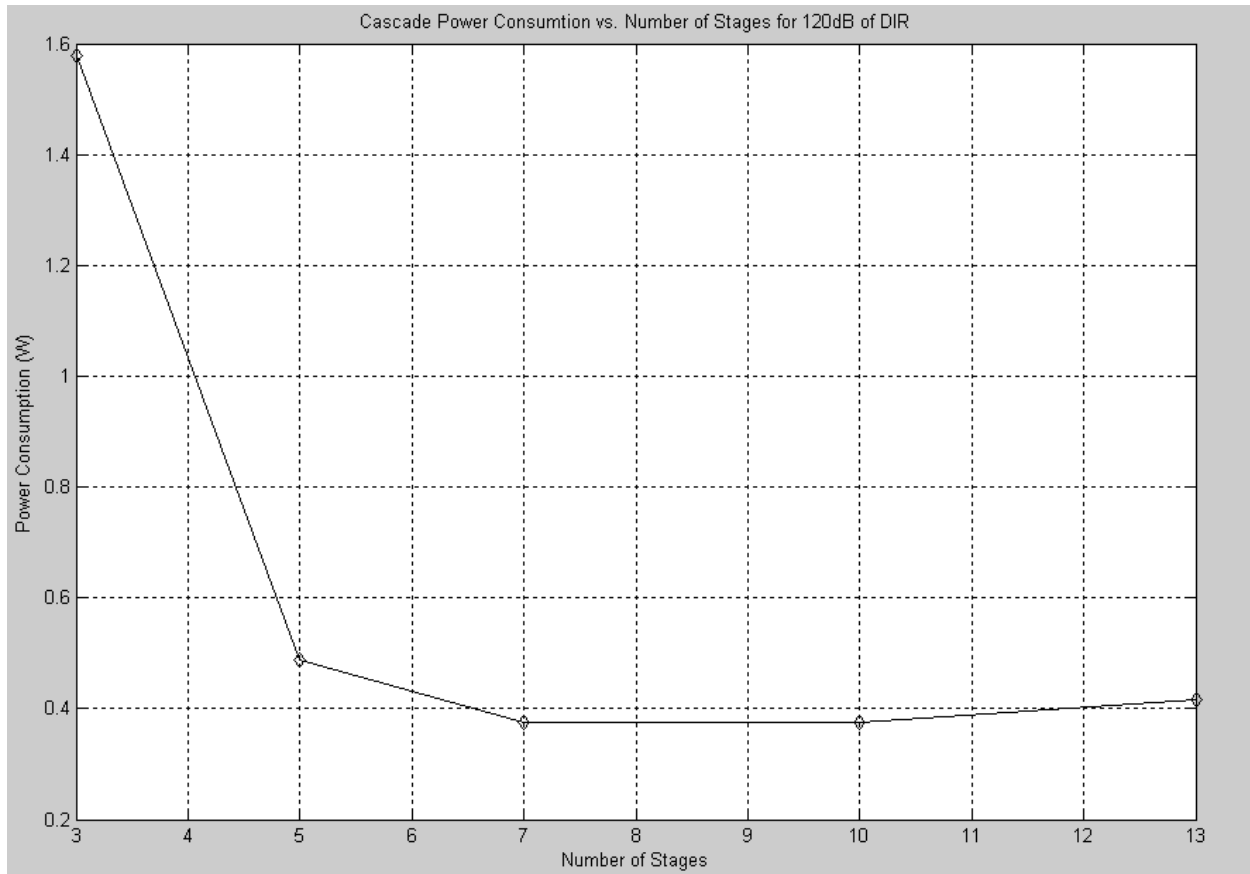


Figure 3.4: Cascade Power Consumption vs. Number of Stages for 120dB of DIR

Figure 3.4 illustrates a prominent decrease in power consumption as the number of stages increases. The power consumption does begin increasing again, only slightly though, and thus the 13-stage configuration with its integer multiplier is still the ideal choice.

The layout of the limiting amplifier is extremely important as the limiter cascade is the largest piece of the overall pseudo-logarithmic amplifier, which will be discussed further in the next section. The tightest possible layout is therefore necessary, and selecting the cascade configuration using 13 stages will help greatly; again, since the topology of this amplifier is reliant upon a multiplier of aspect ratios, the layout area will follow a similar pattern to the one

shown in Figure 3.4. Due to the fact that  $I_{\text{bias}}$  will be set at 1mA, electromigration becomes an important layout consideration as well, particularly in regards to the summing currents which can get as large as 13mA. The final layout of the current limiting is shown below:

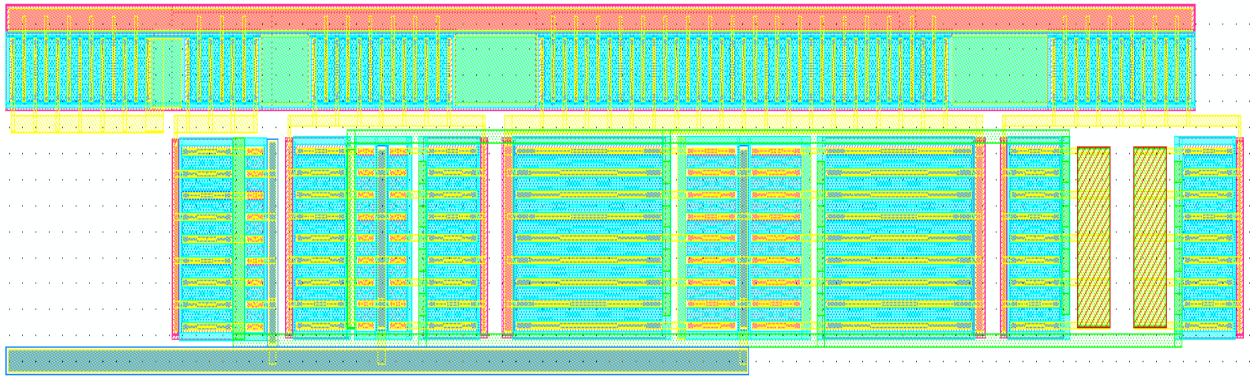


Figure 3.5: Current Limiting Amplifier Layout

The width of the summing current trances was minimized by using all three of the available metal layers and maximizing the interconnect area between them. Notice that the layout above is very similar to the sectioned view of the limiting amplifier shown in Figure 3.3. By folding the devices below the PMOS current mirrors in on themselves the overall rectangular shape was achieved, which has two advantages in the layout of the cascade. First, the vdd! and gnd! connections to their respective wells can be overlapped by vertically inverting every other amplifier stage, which will save area and simplify connecting these two rail voltages to their respective pins. The second advantage is that this limits the number of necessary corners in the traces for the summing currents, which will also help with electromigration concerns. The final dimensions of the current limiting amplifier layout are  $71.25\mu\text{m}$  by  $464.1\mu\text{m}$ . This provided for a cascade layout having dimensions of  $888.15\mu\text{m}$  by  $515.4\mu\text{m}$ , which fits snugly within the roughly  $900\mu\text{m}$  by  $900\mu\text{m}$  inner area of the standard bondpad ring.

### 3.3: Pseudo-logarithmic Amplifier Architecture

As mentioned in the previous section, the cascade of limiting amplifiers is the dominate feature of the overall system. In fact, the only other necessary structure is an operational amplifier that is configured as a difference amplifier, the design and layout of which will be discussed in the next section. Thus, the overall system has the following architecture:

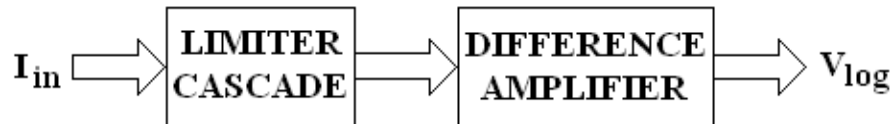


Figure 3.6: Overall Pseudo-logarithmic Amplifier Architecture

The inputs for the difference amplifier are the voltages developed across two  $200\Omega$  resistors by the output summing currents. The difference amplifier actually serves two purposes; it allows the summing outputs to be subtracted from one another, and produces a single-ended voltage output as specified in Table 1.1.

### 3.4: Difference Amplifier

Since the scope of this design project requires only that the output drive an oscilloscope load, there is no need for an extravagant design for the opamp used to implement the difference amplifier; in fact, it would be a waste of space and power to do so. Therefore, a basic two-stage opamp (such as that discussed by Gray et al. in [2]) is sufficient, the schematic of which is shown in Figure 3.7 on the next page.

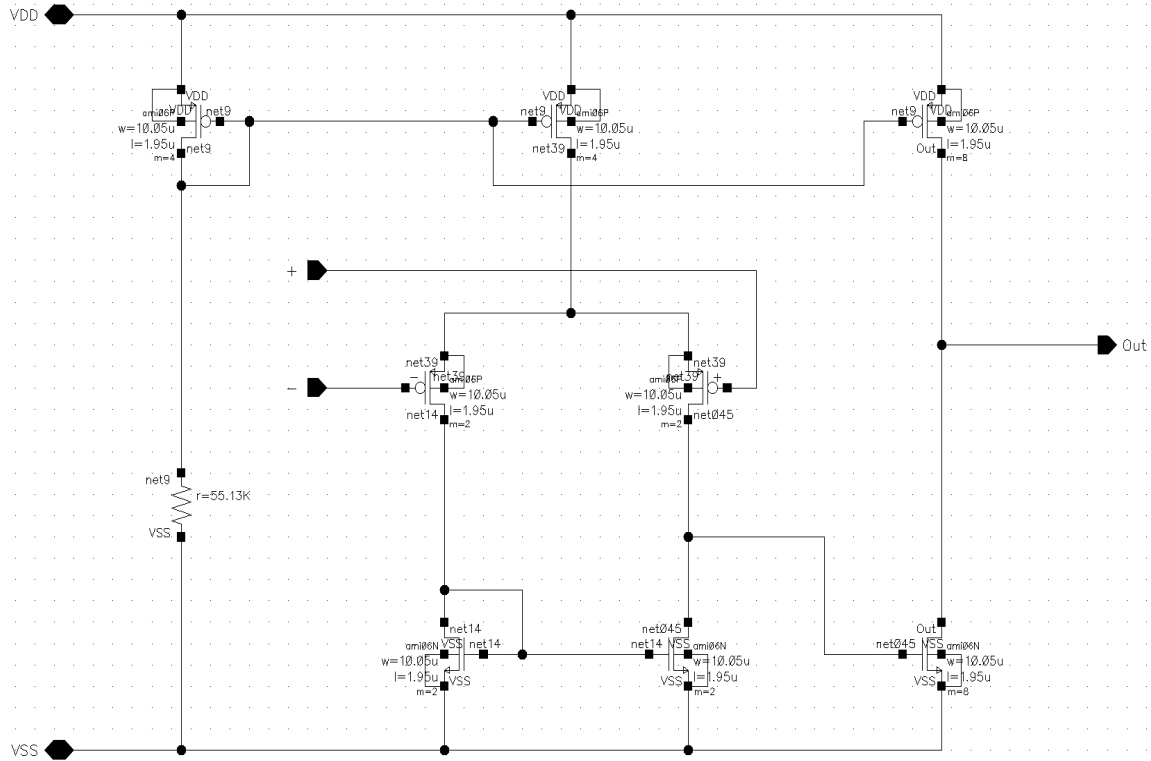


Figure 3.7: Two-Stage Operational Amplifier Schematic

Again, since it is not necessary for the operational amplifier to be overly elaborate, the circuit in the figure above was sized empirically by simulation in order to assure sufficient stability and gain to make the difference amplifier functional. The design above was finalized with a flatband gain of 85.95dB, a gain margin of 19.41dB, and a phase margin of 49.52 degrees. Due to the high degree of phase margin it was unnecessary to add any capacitive compensation. The bandwidth of the opamp is essentially of no concern since the overall system will be operating at or around DC, and the power consumption is negligible compared to that of the limiter cascade.

The layout of the two-stage opamp was quite straightforward and is shown in Figure 3.8 on the next page.

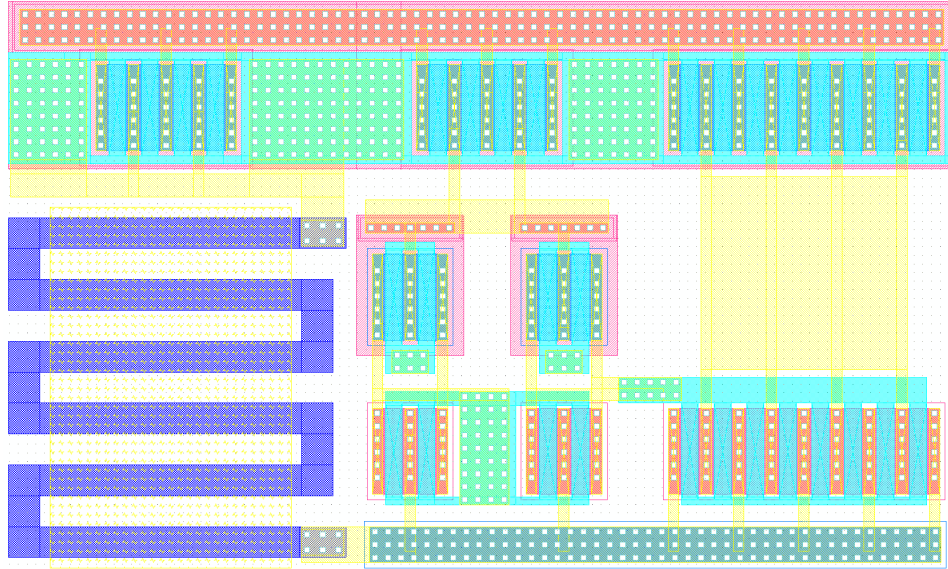


Figure 3.8: Two-Stage Operational Amplifier Layout

The layout shown above was made as compact as possible having final dimensions of  $66\mu\text{m}$  by  $108.9\mu\text{m}$ ; however, this was not entirely necessary as the limiter cascade layout left plenty of available area within the bondpad ring for additional structures.

The two-stage amplifier described above was then connected in the standard difference amplifier configuration as shown in Figure 3.9 below:

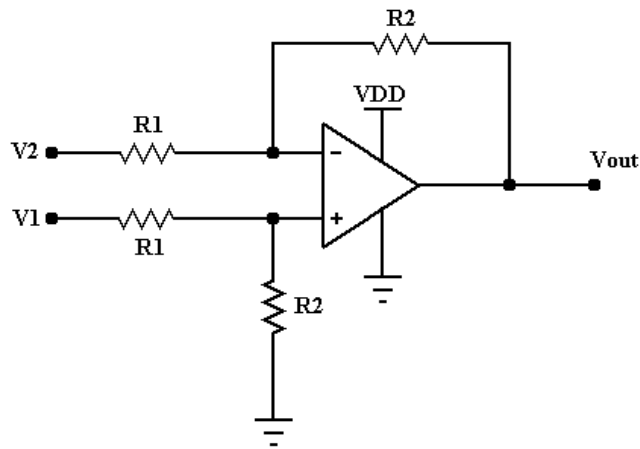


Figure 3.9: Standard Difference Amplifier Configuration



which, of course, exhibits the following behavior:

$$V_{out} = \frac{R_2}{R_1} (V_1 - V_2) \quad (3.3)$$

Thus, the difference of the summation outputs of the limiter cascade can now be taken.  $R_2$  and  $R_1$  were sized to be relatively large at  $75k\Omega$  and  $50k\Omega$ , respectively, in order to avoid limiting the drive capability of the opamp. Furthermore, sizing  $R_2$  greater than  $R_1$  allows the difference signal to be amplified, thereby utilizing an optimum portion (determined empirically) of the output swing of the opamp and increasing the resolution of the overall system.

### 3.5: 120dB Pseudo-logarithmic Amplifier

Having now discussed all of the individual blocks of the overall system, the final design of the 120dB pseudo-logarithmic amplifier is shown in Figure 3.10 below:

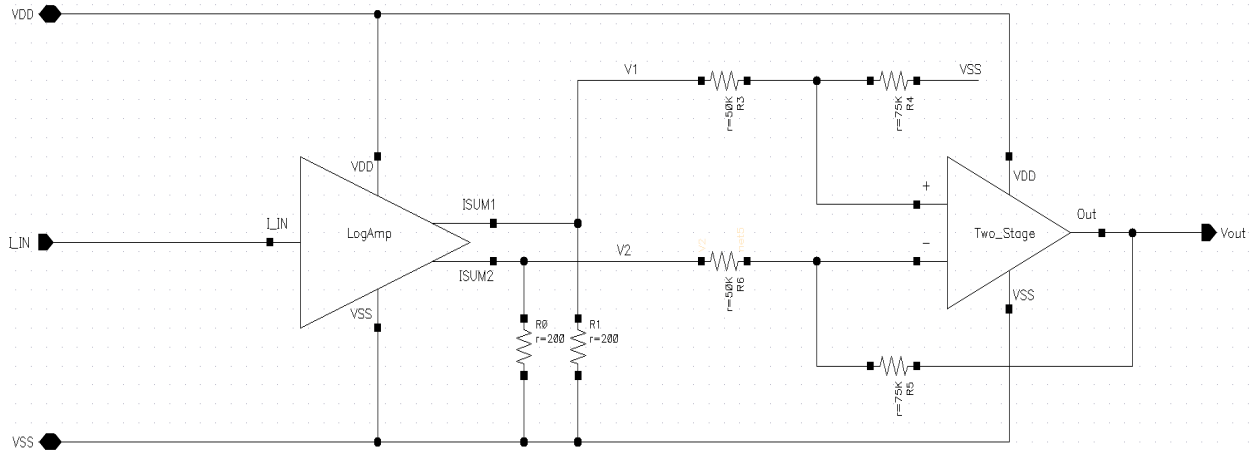


Figure 3.10: 120dB Pseudo-logarithmic Amplifier Design

where the “LogAmp” cell is the cascade of limiting amplifiers and the corresponding simple

NMOS current mirror network that sets  $I_{\text{bias}}$  and delivers it to the diode connected PMOS devices within the cascade.

The layout of the 120dB pseudo-logarithmic amplifier follows from the schematic in Figure 3.10 and the layouts discussed in the previous sections of this chapter. The only difference is the inclusion of several test structures because of the abundant extra space. The layout of the completed chip, including the standard bondpad structure is shown in Figure 3.11 on the following page.

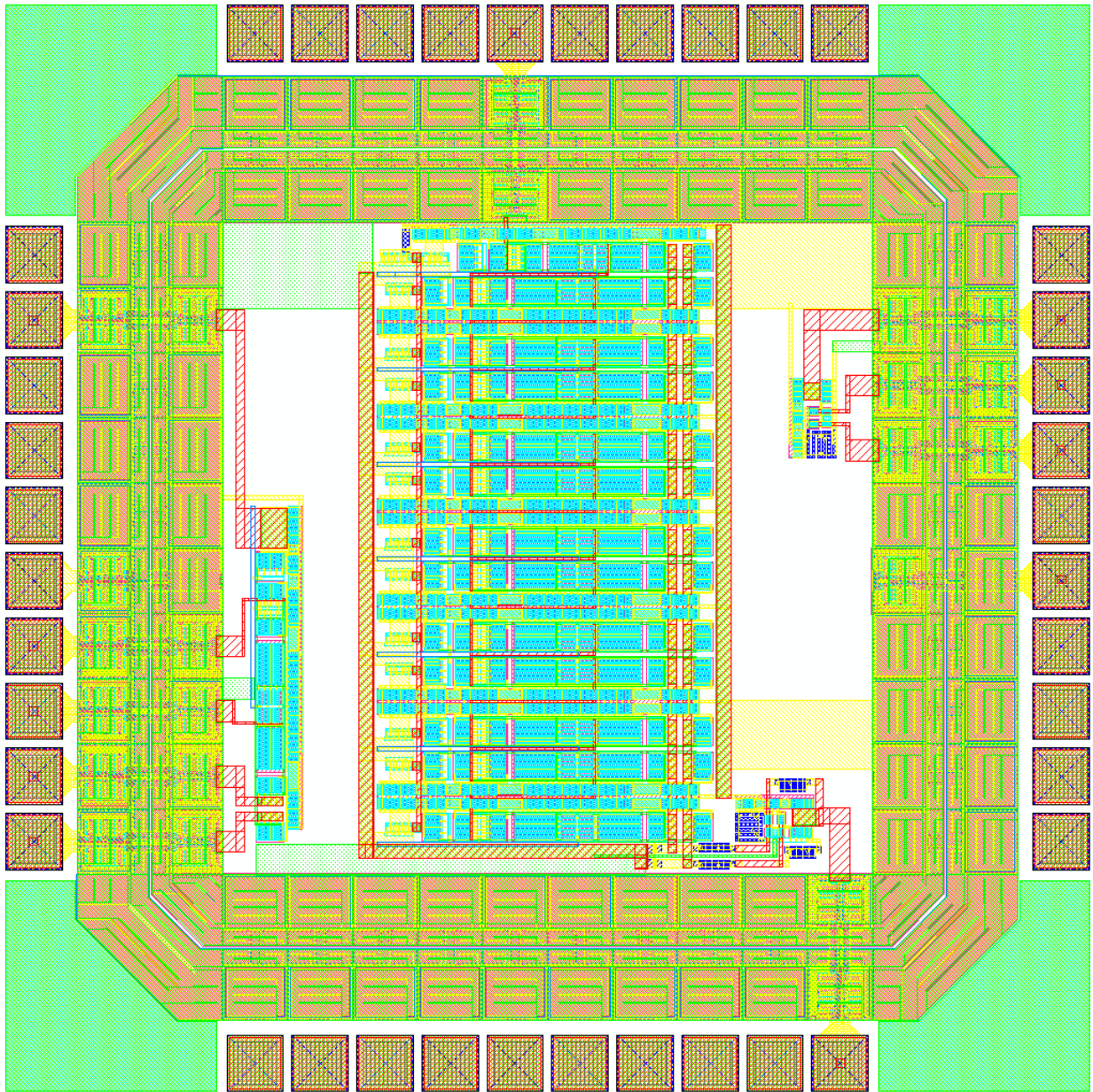


Figure 3.11: 120dB Pseudo-logarithmic Amplifier Layout

In the figure above, the central layout is the cascade of limiting amplifiers which connects to the difference amplifier in the bottom right corner. Also, there are two test structures, a single current limiting amplifier to the left of the cascade and a two-stage opamp in the upper right

corner. The top-level chip layout shown in Figure 3.11 has been verified by the design rule check (DRC) and layout versus schematic (LVS) tools both before and after the stream out process. Input and output pins were selected according to package specifications for lowest parasitics available, and the pins for the rail voltages were selected for the highest parasitic capacitance. The final pinout is displayed in Table 3.2 below; underlined rows are directly involved with the 120dB pseudo-logarithmic amplifier, all others correspond to test structures or “no connect” blocks:

<b>Pin Number</b>	<b>Pin Name</b>	<b>Corresponding Structure</b>	<b>Pin Function</b>
1	N/A	None	NC
2	N/A	None	NC
3	N/A	None	NC
4	LimBias	Current Limiting Amplifier Test Structure	$I_{bias}$ current input
5	N/A	None	NC
6	N/A	None	NC
7	N/A	None	NC
8	N/A	None	NC
9	N/A	None	NC
<u>10</u>	<u>I_IN</u>	<u>120dB Pseudo-logarithmic Amplifier</u>	<u>Single-ended current input of this design project</u>
11	N/A	None	NC
12	N/A	None	NC
13	N/A	None	NC
14	N/A	None	NC
15	N/A	None	NC
16	N/A	None	NC
17	OpOut	Two-Stage Opamp Test Structure	Voltage output of opamp
18	Op+	Two-Stage Opamp	Positive terminal input voltage

		Test Structure	of opamp
19	Op-	Two-Stage Opamp Test Structure	Negative terminal input voltage of opamp
20	N/A	None	NC
<u>21</u>	<u>vdd!</u>	<u>ALL</u>	<u>Chip rail voltage</u>
22	N/A	None	NC
23	N/A	None	NC
24	N/A	None	NC
25	N/A	None	NC
<u>26</u>	<u>Vout</u>	<u>120dB Pseudo-logarithmic Amplifier</u>	<u>Single-ended voltage output of this design project</u>
27	N/A	None	NC
28	N/A	None	NC
29	N/A	None	NC
30	N/A	None	NC
31	N/A	None	NC
32	N/A	None	NC
33	N/A	None	NC
34	N/A	None	NC
35	N/A	None	NC
36	LimSum1	Current Limiting Amplifier Test Structure	Summing current output 1
37	LimSum2	Current Limiting Amplifier Test Structure	Summing current output 2
38	LimIout	Current Limiting Amplifier Test Structure	Amplified current output
39	LimIin	Current Limiting Amplifier Test Structure	
<u>40</u>	<u>gnd!</u>	<u>ALL</u>	<u>Chip ground reference</u>

Table 3.2: Pinout of the Completed Chip

## 4. CONCLUSION

Having discussed the theory behind pseudo-logarithmic approximation and detailing its design and implementation, the methodologies for simulating and characterizing the pseudo-logarithmic amplifier created for this design project must now be addressed.

### 4.1: System Simulation Results

In order to check the functionality of the pseudo-logarithmic amplifier, a DC sweeping simulation was performed on the test bench shown in Figure 4.1 below:

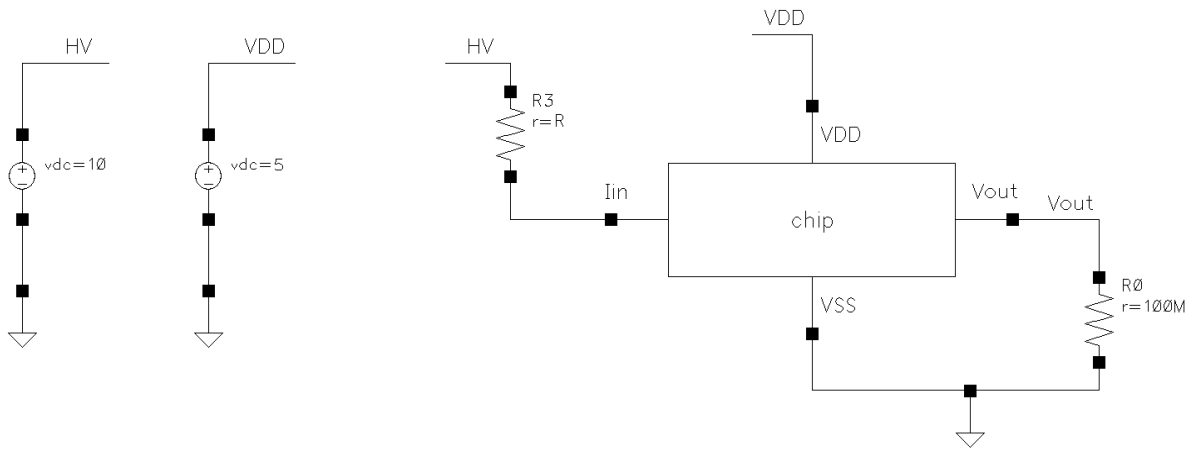


Figure 4.1: System Simulation Test Bench

In this simulation, the resistor connected between the high voltage, HV, rail and the single-ended current input, I\_IN, is swept logarithmically between  $1\text{k}\Omega$  and  $10\text{G}\Omega$ . This effectively generates input currents greater than  $1\text{mA}$  and less than  $1\text{nA}$ , which represents the  $120\text{dB}$  of specified dynamic input range. A DC current source could also have been used to do this; however, the

resistor method avoids the complications that often accompany simulating with ideal current sources. The results of the simulation are displayed in Figure 4.2 below:

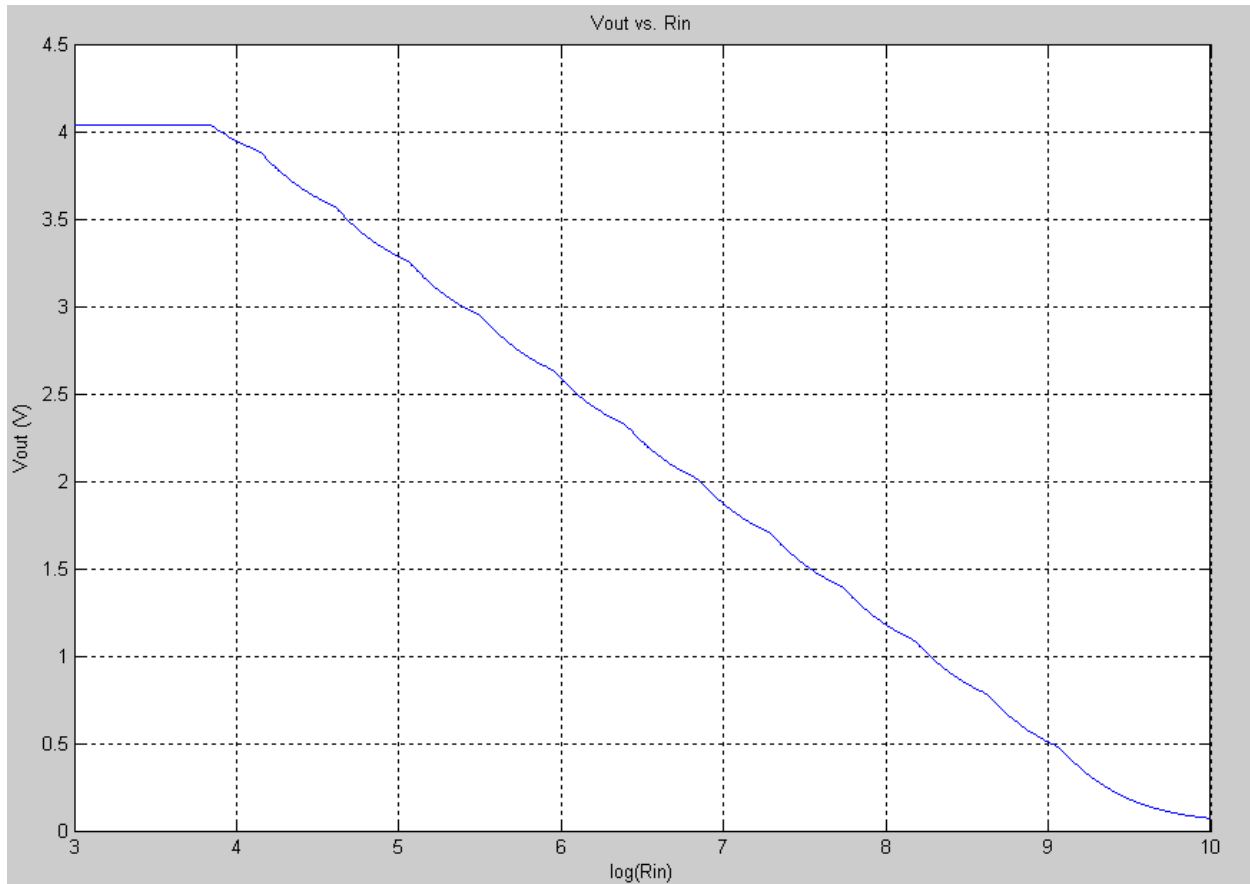


Figure 4.2: Simulated Output Voltage for 120dB Pseudo-Logarithmic Amplifier

In Figure 4.2 the output voltage is plotted against the logarithm of the swept resistor values, and it is clear that the output voltage is exhibiting linear-in-dB behavior. Thus, the output voltage can be said to be linear-in-dB with the input current, which, again, is set by the resistor. It is important to note that the output is saturated just above 4V until the input current reaches 1mA, and once it drops below 1nA, there is a corresponding deviation from linear-in-dB behavior. In order to determine how closely the output approximates ideal behavior, MATLAB was used to

add a first order line of best fit over the data points that fall between the DIR of interest. This is shown in Figure 4.3 below:

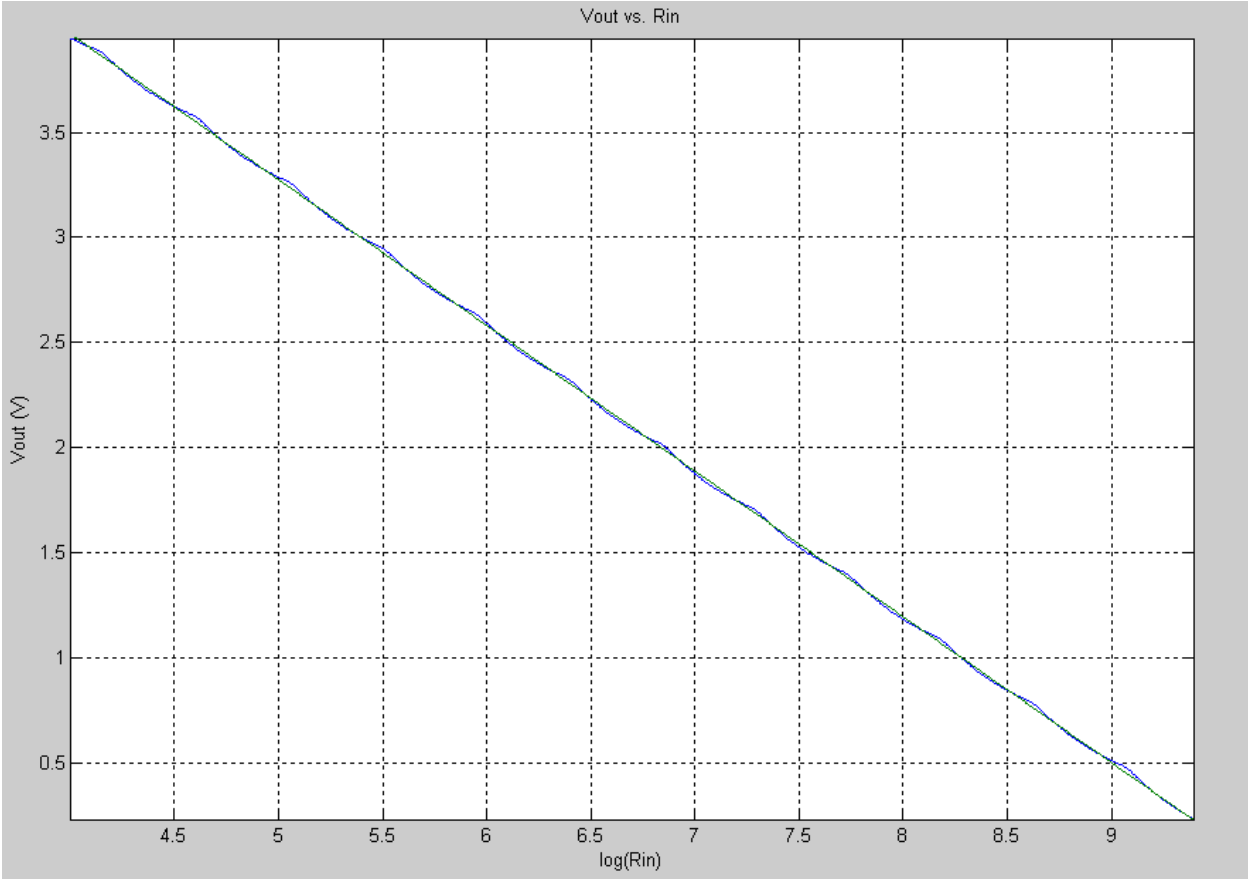


Figure 4.3: Simulated Output Voltage and Ideal Linear-in-dB

From Figure 4.3 it is evident that the high number of stages utilized in the limiter cascade have provided for an extremely accurate approximation of ideal linear-in-dB behavior. The error from the ideal can now be determined by subtracting the voltage output from it, which is shown in Figure 4.4 on the next page.



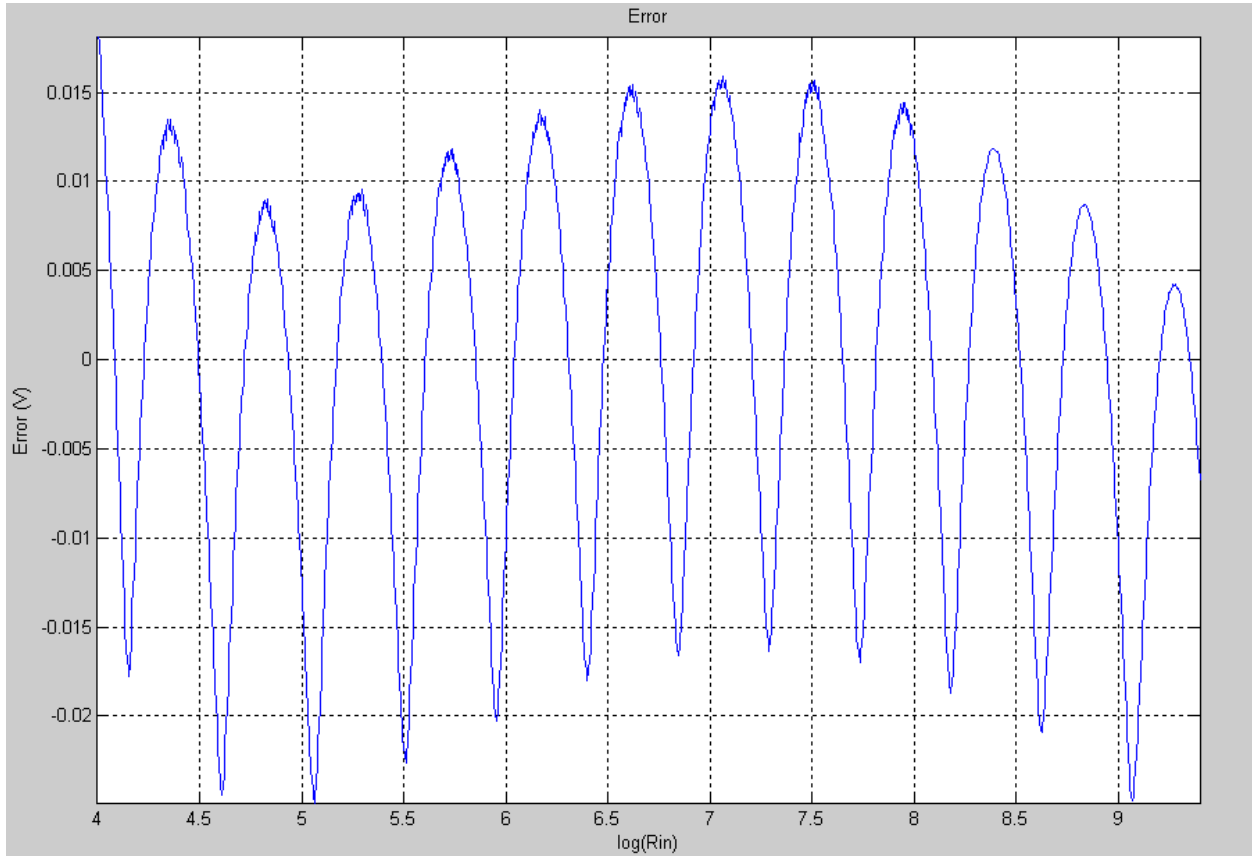


Figure 4.4: Error From Ideal Linear-in-dB Output

Figure 4.4 illustrates that the output error falls within  $\pm 25\text{mV}$  from the ideal, which is a deviation of  $\pm 0.625\%$  of the total output range of roughly  $4\text{V}$ .

## 4.2: Test Procedures and Protocols

Assuming adequate equipment is available, the characterization process of the  $120\text{dB}$  pseudo-logarithmic amplifier will actually be remarkably simple, although tedious. The following equipment will be needed:

- A high precision DC current source capable of generating currents between  $1\text{nA}$  and

1mA

- A DC voltage supply capable of providing 5V
- An oscilloscope

The following procedure will allow for the functionality and error from ideal behavior to be determined. This may be quite time consuming, and if at all possible some sort of automation would be greatly beneficial.

- 1) Connect the ground of the DC supply to pin 40, and the 5V output to pin 21.
- 2) Connect the output of the current supply to pin 10.
- 3) Connect the negative oscilloscope lead to the ground of the DC supply, and the positive lead to pin 26.
- 4) Set the current supply to output 1nA and record the corresponding output voltage.
- 5) Repeat step 4 for currents between 1nA and 1mA until sufficient data are gathered to accurately plot performance.
- 6) Use MATLAB (or some other program) to plot output voltage data versus the logarithm of the input current data; this will display overall functionality. MATLAB is preferable as its built in functions will greatly simplify the next several steps.
- 7) Generate a first order line of best fit for the data used in the plot created in step 6.
- 8) Subtract output data from the line of best fit; this will display error from ideal linear-in-dB behavior.

### **4.3: Summary and Conclusion**

The goal of this project was to design and implement a logarithmic amplifier in the AMI

0.5 $\mu$ m process. In accordance with this goal, various logarithmic amplification methodologies were investigated, and the pseudo-logarithmic approximation topology was chosen, designed, laid out, simulated, verified by DRC and LVS, and sent off for fabrication. All of the specifications set out in Table 1.1 were met except for the upper limit on the single-ended output voltage, which is still well within usable bounds. Thus, the design phase was in many ways a successful one, and the testing and characterization that will begin in the fall of 2007 will determine the extent of that success.

### **4.3: Recommendations for Future Work**

Perhaps the most important improvement that could be made to the overall system would be a reduction in its temperature dependence. In its present configuration a relatively low amount of power ( $\sim 0.45$ W) is consumed and therefore self-heating will not be an issue; however, if placed in a device that will be used in environmental extremes, or if  $I_{\text{bias}}$  is increased, this improvement will be entirely necessary. Fortunately, there is a simple solution. The overall temperature dependence is almost entirely due to that of  $I_{\text{bias}}$ ; thus, by replacing the simple MOS and resistor current reference with a temperature-compensated one, the overall system will be far more robust in regards to temperature variation. There are several configurations available for CMOS only temperature-compensated current references, and the large headroom associated with the AMI 0.5 $\mu$ m process will aid the selection of an optimum topology.

Several other possible improvements come in the form of digital control; predominately that of  $I_{\text{bias}}$ . A setup that would allow  $I_{\text{bias}}$  to take on several values, including zero, would be instrumental in the reduction of power consumption and the versatility of the overall system.

The ability to set  $I_{\text{bias}}$  to zero would effectively act as a power down mechanism for situations when the amplifier is not in use. Furthermore, providing several different values of  $I_{\text{bias}}$  would allow customization of the dynamic input range, which, in situations where only a small DIR is required, could save a great deal of power.

## REFERENCES

- [1] Kimmo Koli and Kari Halonen, "A 2.5V temperature compensated CMOS logarithmic amplifier," *IEEE 1997 Custom Integrated Circuits Conference*, pp. 79-82, May 1997.
- [2] Paul R. Gray, et al., *Analysis and Design of Analog Integrated Circuits*, Fourth Edition, John Wiley & Sons, Inc., New York, New York, © 2001. pp. 425-442.

## APPENDICES

- Appendices A1 and A2 contain MATLAB script and function code, respectively, and are used to simulate the performance of a pseudo-logarithmic amplifier having several different configurations of gain and number of stages that yield the same dynamic input range.
- Appendix A3 contains the small signal model of the current limiting amplifier used in this design project as well MATLAB code with the derived small signal equations that is used to verify amplifier operation.
- Appendix A4 contains the MATLAB code used to model the relationship between power consumption and the different configurations of gain and number of stages that yield the same dynamic input range.
- Appendix A5 contains both the top-level schematic of the 120dB pseudo-logarithmic amplifier and the completed chip layout.

## A1: PSEUDOLOG\_CONFIG\_COMBO\_SIM.M

```
%
% Programmer:      Zachary Richards
% Program Purpose: ECE547 Design Project
%

close all
clear all
home

% Define Cascade Parameters
Ibias = 1e-3;
I_in_min = 1e-9;
I_in_max = 1e-3;

% Define Number of Output Points
m = 0.5*1e7;

% Calculate Cascade Performance for N = 3,5,7,10,and 13
[Ilog3, r3, DR3] = pseudolog(Ibias,I_in_min,I_in_max,102,3,m);
% DR3
[Ilog5, r5, DR5] = pseudolog(Ibias,I_in_min,I_in_max,16.2,5,m);
% DR5
[Ilog7, r7, DR7] = pseudolog(Ibias,I_in_min,I_in_max,7.4,7,m);
% DR7
[Ilog10, r10, DR10] = pseudolog(Ibias,I_in_min,I_in_max,4.1,10,m);
% DR10
[Ilog13, r13, DR13] = pseudolog(Ibias,I_in_min,I_in_max,3,13,m);
% DR13

% Define Output Variable and Output Domain Variable
ILOG = (1e3)*[Ilog3;Ilog5;Ilog7;Ilog10;Ilog13];
R = [r3;r5;r7;r10;r13];

% Plot Results
figure
plot(R(1,:), ILOG(1,:), 'k', R(2,:), ILOG(2,:), 'k', R(3,:), ILOG(3,:), 'k', ...
      R(4,:), ILOG(4,:), 'k', R(5,:), ILOG(5,:), 'k')
title('Cascade Performance for Various N')
xlabel('log10(I_{in}(A))')
ylabel('I_{log} (mA)')
grid on
```

## A2: PSEUDOLOG.M

```
function [I_LOG,r_I_in_log,DR] = pseudolog(Ibias,I_in_min,I_in_max,G,N,m);

%
% PSEUDOLOG Calculate pseudo-logarithmic approximation
% [I_LOG,r_I_in_log,DR] = pseudolog(Ibias,I_in_min,I_in_max,G,N,m)
% calculates an output current, I_LOG, based upon a user specified bias
% current, Ibias; a user specified input current range defined by
% I_in_min and I_in_max; a user specified stage gain, G; and a user
% specified cascade size (the number of stages), N. The domain variable
% for the calculated output, r_I_in_log, as well as the resultant dynamic
% input range, DR, are also calculated and passed back. The number of
% points to be calculated, m, is also specified by the user.
%
%
% Programmer:          Zachary Richards
% Program Purpose:    ECE547 Design Project
%
%
% Initialize Output Variables
I_LOG = [];
r_I_in_log = [];
DR = 0;

% Calculate G_cascade
G_cascade = G-1;
for i = 1:N-1
    G_cascade = G_cascade*G;
end
DR = 20*log10(G_cascade);

% Define Current Input and Domain variable for Plotting
I_in = linspace(I_in_min,I_in_max,m);
r_I_in_log = log10(I_in);

% Calculate Output Current, I_LOG
I_SUM = zeros(N,m);
for i = 1:m
    if I_in(i) <= Ibias
        I_SUM(1,i) = I_in(i);
    else
        I_SUM(1,i) = Ibias;
    end
end
end
```



```
for i = 2:N
    for j = 1:m
        if I_in(j)*(G-1)*G^(i-2) <= Ibias
            I_SUM(i,j) = I_in(j)*(G-1)*G^(i-2);
        else
            I_SUM(i,j) = Ibias;
        end
    end
end
end
I_SUM;

I_LOG = zeros(1,m);
for i = 1:N
    I_LOG(1,:) = I_LOG(1, :)+I_SUM(i, :);
end

return;
```

### A3: ANALYSIS OF CURRENT LIMITING AMPLIFIER

The following figure is a small signal representation of the current limiting amplifier discussed in Section 3.2, and was used in conjunction with a MATLAB script, also below, to verify the theoretical operation of the amplifier

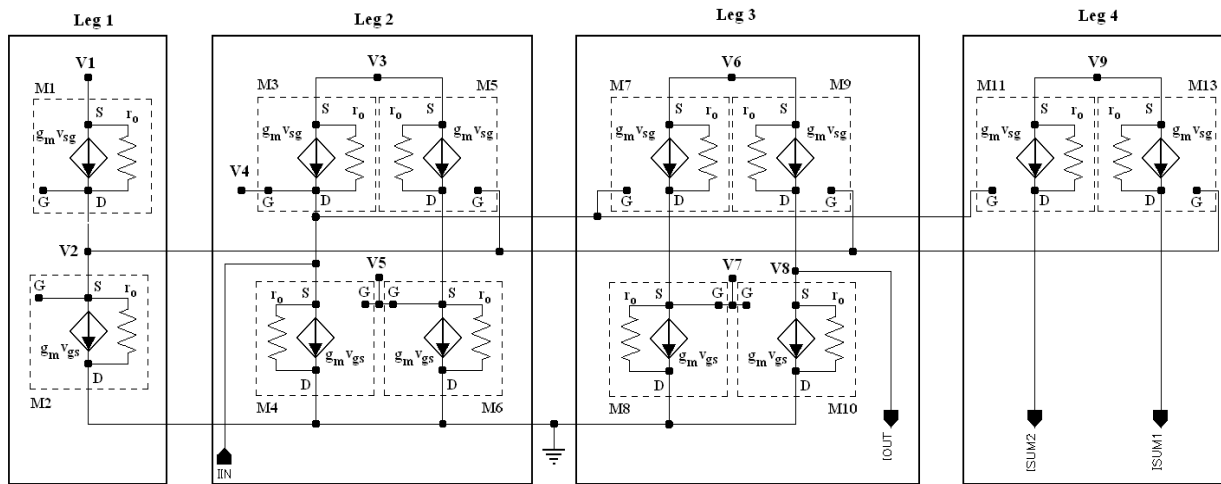


Figure A3.1: Small Signal Model of Current Limiting Amplifier

### PSEUDOLOG\_TF.M

```

%
% Programmer:      Zachary Richards
% Program Purpose: ECE547 Design Project
%

```

```

clear all
close all
home

```

```

%*****%
%   DEFINITIONS   %
%*****%

% Define Process Parameters
k_p = 18.4*1e-6;
k_n = 54.8*1e-6;
ibias = 1e-3;

lam_n = 0;      % NOTE:  Unfortunately, Lambda was not defined in the
lam_p = 0;      %           process models, so these Vllues were assumed as
                %           ideal.

% Define Aspect Ratio Multiplier
G = 3;

% Approximate Small Signal Device Parameters
r01 = (1/lam_p)/(ibias/2);
r02 = (1/lam_n)/(ibias/2);
r03 = (1/lam_p)/(ibias/2);
r04 = (1/lam_n)/(ibias/2);
r05 = (1/lam_p)/(ibias/2);
r06 = (1/lam_n)/(ibias/2);
r07 = (1/lam_p)/(G*ibias/2);
r08 = (1/lam_n)/(G*ibias/2);
r09 = (1/lam_p)/(G*ibias/2);
r10 = (1/lam_n)/(G*ibias/2);
r11 = (1/lam_p)/(ibias/2);
r13 = (1/lam_p)/(ibias/2);
gm1 = sqrt(2*k_p*(3*8*(6/2.4))*(ibias/2));
gm2 = sqrt(2*k_n*(8*(6/2.4))*(ibias/2));
gm3 = sqrt(2*k_p*(3*8*(6/2.4))*(ibias/2));
gm4 = sqrt(2*k_n*(8*(6/2.4))*(ibias/2));
gm5 = sqrt(2*k_p*(3*8*(6/2.4))*(ibias/2));
gm6 = sqrt(2*k_n*(8*(6/2.4))*(ibias/2));
gm7 = sqrt(2*k_p*(G*3*8*(6/2.4))*(G*ibias/2));
gm8 = sqrt(2*k_n*(G*8*(6/2.4))*(G*ibias/2));
gm9 = sqrt(2*k_p*(G*3*8*(6/2.4))*(G*ibias/2));
gm10 = sqrt(2*k_n*(G*8*(6/2.4))*(G*ibias/2));
gm11 = sqrt(2*k_p*(3*8*(6/2.4))*(ibias/2));
gm13 = sqrt(2*k_p*(3*8*(6/2.4))*(ibias/2));

% Set Input Current at Unity
i_in = 1;

```

```

% Set Load Resistance at Scope Magnitude
RL = 100*1e6;

%*****%
%   SMALL SIGNAL ANALYSIS EQUATIONS (IN MATRIX FORM)   %
%*****%

% From Leg 1:
A1 = [(1/r02+1/r01+gm2+gm1), (-1/r01-gm1); (-1/r01-gm1), (1/r01+gm1)];
B1 = [0;0];
V_Mat1 = (A1^-1)*B1;
V2 = V_Mat1(1,1);
V1 = V_Mat1(2,1);

% From Leg 2:
A2 = [(1/r03+1/r05+gm3+gm5), (-1/r03-gm3), (-1/r05);...
      (-1/r03-gm3), (1/r04+1/r03+gm3), (gm4);...
      (-1/r05-gm5), (0), (1/r06+1/r05+gm6)];
B2 = [0; i_in; -gm5*V2];
V_Mat2 = (A2^-1)*B2;
V3 = V_Mat2(1,1);
V4 = V_Mat2(2,1);
V5 = V_Mat2(3,1);

% From Leg 3:
A3 = [(1/r07+1/r09+gm7+gm9), (-1/r07), (-1/r09);...
      (-1/r07-gm7), (1/r08+1/r07+gm8), (0);...
      (-1/r09-gm9), (gm10), (1/r10+1/r09+1/RL)];
B3 = [(gm7*V4+gm9*V2); (-gm7*V4); (-gm9*V2)];
V_Mat3 = (A3^-1)*B3;
V6 = V_Mat3(1,1);
V7 = V_Mat3(2,1);
V8 = V_Mat3(3,1);

% Output Equations
i1 = V6/r09+gm9*(V6-V2);
i2 = gm10*V7+V8/r10;
i_out = i1 - i2;
Ai = i_out/i_in;

```

```
% Display Results  
i_out  
Ai
```

## **MATLAB COMMAND WINDOW RESULTS**

```
i_out =  
      3  
  
Ai =  
      3  
  
>>
```

## A4: POWER\_VS\_N.M

```
%
% Programmer:      Zachary Richards
% Program Purpose: ECE547 Design Project
%

close all
clear all
home

% Define Stage Number and Gain Matrices
N = [3,5,7,10,13];
G = [102,16.2,7.4,4.1,3];

% Define Bias Current and VDD
ibias = 1e-3;
vdd = 5;

% Calculate Power for N,G Combinations
P = [];
for i = 1:5
    P(1,i) = vdd*ibias*((1+0.5*1+1+(G(1,i)-1)*1+1)+...
        (N(1,i)-1)*(1+0.5*1+1+G(1,i)*1+1));
end

% Plot Results
figure
plot(N,P,'kd-')
title('Cascade Power Consumption vs. Number of Stages for 120dB of DIR')
xlabel('Number of Stages')
ylabel('Power Consumption (W)')
grid on
```

## A5: TOP LEVEL SCHEMATIC AND FULL CHIP LAYOUT

Both of the following figures appear in the “paper proper”; however, they have also been included in this appendix for convenience and easy reference.

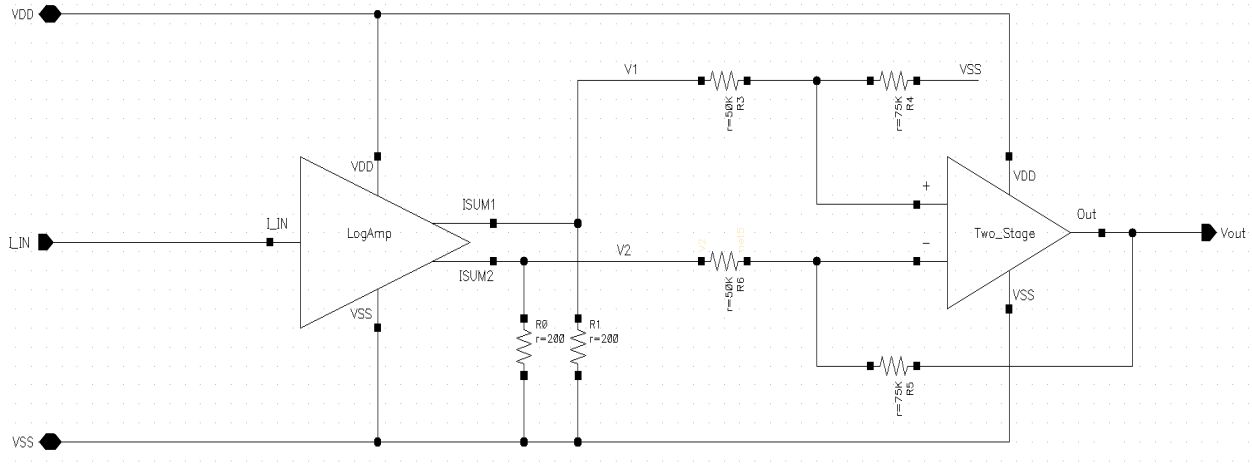


Figure A5.1: Top-Level Schematic of the 120dB Pseudo-logarithmic Amplifier

NOTE: The cell “LogAmp” contains the cascade of limiting current amplifiers described in section 3.2, and the cell “Two\_Stage” contains the two-stage operational amplifier described in section 3.4.

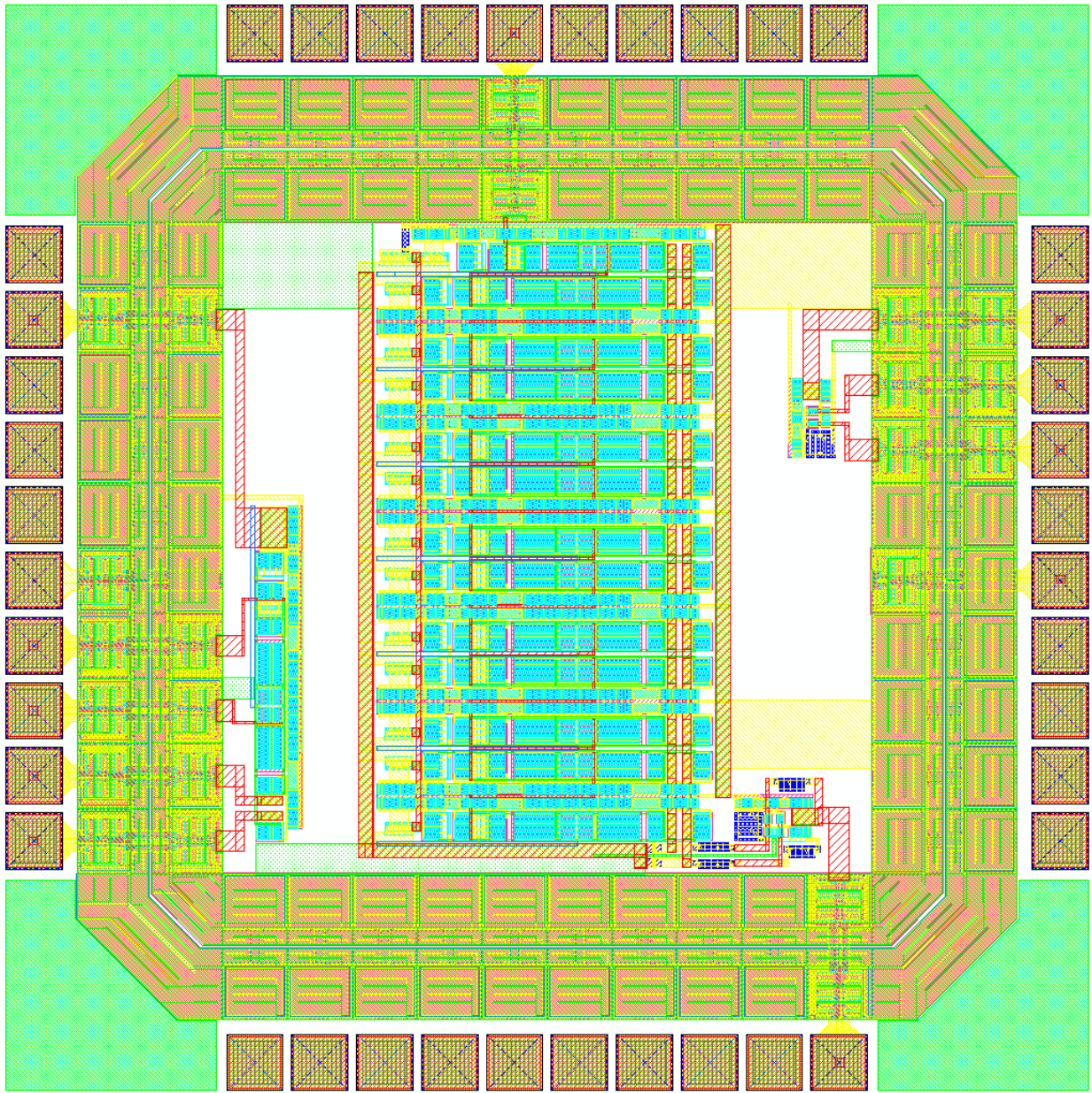


Figure A5.2: Completed Chip Layout

NOTE: This layout contains the 120dB pseudo-logarithmic amplifier as well two additional test structures—a single current limiting amplifier and a two-stage opamp.



## **BIOGRAPHY OF THE AUTHOR**

Zachary Richards was born in Ellsworth, Maine on October 3, 1984, and grew up in the small coastal town of Roque Bluffs, Maine. He began attending the University of Maine in September of 2002 and graduated with his Bachelor of Science degree in Electrical Engineering in May of 2006. While an undergraduate he also completed minors in Mathematics and English. He returned to the University of Maine in September of 2006 to pursue a Master of Science degree in Electrical Engineering.

During his time at the University of Maine he has been a member of the Eta Kappa Nu, Tau Beta Pi, and Senior Skulls honor societies.

He currently resides in South Portland, Maine where he is completing a second summer internship with National Semiconductor as an analog IC design engineer.