10-Bit D/A Converter for 50MHz Direct Digital Synthesizer

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i. Abstract

VLSI design of a Direct Digital Synthesizer (DDS) for the AMI C5N process. The focus here will be on the implementation of a 50MHz DDS with particular attention being paid to the 10-bit DAC block. This DDS implementation includes a 12-bit Pipeline Accumulator, 8-bit ROM Pointer, 4x64-bit ROM, DAC Driver and 10-bit D/A Converter. This implementation is designed to operate at 50MHz (clock rate) and produce a 25MHz $1.7V_{p-p}$ sinusoidal output, centered at 2.55V. The chip output (pin 10) can drive a maximum capacitive load of 30pF in parallel with a minimum resistive load of 5kΩ. Spectral analysis of the output signal shows the fundamental signal strength (25MHz peak) to be approximately 30dB higher than the nearest overtone (50MHz).

Table of Contents

iv. List of Figures

1 Introduction

1.1 Synthesizers

Synthesizers are used in many applications where the generation of low distortion, frequency agile waveforms is critical. Devices such as function generators are basically very high performance synthesizers. Two technologies dominate the world synthesizer design, Analog PLL and Direct Digital Synthesizers (DDS).

1.2 Direct Digital Synthesizer (DDS)

DDS systems offer a number of advantages over analog PLL synthesizers, including precise and rapid manipulation of phase and frequency. Digital control of the DDS system allows for fast switching of signal frequency and phase. A DDS works by storing points of a waveform in digital format (in a ROM) and recalling the waveform data (using an Accumulator to point to the wave data in ROM). The recalled digital waveform is then converted to an analog waveform by way of a high speed DAC. The frequency at which the digital waveform is recalled determines the frequency of the analog signal output.

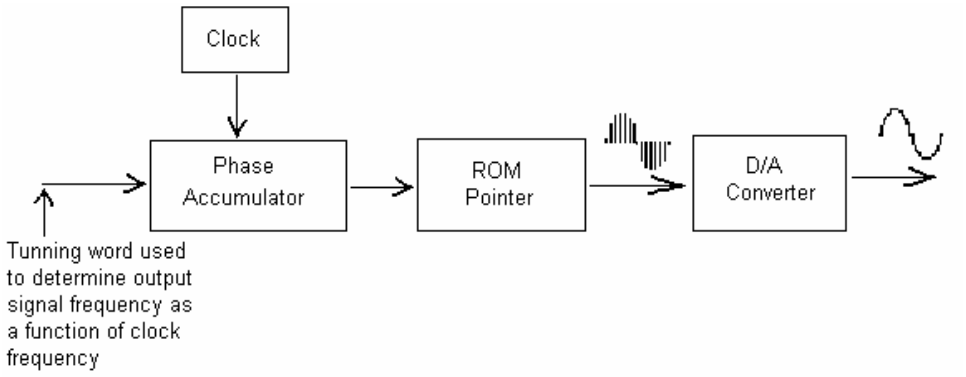

Figure 1.2[1] – Basic Block Diagram of a DDS

1.2.1 Pipeline Accumulator

Phase accumulators are devices that perform the arithmetic of mathematical integration. Accumulators can be implemented such that they either manipulate binary or decimal values, and accumulate the result in BCD format. The design used in this device implements pipelining which allows the accumulate to increase or decrease the DDS speed. The accumulator output is a phase ramp based on some fraction of the clock frequency.

For further detail on this design block please refer to the project report at http://www.eece.maine.edu/research/vlsi/Reghu.

1.2.2 ROM Pointer

Uses the phase ramp output of the accumulator to point to the appropriate address space in the ROM. The ROM pointer directs the ROM to output the appropriate digital waveform amplitude values at an appropriate rate, hence causing the ROM to output a digital representation of the intended waveform at the appropriate frequency. The ROM pointer implementation in this project uses on the first 8 most significant bits of the accumulator output.

For further detail on this design block please refer to the project report at http://www.eece.maine.edu/research/vlsi/Nikolic.

1.2.3 ROM

This is the memory mapping device of the DDS, it stores a digital representation of the waveform(s) that is to be created. The ROM is driven by the accumulator to output a digital representation of the waveform which is input to a DAC for creation of the analog waveform. The ROM implementation in this project is based on a 4x64-bit architecture.

For further detail on this design block please refer to the project report at http://www.eece.maine.edu/research/vlsi/Miller.

1.2.4 DAC Driver

This is an array of digital buffers pairs, one pair per input to the DAC. Each pair of buffers consists of two stages 3x (capacitive load multiplier) followed by a 10x stage. The two stages are required since each stage inverts its input. The DAC driver allows the inputs to the DAC to be driven at 25MHz.

For further detail on this design block please refer to the project report at http://www.eece.maine.edu/research/vlsi/Ramanujam.

1.2.5 D/A Converter

The DAC takes the digital waveform representation output of the ROM and converts it into an analog waveform of the same frequency. The DAC implementation in this project is based on a 10-bit R-2R Ladder input stage followed by a 3-Stage Op-Amp configured as a non-inverting voltage follower. The DAC is designed to operate at 25MHz while driving a capacitive load of up to 30pF and a resistive load as low as 5kΩ.

Details of the DAC design is present below in section 2.

1.3 Scope of Discussion

This report will explore in detail the design of only the 10-bit DAC implemented in this DDS. Details concerning other design blocks are beyond the scope of this document. Please refer to the reference listed for each design block if you require more information on its implementation.

2 DAC Circuit Design

2.1 3-Stage Op-Amp

The op-amp is based on a 3-stage architecture: a Differential Input stage, followed by a Common Source stage and finally a Buffer stage. It should be noted that Miller Compensation has been implemented to improve operational stability. Exclusion of this compensation will cause the output of the op-amp to oscillate about it desired output voltage.

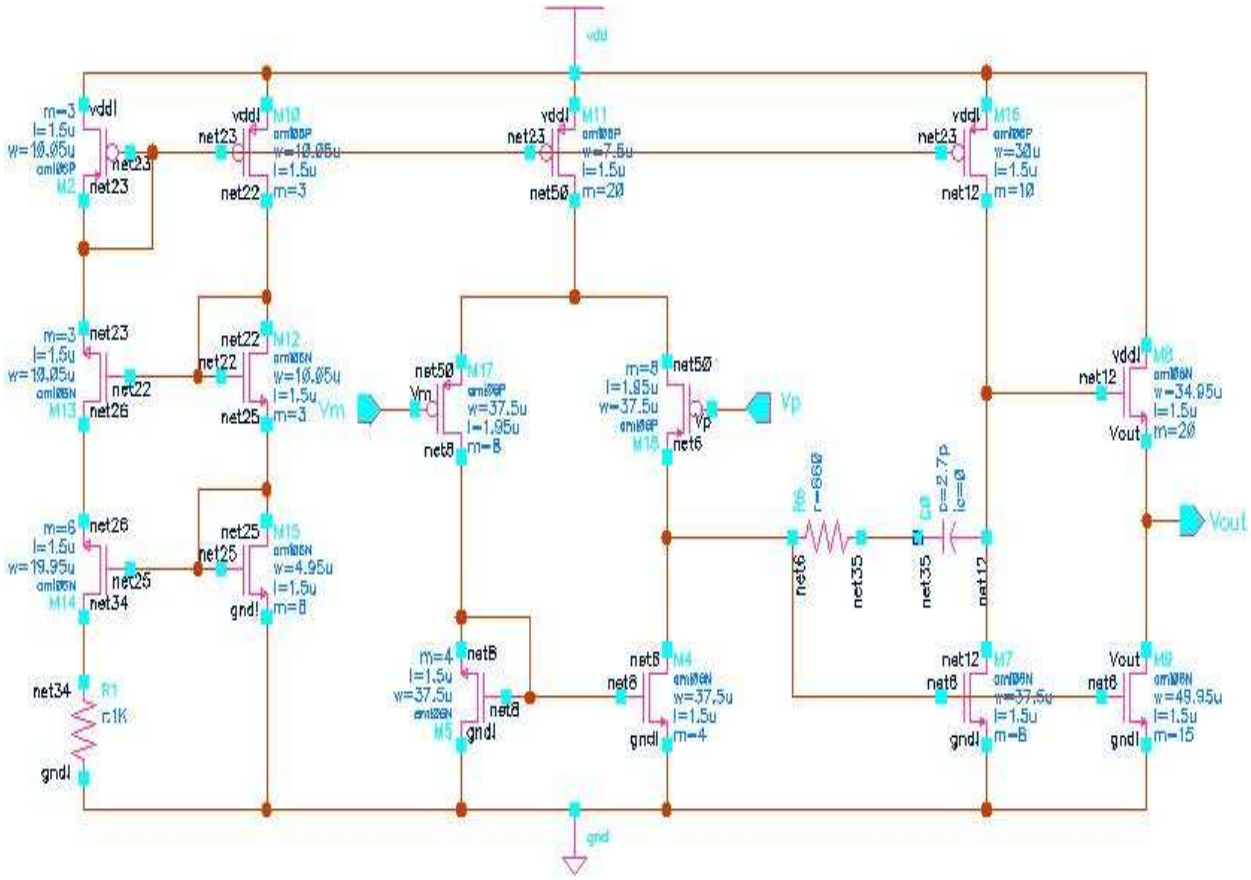

Figure 2.1[1] – 3-Stage Op-Amp Schematic

2.1.1 Biasing Circuit

The biasing circuit Q-points and shown below in Figure 2.1.1. This circuit is shown by simulation to draw no more than 0.65mA from the supply when operation at a temperature of approximately 75°C. The left most (reference) branch of the biasing circuit is designed to operate about a DC current Q-point of 0.25mA.

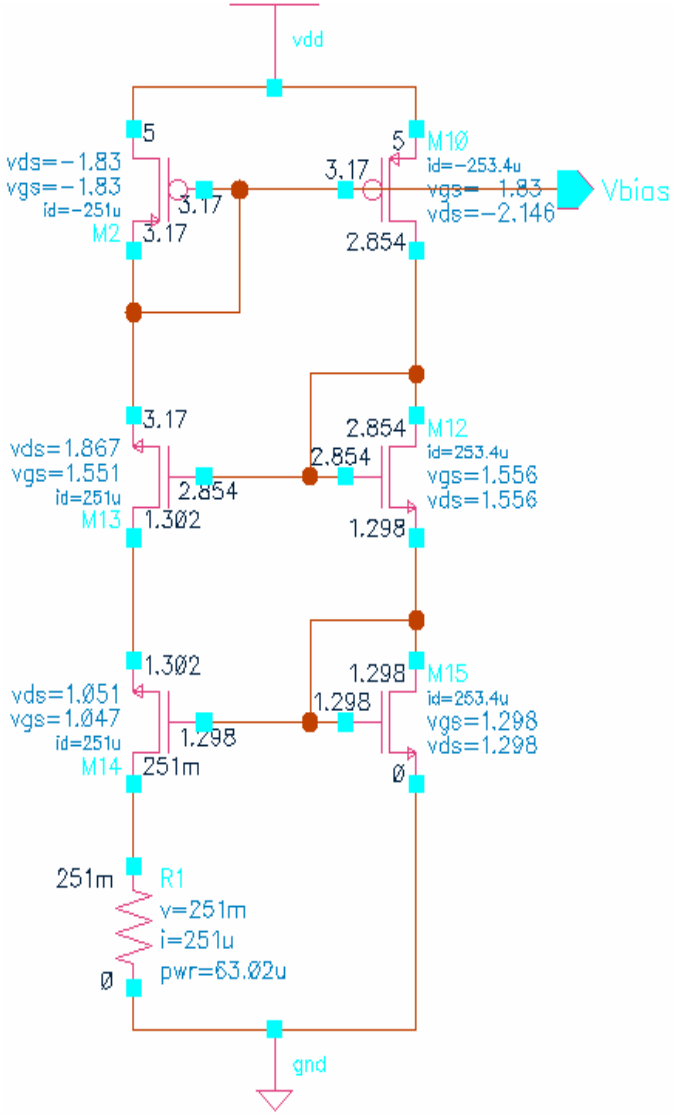

Figure 2.1.1[1] – Biasing Circuit Q-points

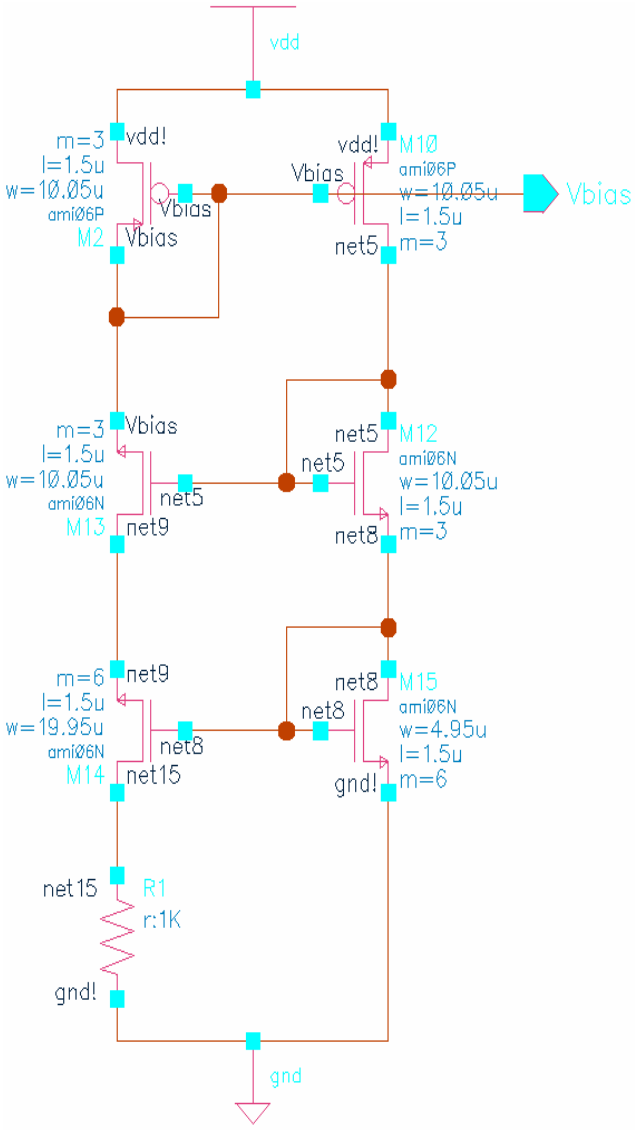

Figure 2.1.1[2] – Biasing Circuit Sizing

2.1.2 Differential Pair

Stage 1 of the op-amp is a fully differential input stage. This differential input stage was designed to operate about a DC Q-point current of 1.0mA. Simulation shows that with Miller Compensation from the Common Source stage, the differential input stage will actually draw approximately 0.65mA of current from the voltage supply.

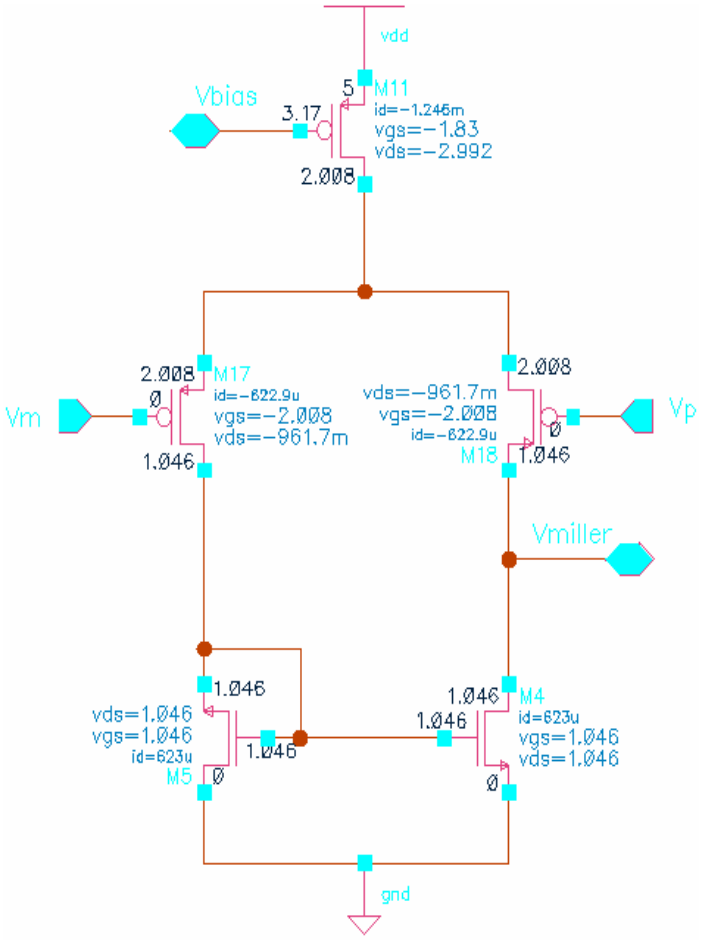

Figure 2.1.2[1] – Differential Pair Q-points

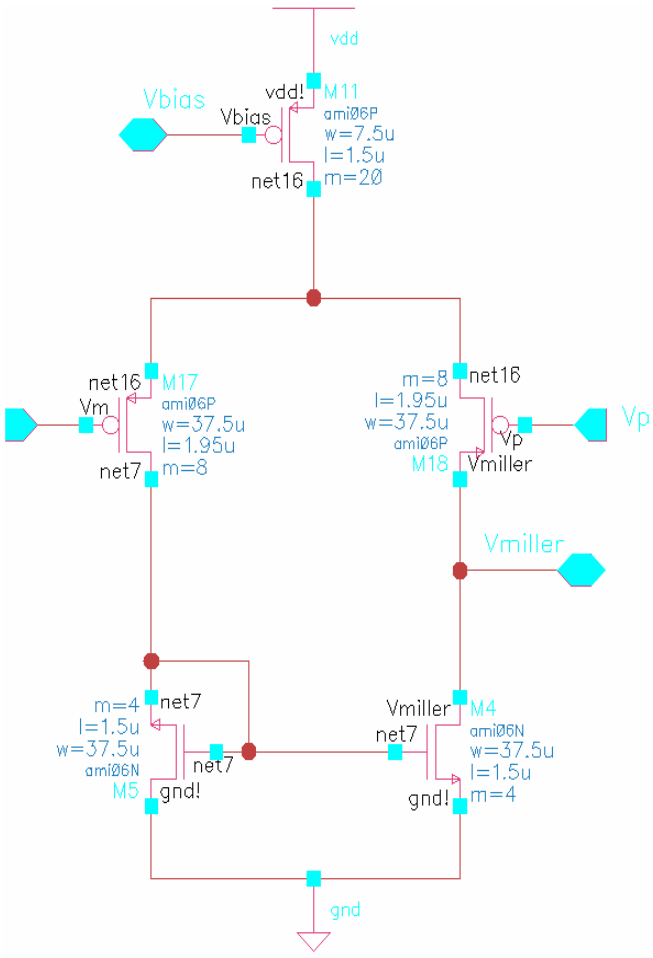

Figure 2.1.2[2] – Differential Pair Sizing

2.1.3 Common Source with Output Buffer

The final two stages of the op-amp are the common source and buffer stages. The common source stage offers greater amplification over a standalone differential pair, while the output buffer lowers considerably lowers the output resistance of the op-amp and matches the capacitive load of 30pF. The output buffer enables this op-amp to drive a minimum resistive load of 5kΩ in parallel with a maximum capacitive load of 30pF.

The final two stages of the op-amp can draw as much as 6mA of current from the power supply with the output buffer drawing as much as 4.5mA and the common source as much as 1.5mA.

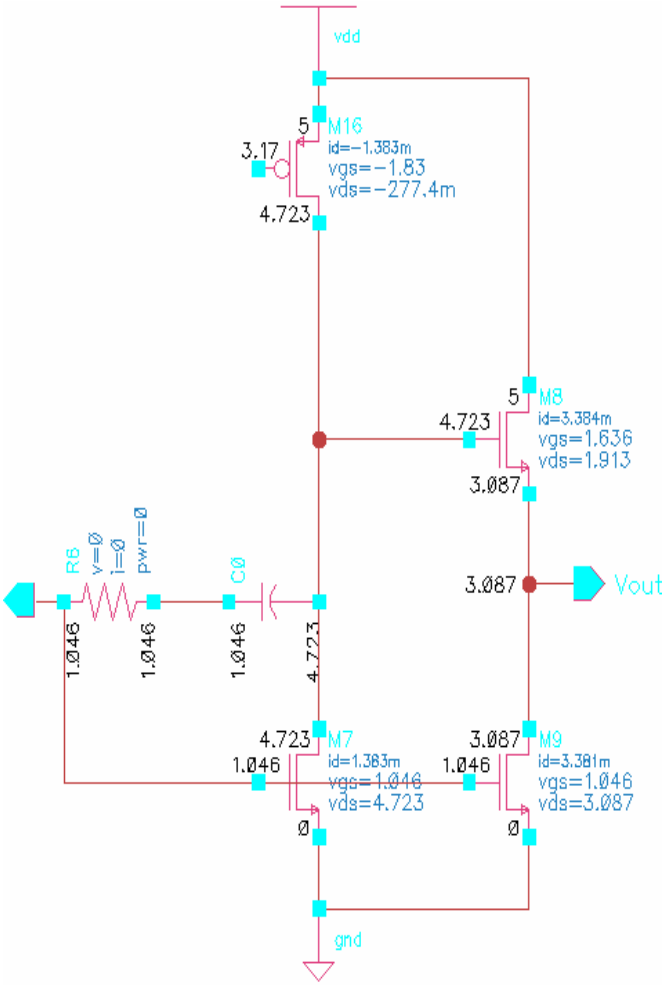

Figure 2.1.3[1] – CS & Buffer Q-points

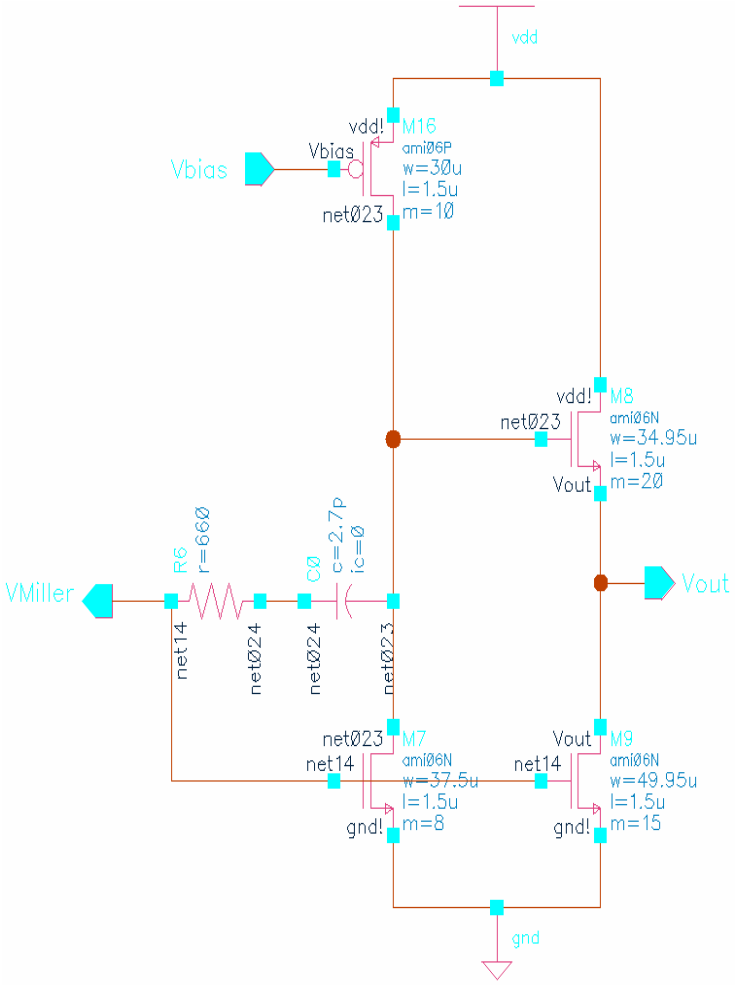

Figure 2.1.3[2] – CS & Buffer Sizing

2.2 Resistor Ladder

The resistor ladder design used in this DAC implementation was of the R-2R configuration, where R was chosen to be 15kΩ. The 3-stage op-designed did not offer rail-to-rail input capabilities (V_p needed to be constrained between 1.5V and 3.5V), so a 12-bit ladder was actually implemented only the 10 least significant bits were used for the DAC inputs, while the 11-bit was tied to V_{dd} (5V) and the 12-bit tied to ground. The ladder output was taken from base of the 11-bit input resistor, and in so doing offered an easy solution to retricting the input voltage to the op-amp to the required range (the actually input to V_p of the op-amp ranged from 1.7V to 3.4V).

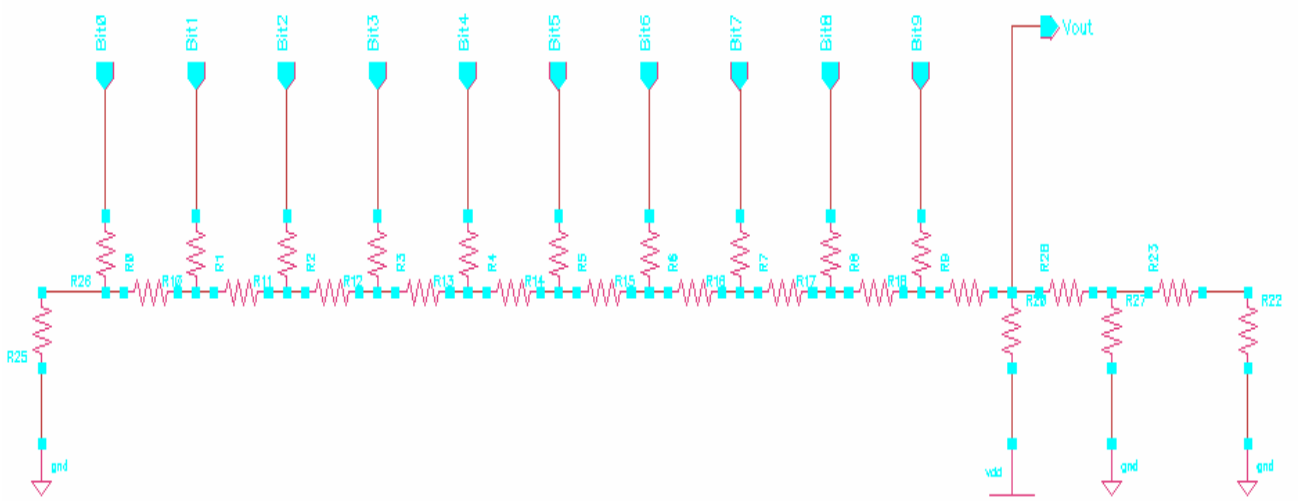

Figure 2.2[1] – R-2R Ladder Implementation

3 Simulation Results

3.1 Resistor Ladder Signal Response at 25MHz

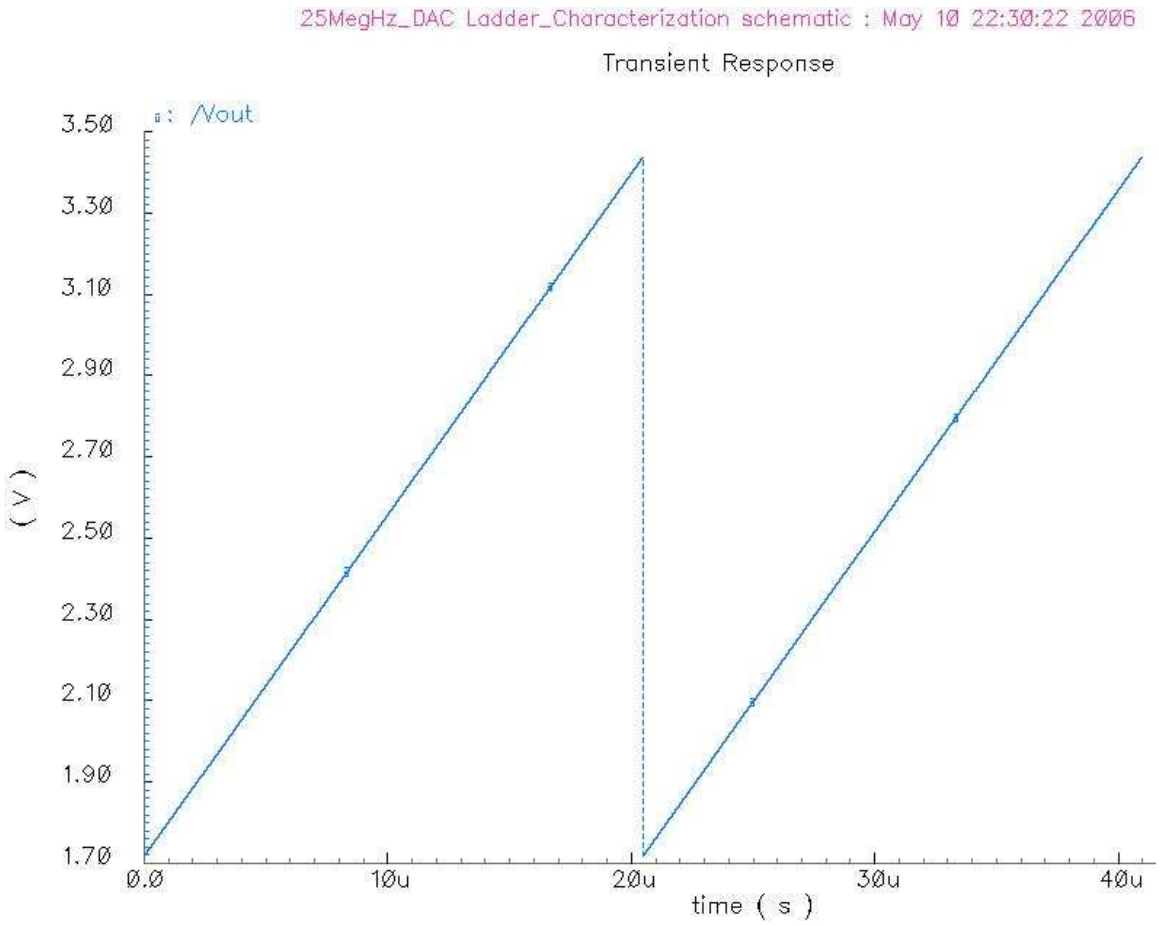

Figure 3.1[1] – Ramp Response of Ladder for 25MHz Input Transitions

Figure 3.1[2] shows the resolution of the 10-bit ladder implementation to be approximately 1.8mA.

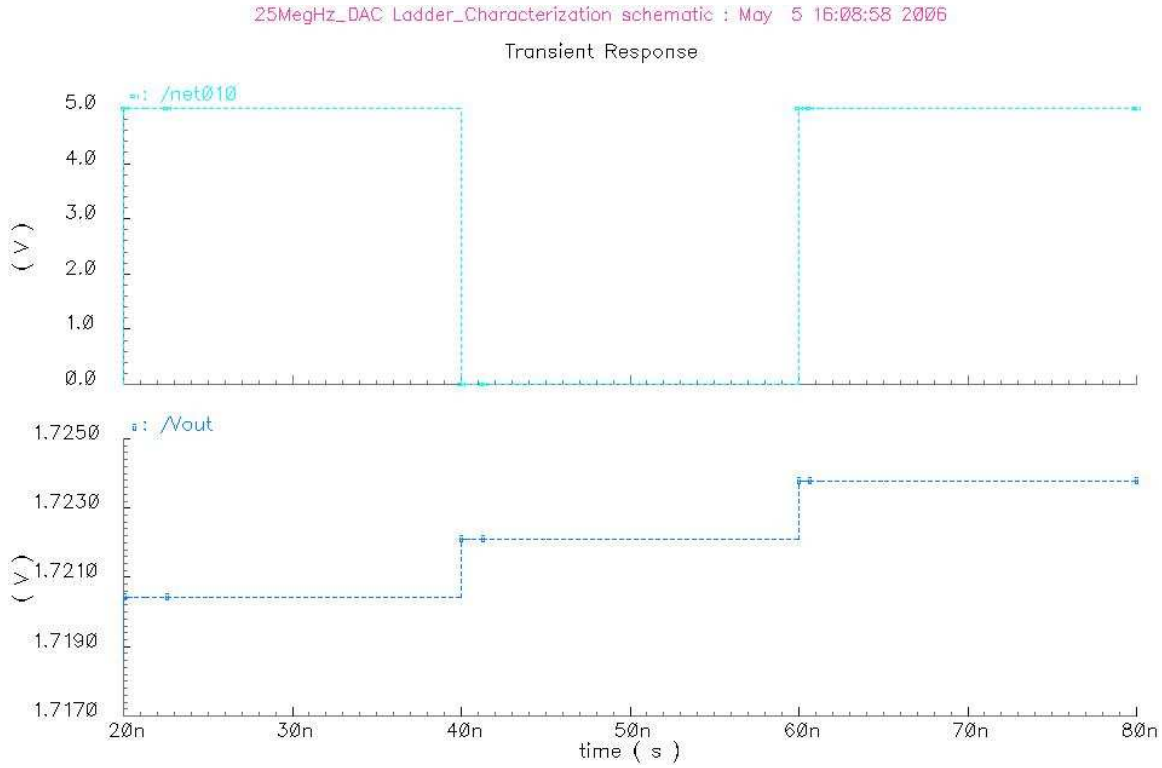

Figure 3.1[2] – Resistor Ladder Resolution

3.2 Op-Amp Signal Response

3.2.1 Step Response

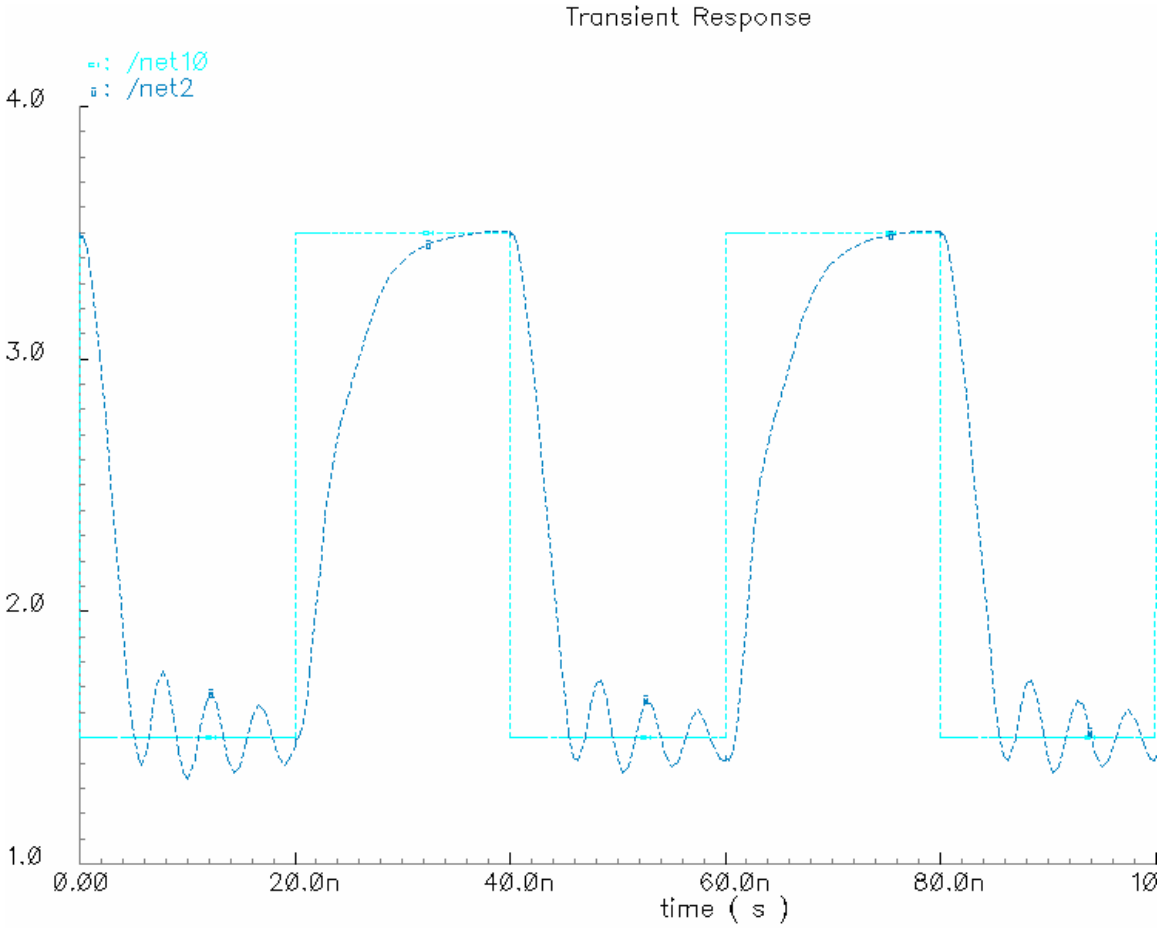

Figure 3.2.1[1] – Op-Amp Step Response

3.2.2 Sinusoidal Response

Figure 3.2.2[1] shows the op-amp output (/net2) following an input sine wave at 25MHz (/net10), while driving a 20pF capacitive load in parallel with a 1MΩ resistive load.

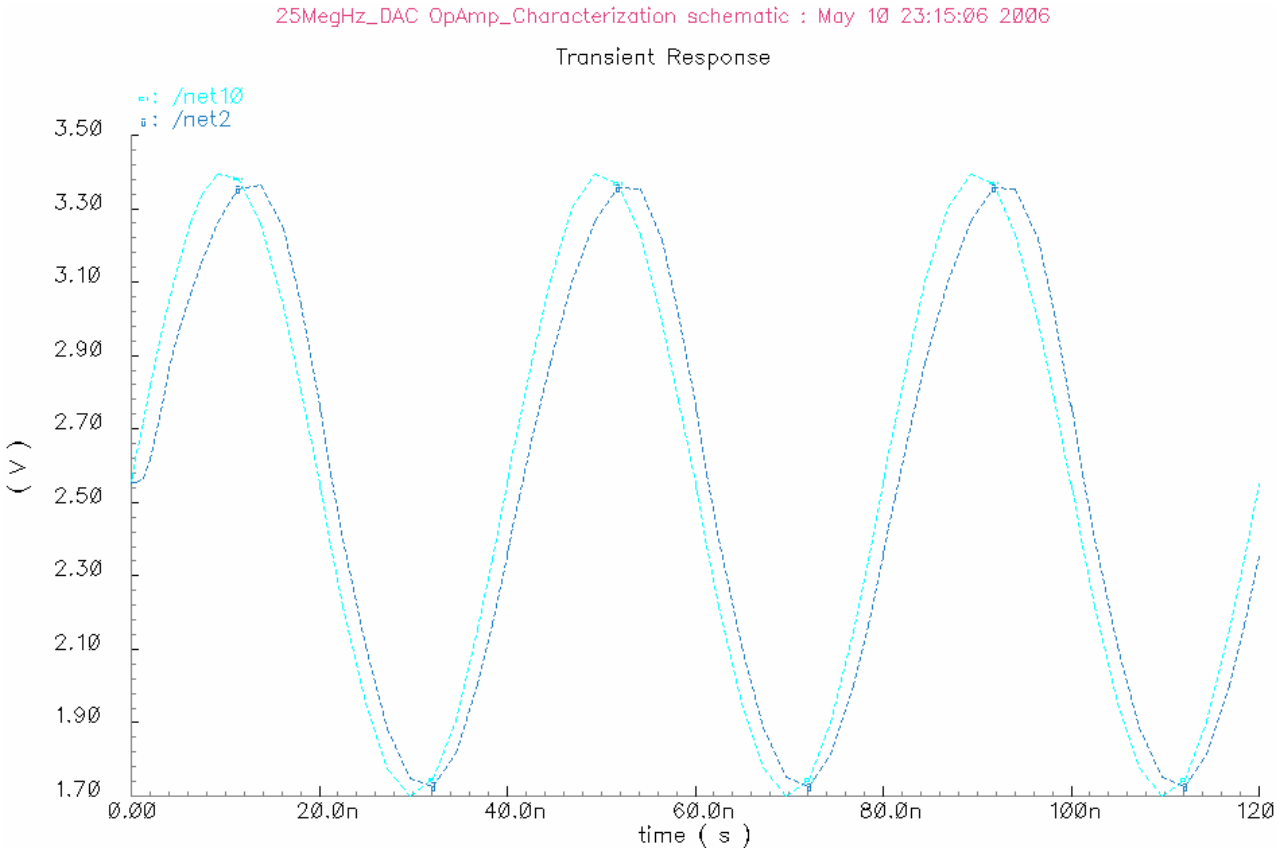

Figure 3.2.2[1] – Op-Amp Sinusoidal Response at 25MHz

Figure 3.2.2[2] shows the op-amp output (/net2) following an input sine wave at 50MHz (/net10), while driving a 20pF capacitive load in parallel with a 1MΩ resistive load.

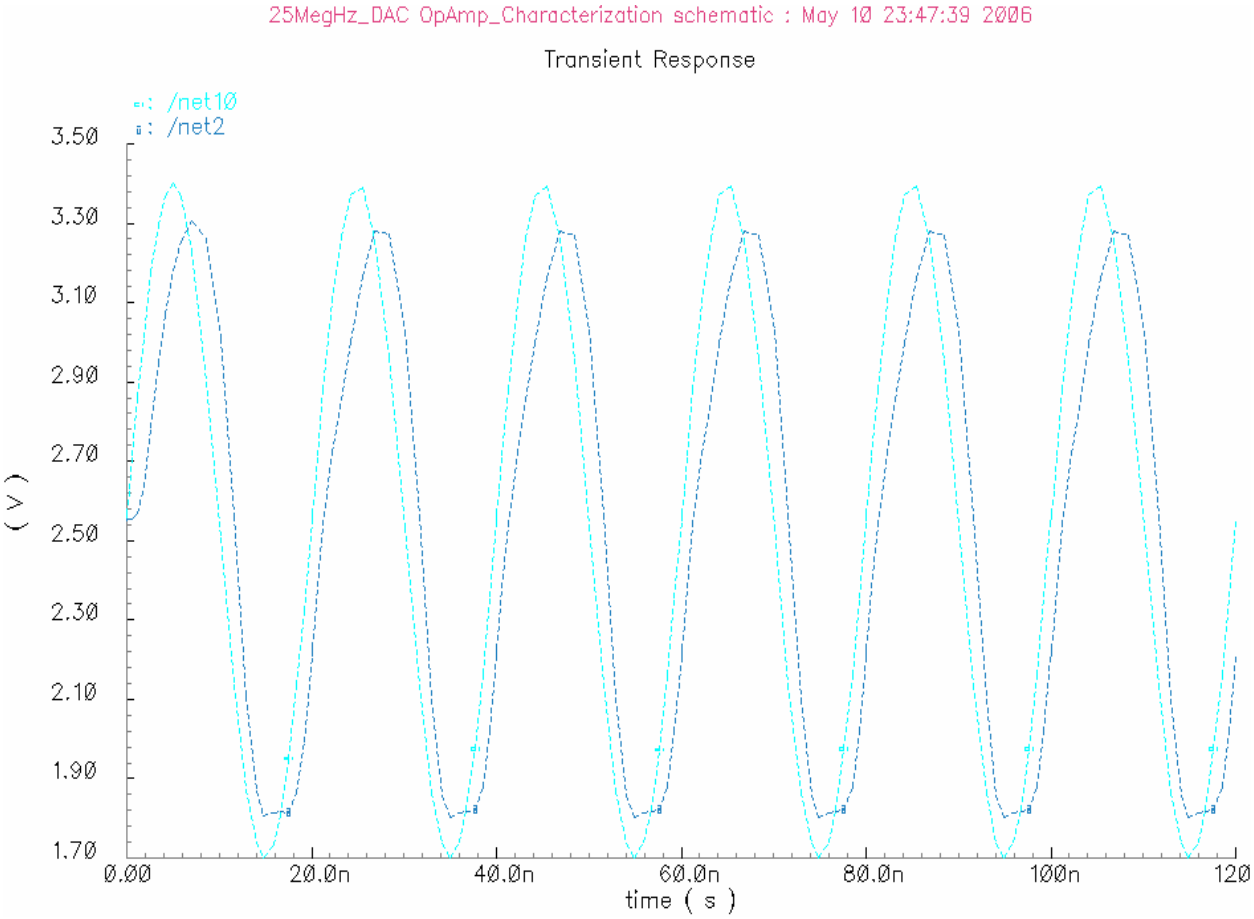

Figure 3.2.2[2] – Op-Amp Sinusoidal Response at 50MHz

3.2.3 AC Response

Figure 3.2.3[1] shows the ac response of the op-amp, note the instability that is centered at 190.55MHz. This is instability is most like as a result of in accurate pole-zero cancellation of the miller compensator, however since this op-amp is not meant to be operated beyond 25MHz the DDS system is not affected by this anomaly.

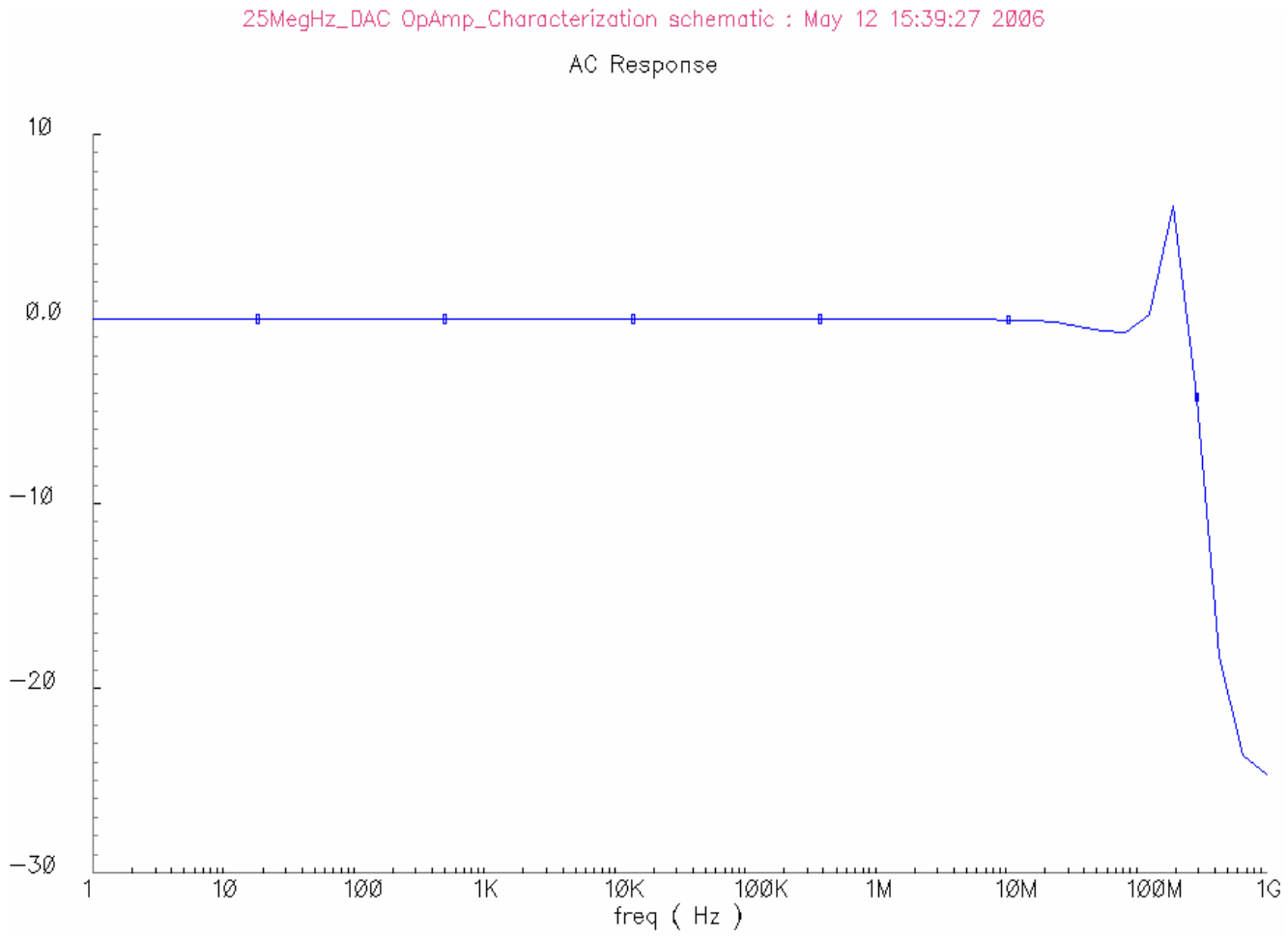

Figure 3.2.3[1] – AC Response of Op-Amp

3.3 DAC Signal Response

3.3.1 Ramp Response

Figure 3.3.1[1] shows the DAC's response to digital ramp waveform input. Notice the undershoot that occurs at 20.48u, at the start of the new cycle. This undershoot is as a result of slew rate limitations in the op-amp, it is interesting to note that this does not occur in the ladder's response (see Figure 3.1[1]).

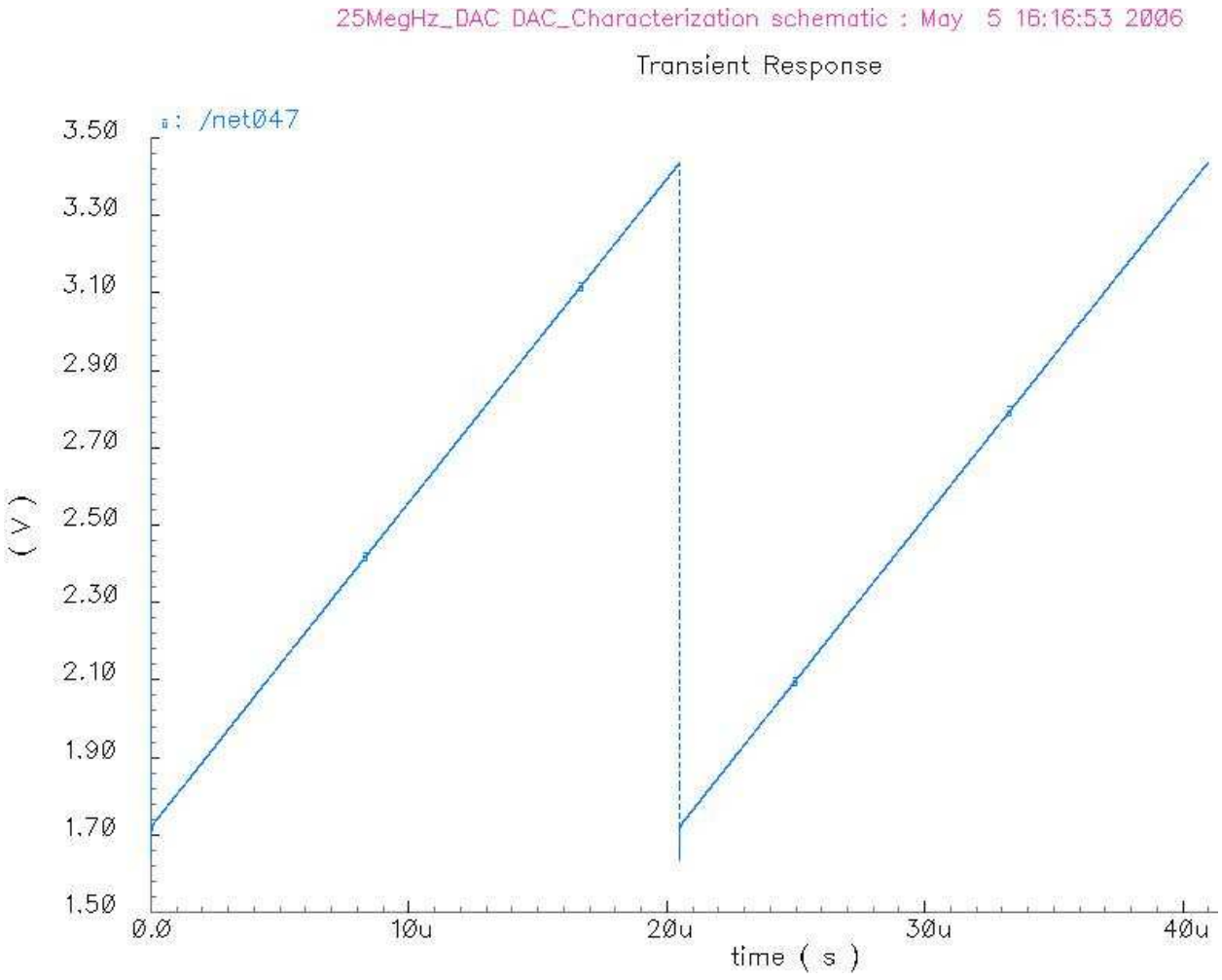

Figure 3.3.1[1] – DAC Ramp Response

The DAC offers some low pass filtering to the output signal, the 1.8mA steps the occur in the resistor ladder response (see Figure 3.1[2]), are somewhat smoothened.

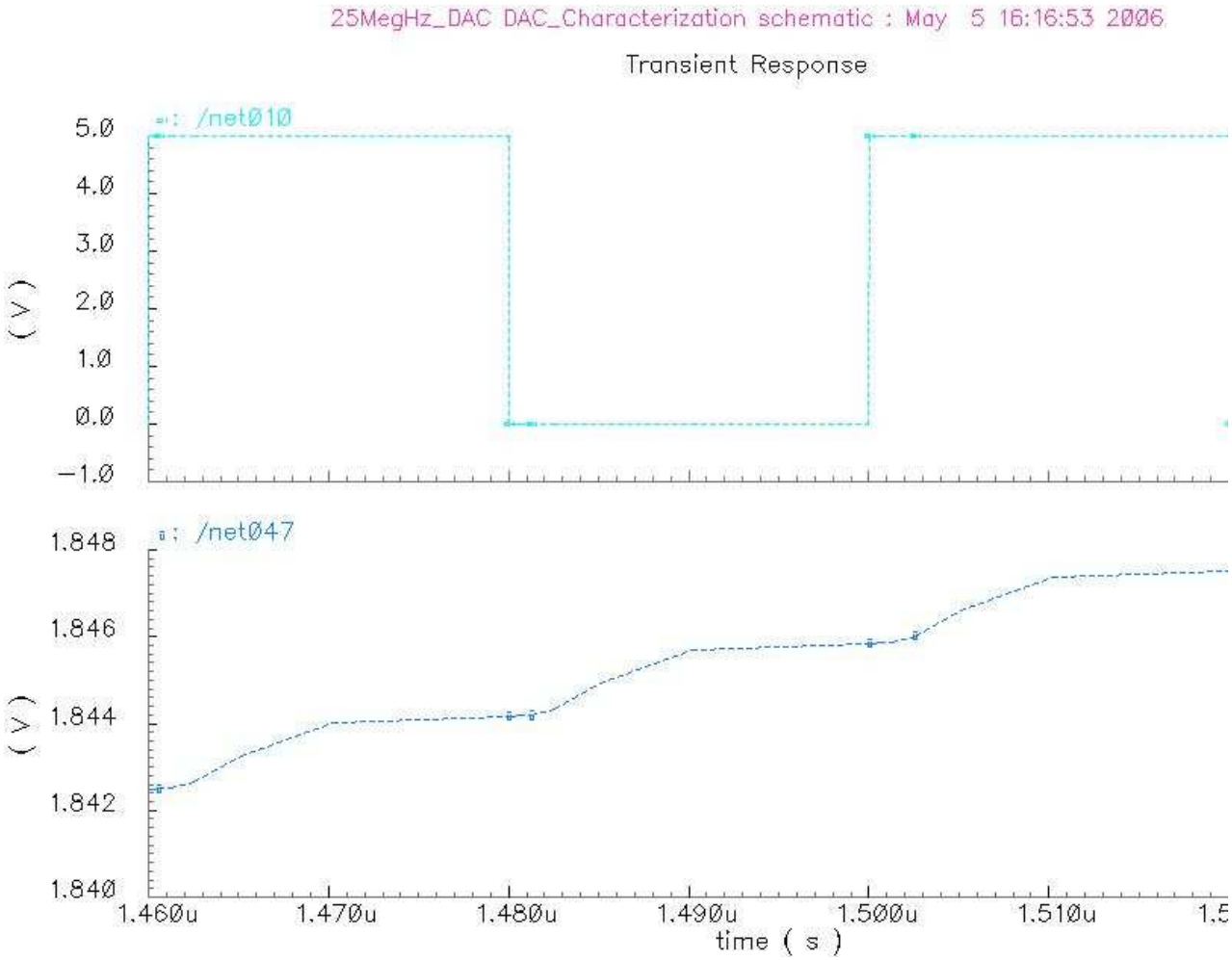

Figure 3.3.1[2] – DAC Resolution

4 Design Layout

4.1 Resistor Ladder

4.1.1 15kΩ Resistor

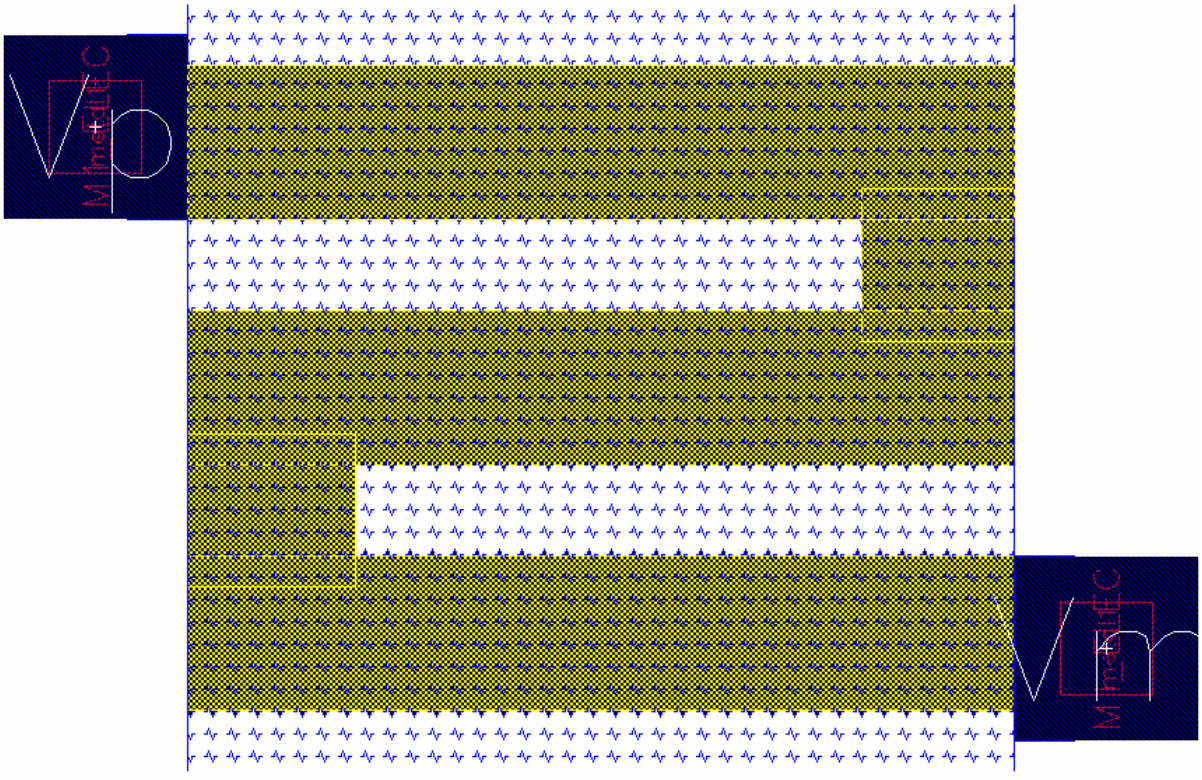

Figure 4.1.1[1] – Layout of 15kΩ Resistor

4.1.2 30kΩ Resistor

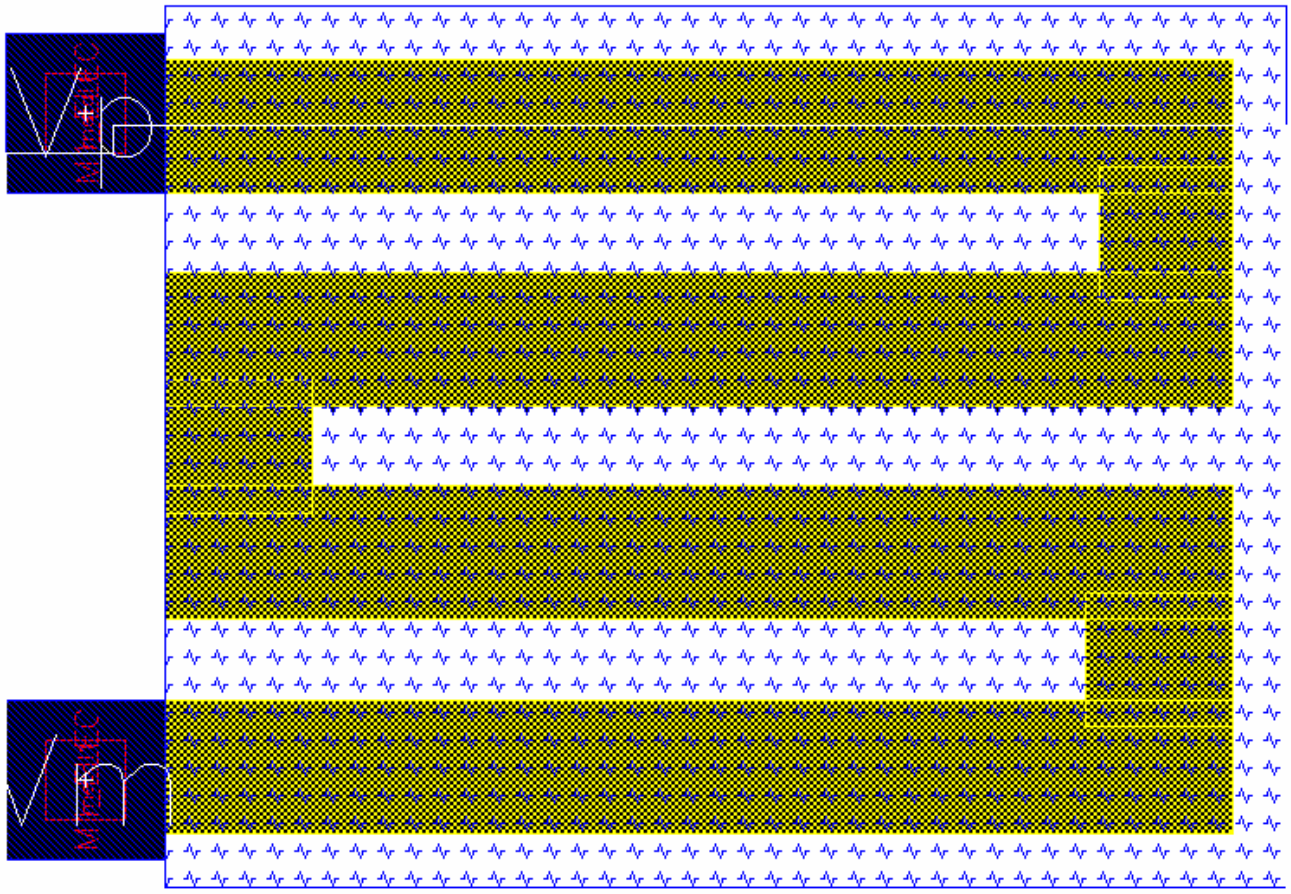

Figure 4.1.2[1] – Layout of 30kΩ Resistor

4.1.3 R-2R Configuration

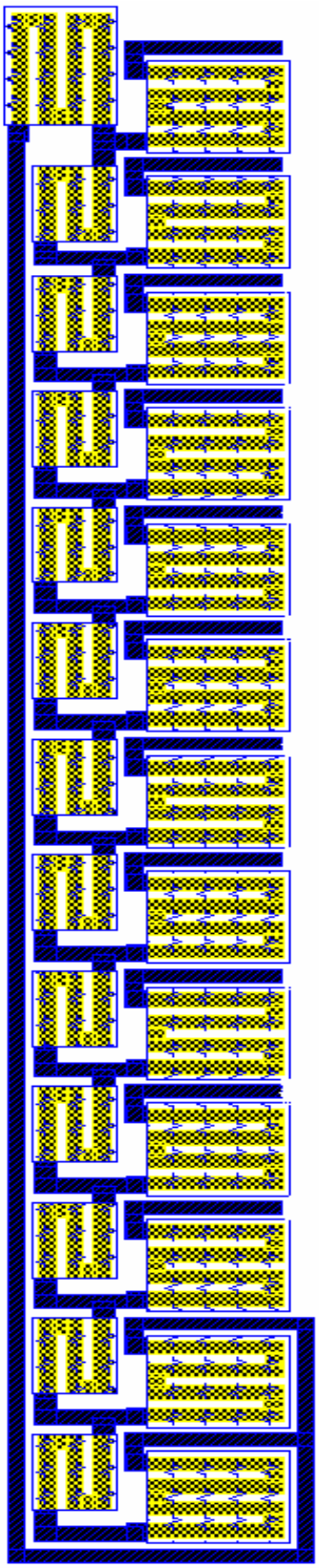

Figure 4.1.3[1] – Layout of R-2R Ladder

4.2 Op-Amp

4.2.1 Biasing Op-Amp

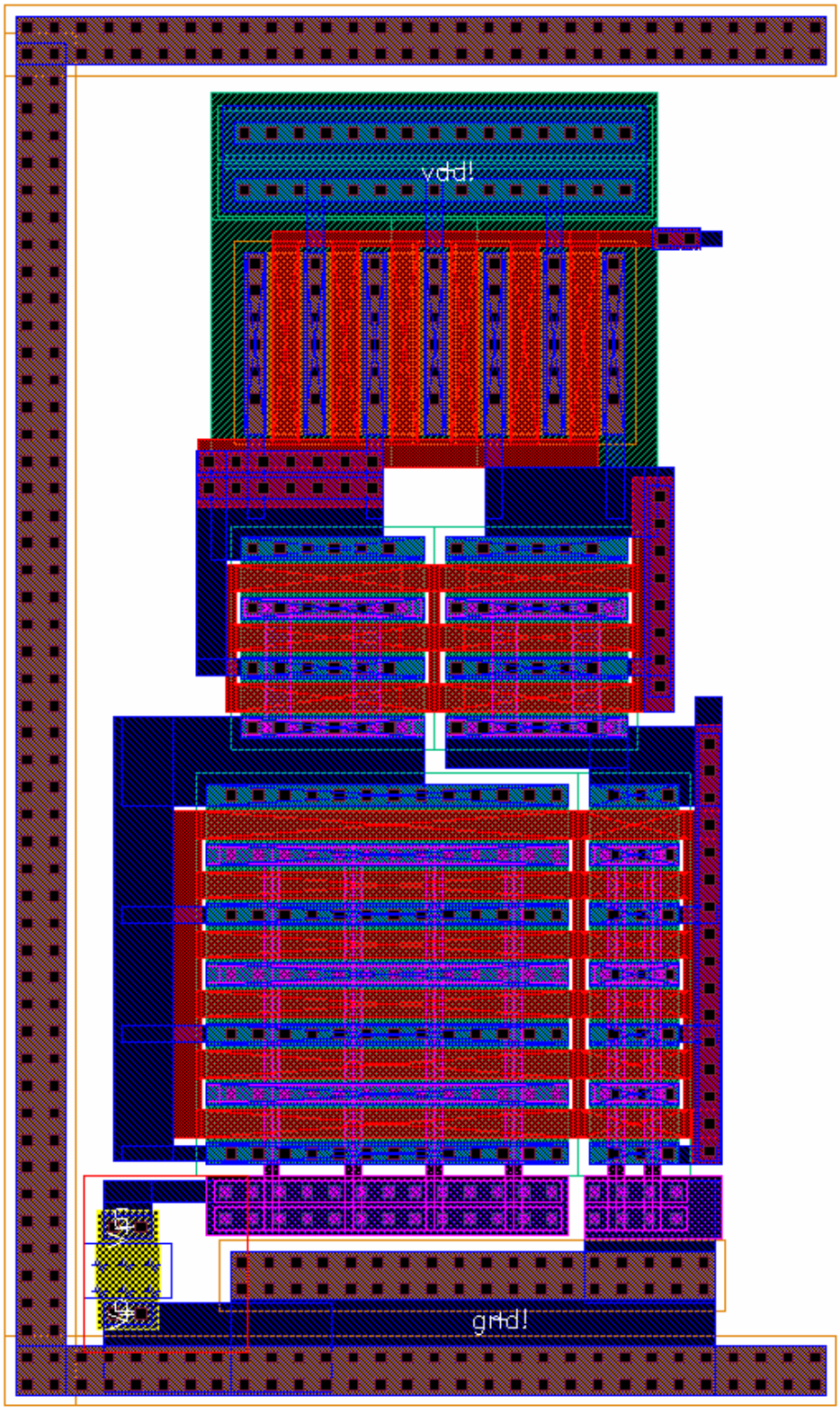

Figure 4.2.1[1] – Layout of Op-Amp Biasing Circuit

4.2.2 Differential Pair

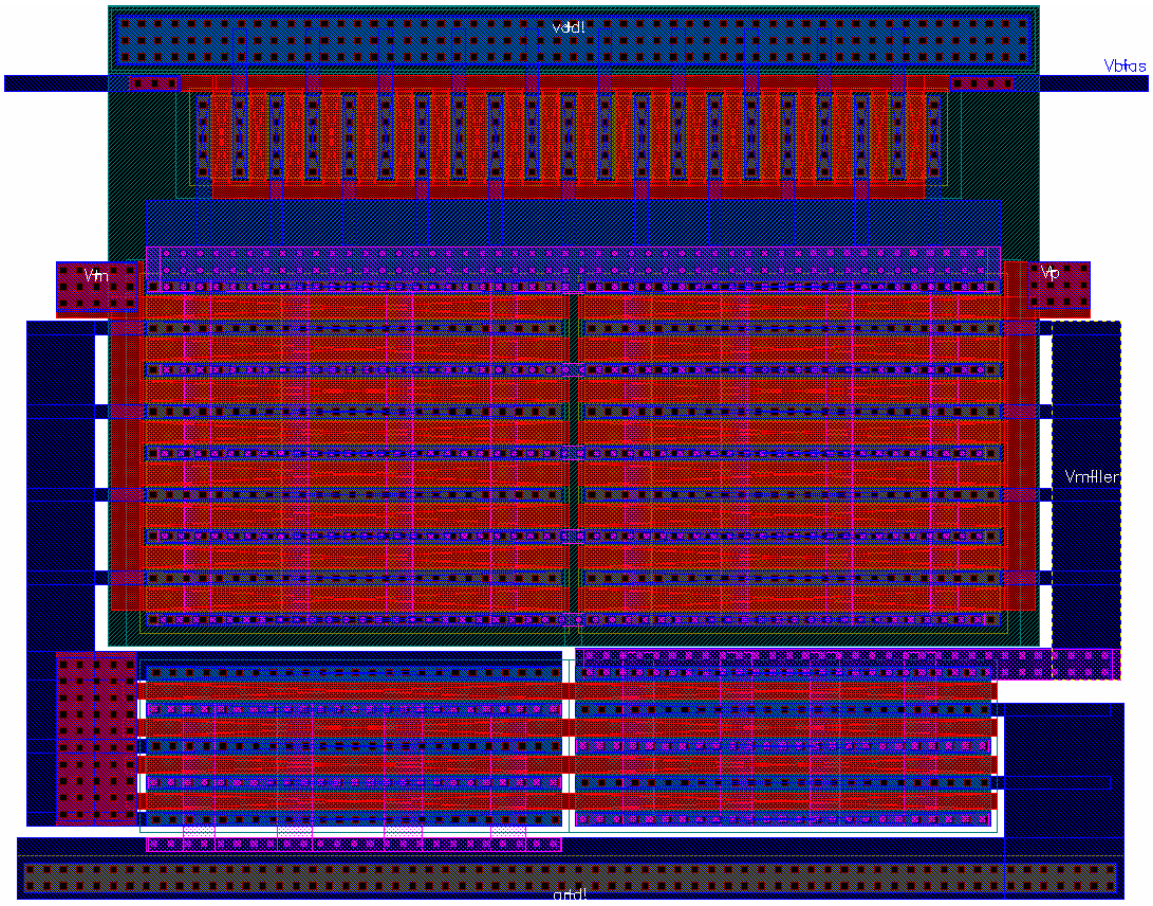

Figure 4.2.2[1] – Layout of Differential Input Stage

4.2.3 Common Source & Buffer with Miller Compensation

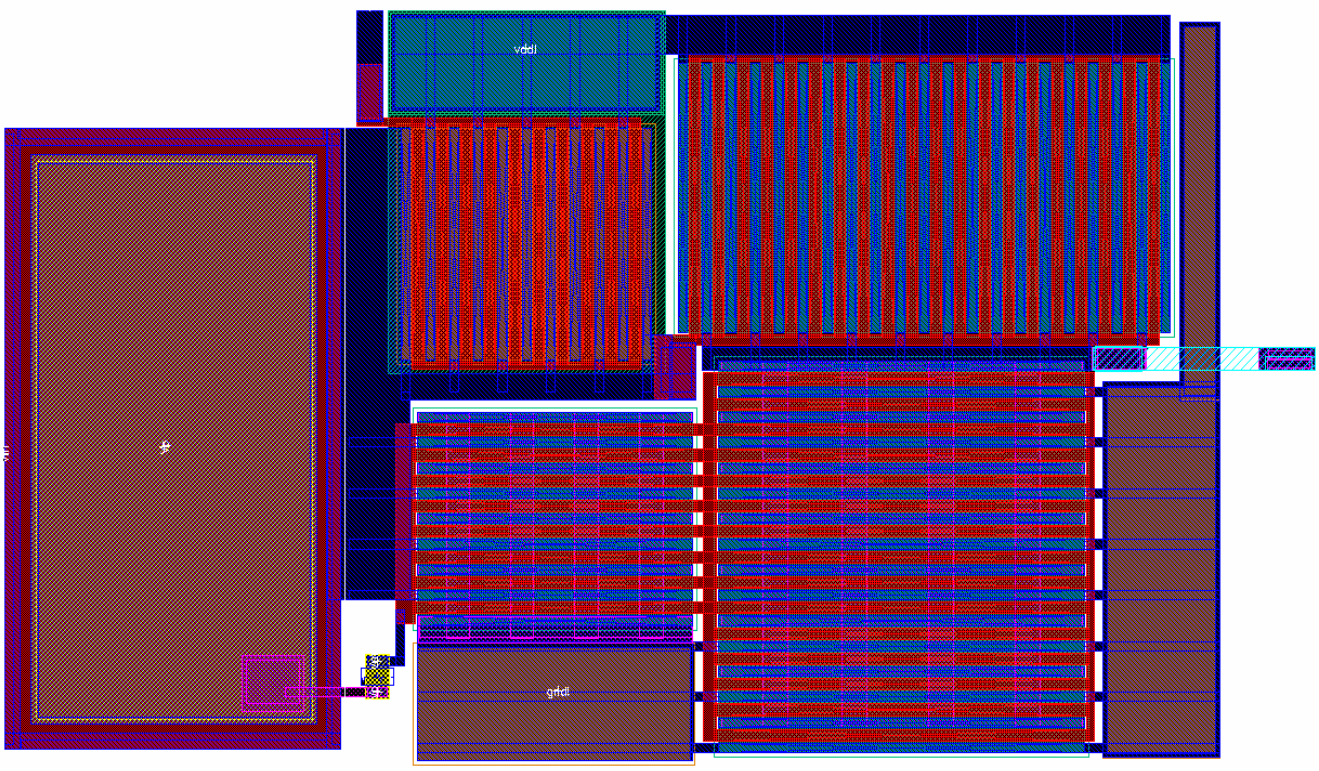

Figure 4.2.3[1] – Layout of CS and Buffer with Miller Compensator

4.2.4 Op-Amp Configuration

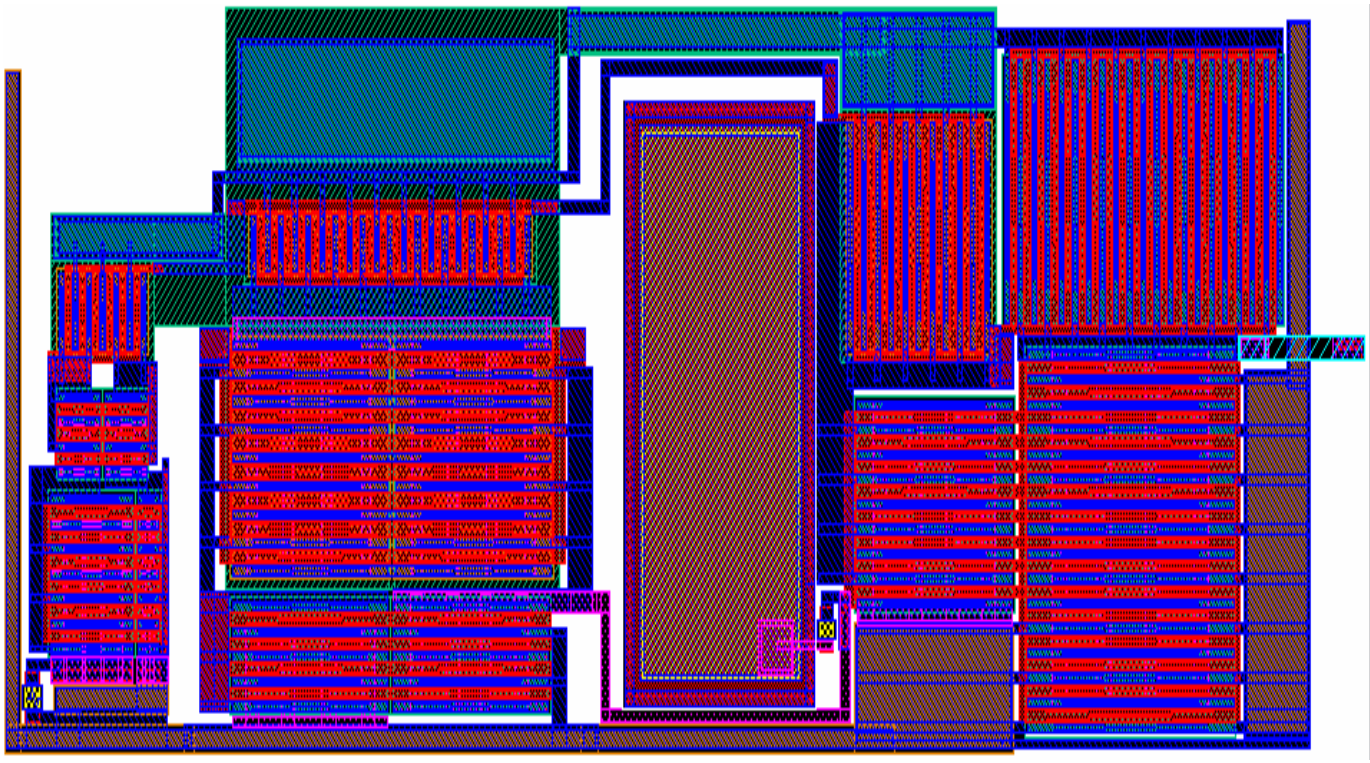

Figure 4.2.4[1] – Layout of Op-Amp

4.3 D/A Converter

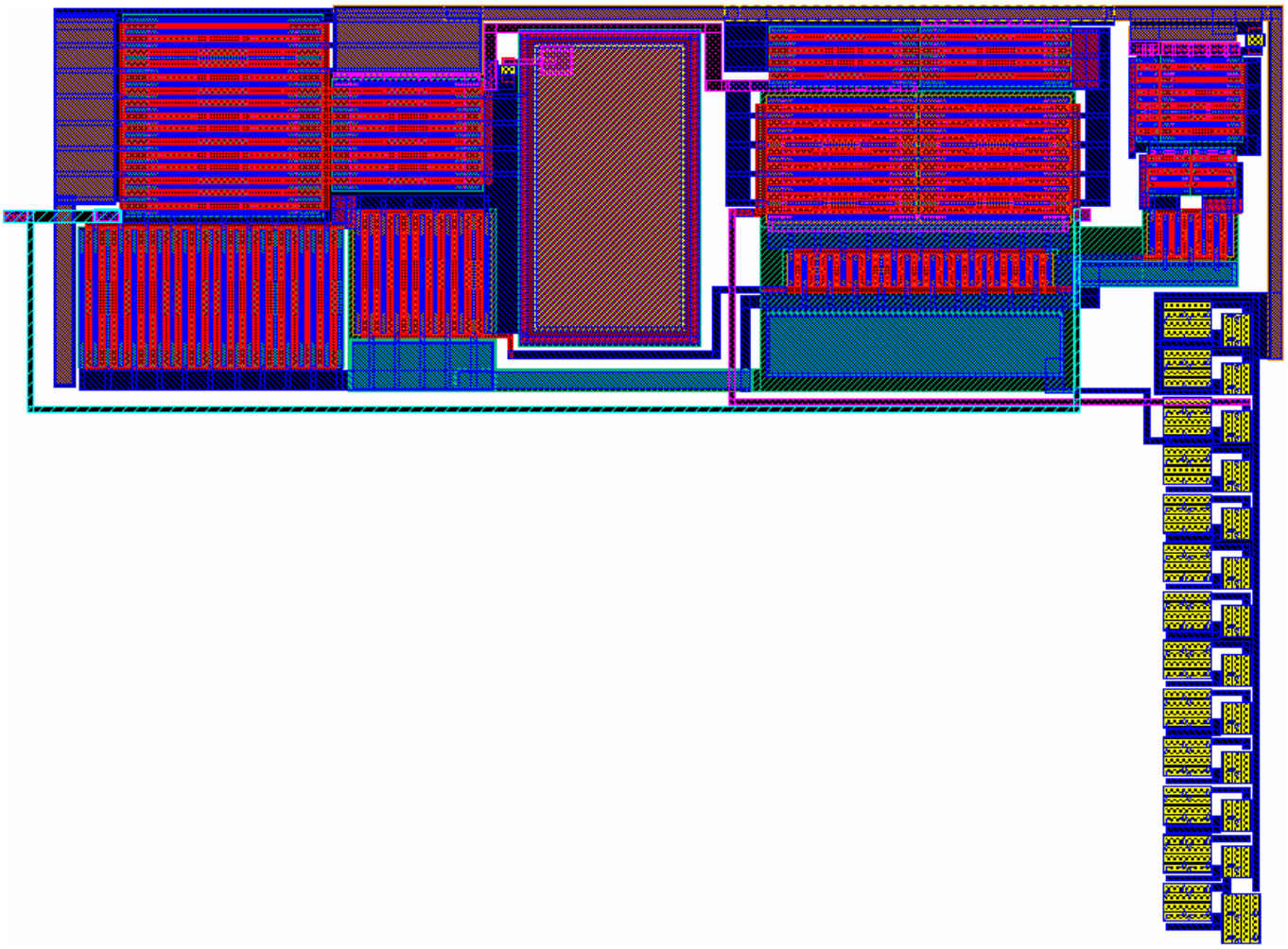

Figure 4.3[1] – Layout of DAC

5 References and Notes

(1) D. A. Johns and Martin, Analog Integrated Circuit Design, *John Wiley*, 1997

(2) R.J.Baker, CMOS Circuit Design, Layout and Simulation, IEEE Press, 2005