12 BIT ACCUMULATOR FOR DDS

ECE547 Final Report

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Chapter 1
Introduction

1.1 Project Overview

Direct digital synthesis (DDS) is a powerful technique used in the generation of radio frequency signals for use in a variety of applications from radio receivers to signals generators and many more. The technique has become far more widespread in recent years with the advances being made in integrated circuit technology that allow much faster speeds to be handled which in turn enable higher frequency DDS chips to be made.

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1.1.1 How It Works

As the name suggests this form of synthesis generates the waveform directly using digital techniques. This is different to the way in which the more familiar indirect synthesizers that use a phase locked loop as the basis of their operation.

A direct digital synthesizer operates by storing the points of a waveform in digital format, and then recalling them to generate the waveform. The rate at which the synthesizer completes one waveform then governs the frequency. The overall block diagram is shown below, but before looking at the details operation of the synthesizer it is necessary to look at the basic concept behind the system.

The operation can be envisaged more easily by looking at the way that phase progresses over the course of one cycle of the waveform. This can be envisaged as the phase progressing around a circle. As the phase advances around the circle, this corresponds to advances in the waveform.

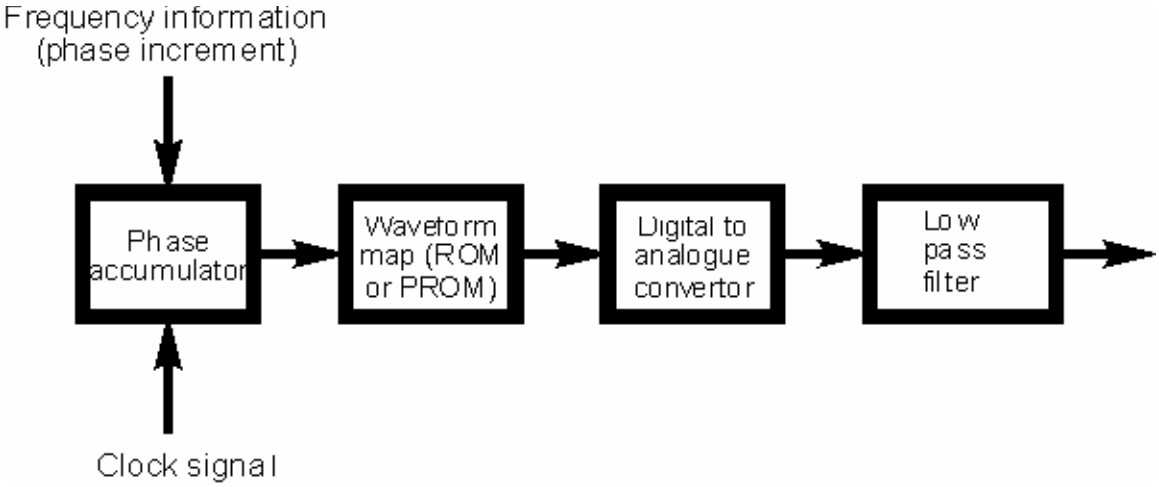

Fig 1. Block Diagram of a Basic Direct Digital Synthesizer (DDS).

The synthesizer operates by storing various points in the waveform in digital form and then recalling them to generate the waveform. Its operation can be explained in more detail by considering the phase advances around a circle as shown in Figure 2. As the phase advances around the circle this corresponds to advances in the waveform, i.e. the greater the number corresponding to the phase, the greater the point is along the waveform. By successively advancing the number corresponding to the phase it is possible to move further along the waveform cycle.

The digital number representing the phase is held in the phase accumulator. The number held here corresponds to the phase and is increased at regular intervals. In this way it can be sent hat the phase accumulator is basically a form of counter. When it is clocked it adds a preset number to the one already held. When it fills up, it resets and starts counting from zero again. In other words this corresponds to reaching one complete circle on the phase diagram and restarting again.

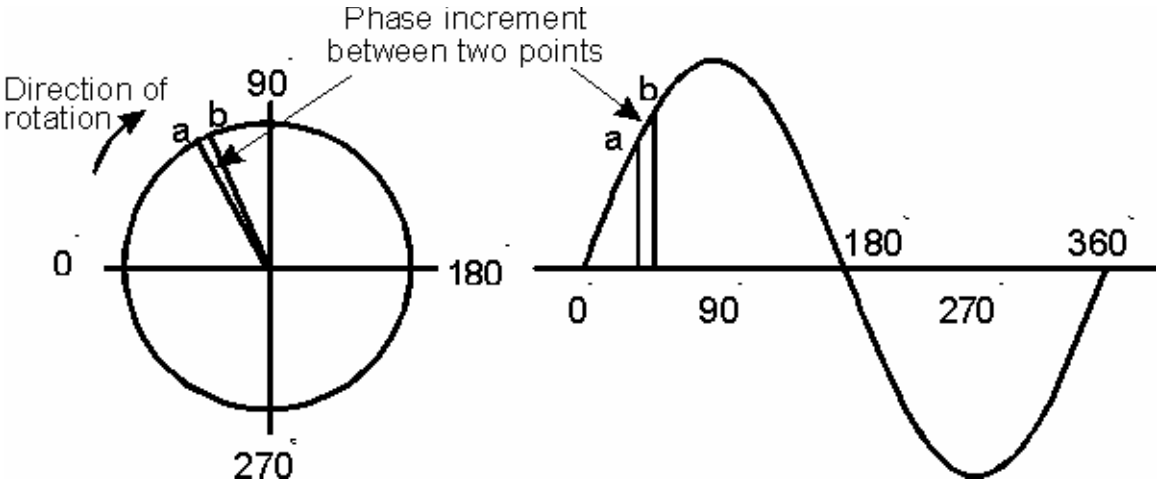

Fig 2. Operation of the phase accumulator in a direct digital synthesizer.

Once the phase has been determined it is necessary to convert this into a digital representation of the waveform. This is accomplished using a waveform map. This is a memory which stores a number corresponding to the voltage required for each value of phase on the waveform. In the case of a synthesizer of this nature it is a sine look up table as a sine wave is required. In most cases the memory is either a read only memory (ROM) or programmable read only memory (PROM). This contains a vast number of points on the waveform, very many more than are accessed each cycle. A very large number of points is required so that the phase accumulator can increment by a certain number of points to set the required frequency.

The next stage in the process is to convert the digital numbers coming from the sine look up table into an analogue voltage. This is achieved using a digital to analogue converter (DAC). This signal is filtered to remove any unwanted signals and amplified to give the required level as necessary.

1.2 Objective

The objective of this project is to design, simulate and document a 12-bit digital accumulator (12BDA).The 12-bit digital accumulator (12BDA) will operate at a power supply of 5V and a clock frequency of 50 MHz with minimum power consumption. The 12BDA is the most critical part concerning the speed of DDS throughput, thus we will need to design the 12BDA with the fastest possible speed.

Chapter 2
Circuit Design

2.1 Design Objective

The goal of this project is to design, simulate and document a 12-bit digital accumulator (12BDA). The 12BDA will operate at 5V, power supply and at a clock frequency of 50 MHz.

2.2.1 Problem Statement

An accumulator consists of adders and data storage registers e.g. Flip-Flop (FF). Typical accumulator operates at the speed of 10-30MHz and this speed limitation is due to the propagation delay of the adders.

Since we will use this 12 BDA in DDS at an operating frequency 50 MHz and one of the slowest parts of DDS is the adder in digital accumulator, we need to design a faster respond adder.

The operational speed of FF determines the correctness and accuracy of the functionality of 12BDA. To ensure the 12BDA is error-free, FF in the 12BDA is able to operate at the clock frequency rate or higher. This ensures that FF can correctly capture and store every incoming data.

2.2.2 Design Specifications

The 12BDA will under the following conditions:

- Operating clock frequency of 50 MHz
- Supply voltage of 5V

2.2.3 Pipelining

Pipeline is to divide a big stage in smaller independent combinatorial sub-stages (or sub-tasks), that works at the same time on a part of the throughput. In every sub-stage, a register stores the result of the previous sub-stage and feeds it to the following stage at the following clock pulse. Many existing DDFS systems include pipelined accumulator architecture, which improves throughput over a simple adder based accumulator. The maximum update rate of a pipelined accumulator is limited by the time it takes for the carry to propagate through the adder in the system. The size of the largest adders can be reduced by subdividing the accumulator further. This is done at the cost of increasing the number of pipeline stages and the number of D-type flip flops. The DFFs account for 95% of the total accumulator power consumption. I have implemented pipelining in my design to overcome the propagation delay due to adders. I have designed my 12 bit accumulator by pipelining three 4 bit accumulators.

2.2.4 Basic CMOS Gate Sizing

Transistor sizing is the process of specifying the widths of the transistors in logic gates. Device sizes control the rise and fall propagation delays in CMOS. This is the primary reason to specify the sizes of the transistors. To obtain approximately equal rise and fall delays, we found that the PMOS devices must be roughly twice the size of the NMOS device.

For a NAND gate there are 2 parallel PMOS devices and 2 series NMOS devices. Since the 2 PMOS devices are in parallel we assume that only one is on and the other is off during pull-up phase. Each pull up should be sized to 2W where W =1.5 micrometer.

Next consider two pull down transistors that are in series. Since both transistors must be on to pull the output low, we will see roughly twice the resistance if they are sized 2W and W. So we double the widths to cut resistance in half. Thus the two transistors are of 2W.

Similar considerations apply for NOR gates. Both NMOS devices should be set to W to match pull down delay. The PMOS devices should be doubled (2W) as they are in series. Given below is the figure showing device sizing for a NAND gate.

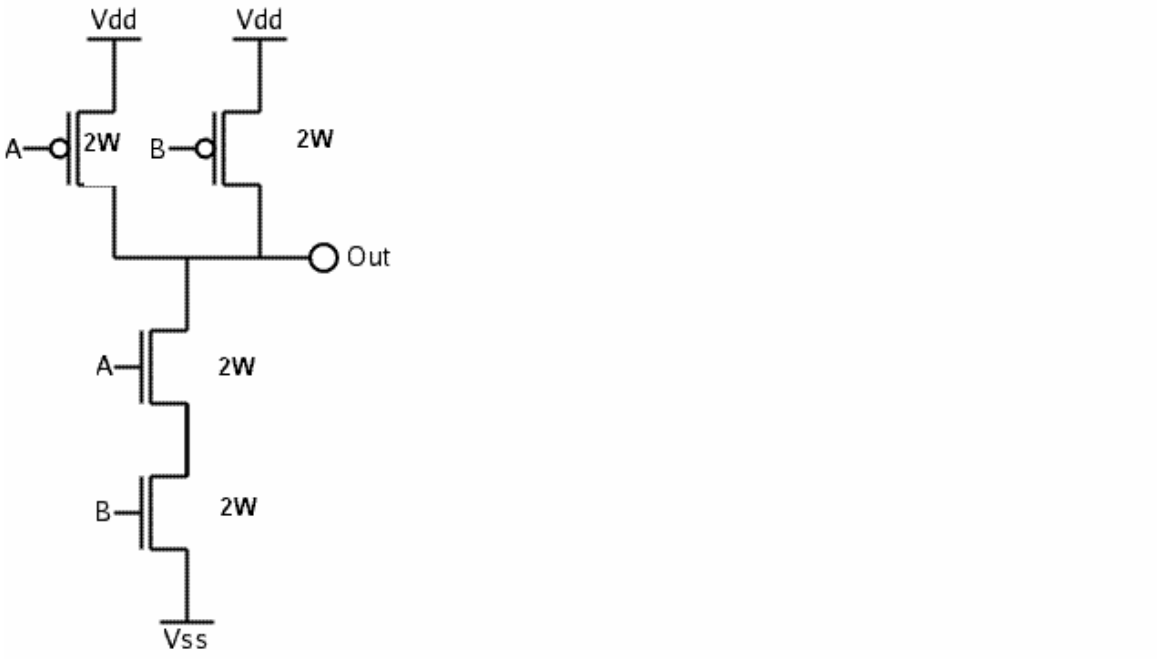

Fig 3. Device sizing for CMOS NAND gate.

2.2.5 Basic Logic Circuits

2.2.5.1 Inverter

The most important CMOS gate is the CMOS inverter. It consists of only two transistors, a pair of one N-type and one P-type transistor. The transistors are sized. The schematic is shown below.

If the input voltage is '1' (Vdd) the P-type transistor on top is nonconducting, but the N-type transistor is conducting and provides a path from ground to the output. The output level therefore is '0'. On the other hand, if the input level is '0', the P-type transistor is conducting and provides a path from VDD to the output, so that the output level is '1', while the N-type transistor is blocked.

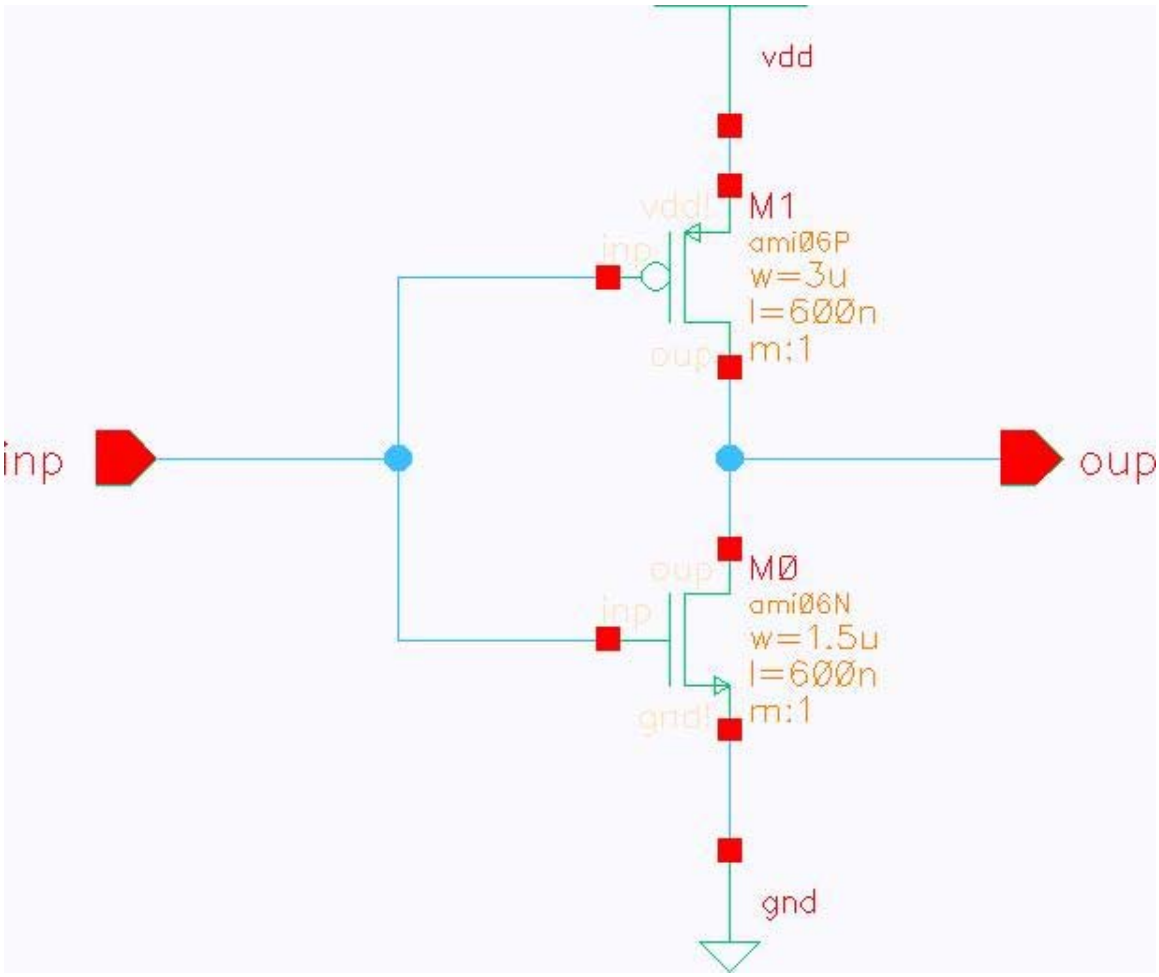

Fig 4. Schematic of a CMOS INVERTER

2.2.5.2 2-input NOR gate

The 2-input NOR gate is the simplest CMOS gate to illustrate the name *complementary* MOS: The P-type transistors are connected in series between Vdd and the output, while the N-type transistors are connected in parallel between ground and the output. That is, the N-type and the P-type parts of the CMOS gate are complementary (in respect to topology, and therefore function).

Only if both inputs are '0' (corresponding to ground), there is a conducting path from Vdd to the output (output level '1'). An input combination with either of the inputs '1' blocks the path from VCC to the output, but opens a path from ground to the output (so that the output level is '0').

The schematic is shown below.

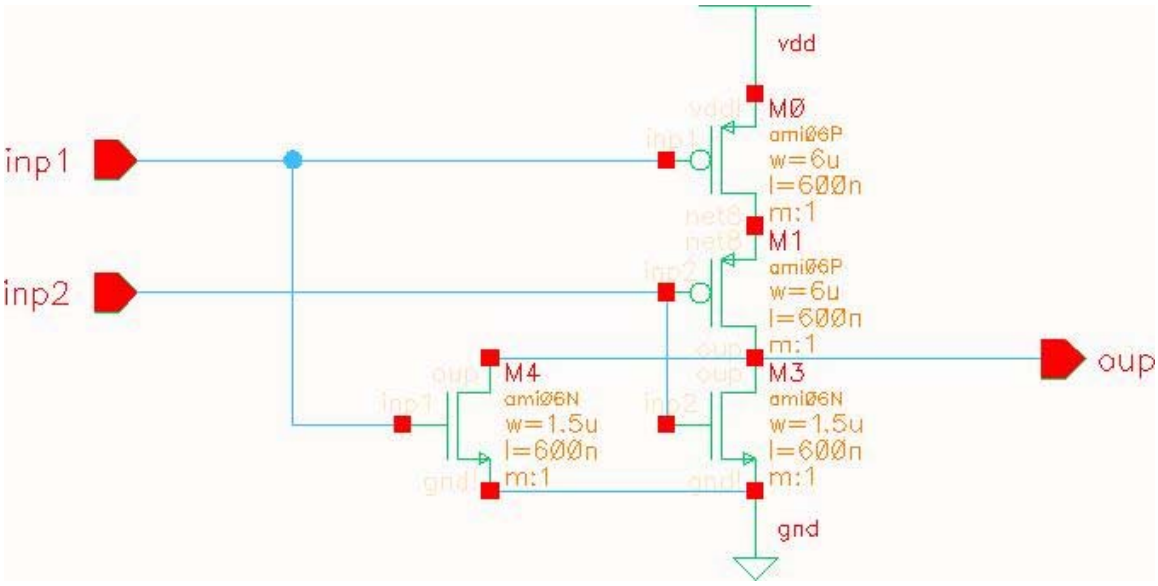

Fig 5. Schematic of a 2-input NOR gate

2.2.5.3 2-input NAND gate

In the two-input NAND gate the P-type transistors are connected in parallel between Vdd and the output, while the N-type transistors are connected in series from ground to the output. Schematic is given below.

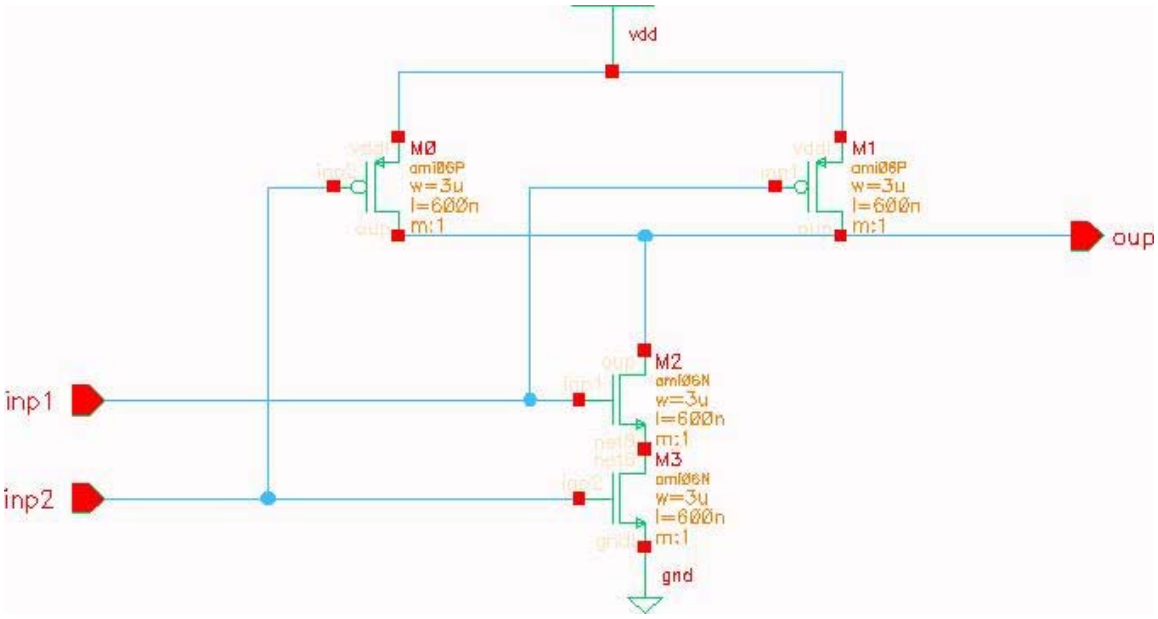

Fig 6. Schematic of a 2-input NAND gate

2.2.5.4 2-input AND gate

The AND gate is obtained by connecting an inverter to the output of the NAND gate. Schematic is given below.

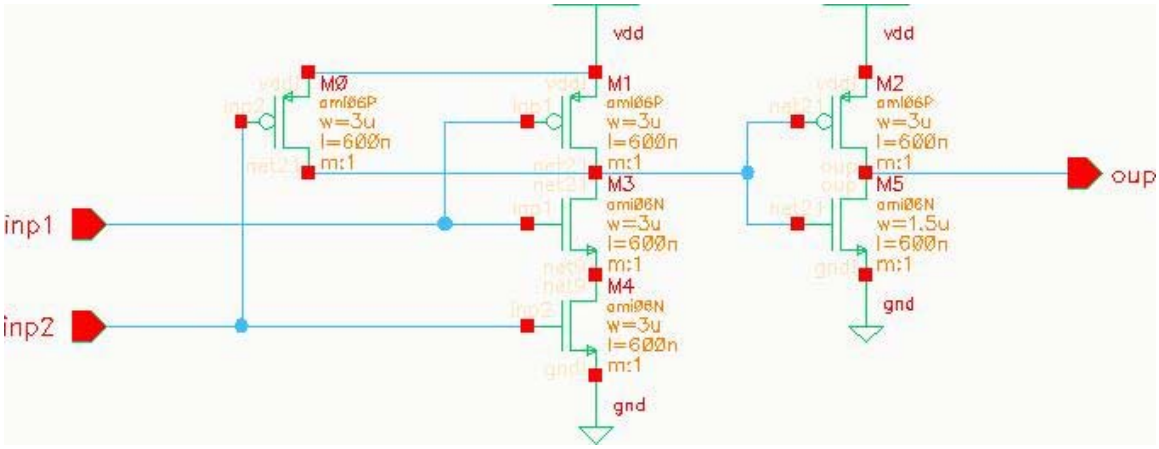

Fig 7. Schematic of a 2-input AND gate

2.2.5.5 2-input OR gate

OR gate is also nothing but an inverter connected to the output of a NOR gate. Schematic is shown below.

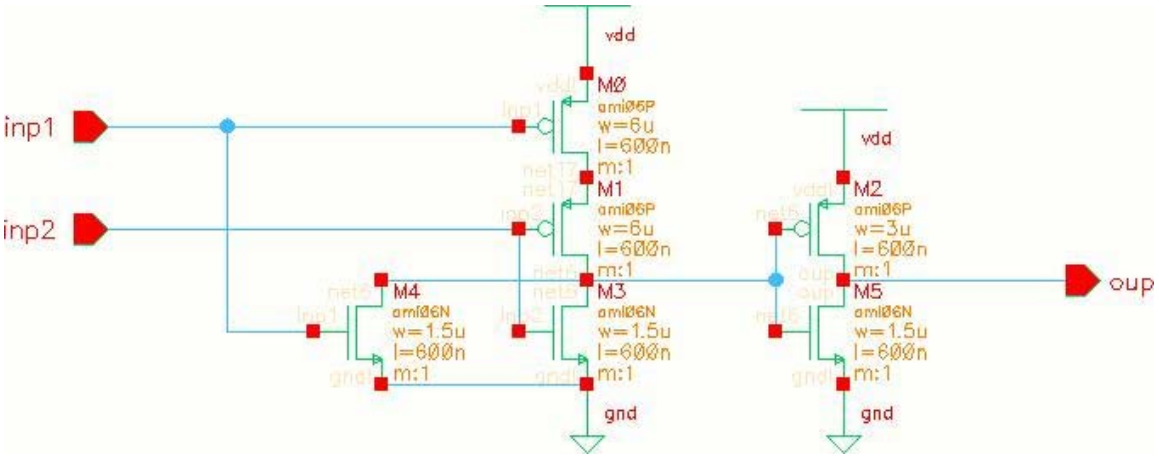

Fig 8. Schematic of a 2-input OR gate

2.2.5.6 2-input XOR gate

XOR is a 'stricter' version of the OR gate. Rather than allowing the output to be HIGH when either one or both of the inputs are HIGH, an XOR gate has a HIGH output only when only *one* input is HIGH. This can also be interpreted (for a two-input gate) as "HIGH output when the inputs are different". The schematic of a 2 input XOR gate is shown below. The output of the gate is given by

oup = inp1⊕ inp 2

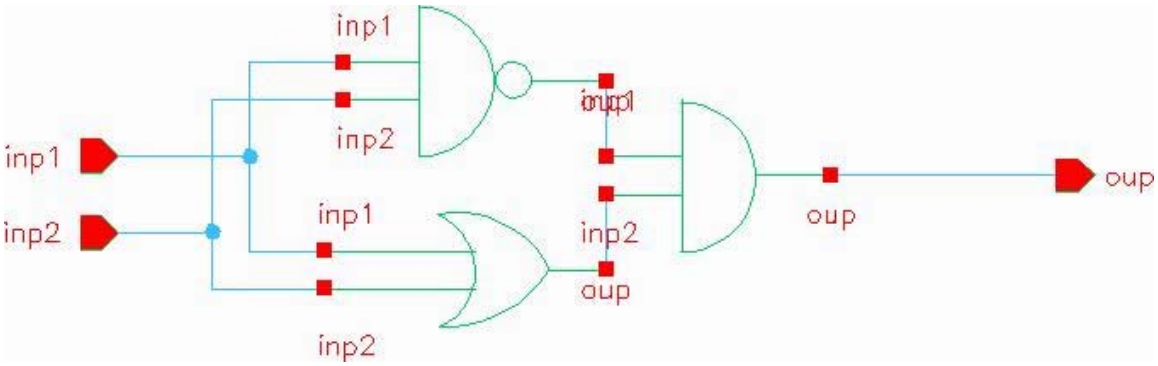

Fig 9. Schematic of a 2-input XOR gate

2.2.5.7 D Flip Flop

A flip flop is a storage device, which holds some data within a clock period. There are some points that we need to consider when we designed the flip flop. We had to pay attention to the clock distribution in order to minimize the clock skew, the fault output signal of the clock. Clock speed is 50MHz and so the signal lost is kept to a minimum.

A flip flop always includes a latch as a signal storage module. I have used a two D latches in a master-slave configuration driven by a clock. It is designed to operate as a positive edge-triggered D-flip flop. Its operation is shown in the graph below.

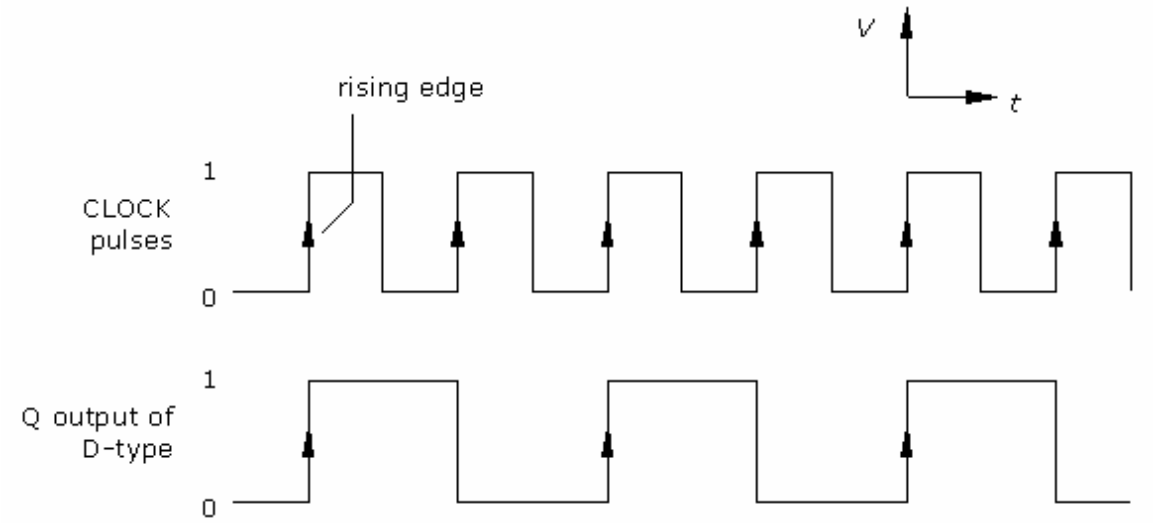

Fig 10. D flip flop operation

The schematic of the DFF is shown below.

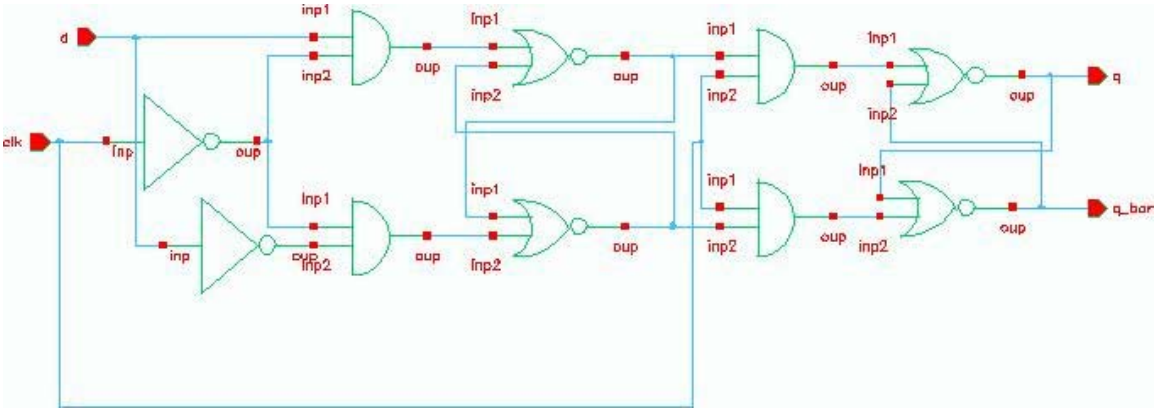

Fig 11. Schematic of a rising edge D flip flop

2.2.5.8 Full adder

As mentioned before, an adder is a very important design because it is the module which affects the speed of the accumulator. In our accumulator, we will use a single-bit adder to do the accumulation because it is the most generally and commonly used adder which is easily to be understood. Moreover, it has a small size.

An implementation of an adder is shown below:

S=A ⊕ B ⊕ Cin

Cout=AB+ (A ⊕ B) Cin

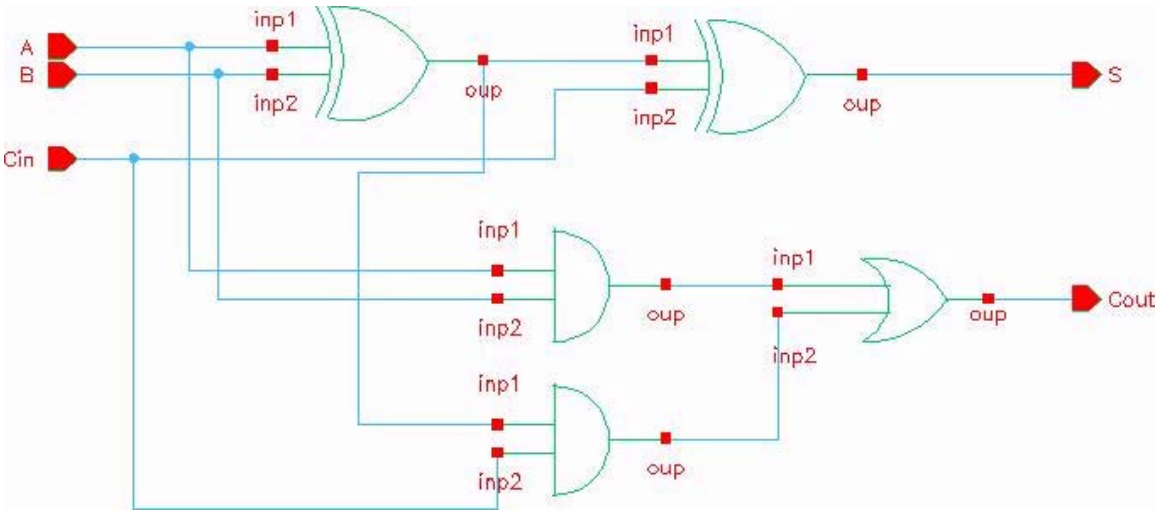

Fig 12. Schematic of a Full Adder.

2.2.6 4 Bit Accumulator

The 4 Bit accumulator is designed using 4 full adders and 5 DFFs. The output is obtained at the end of every clock cycle. The output of the first 4 DFFs are given back to the input of the corresponding adder in order for accumulation to take place. Notice that the carry out bit of the first adder is given to the carry in bit of the second stage and this continues till the last stage. The carry out bit of the last adder is given to the DFF. This is done to ensure that while pipelining three of these 4 bit accumulators, the carry bit of one stage is sent to the carry bit of the next stage in exactly one clock cycle.

The schematic of the 4 bit accumulator is shown below.

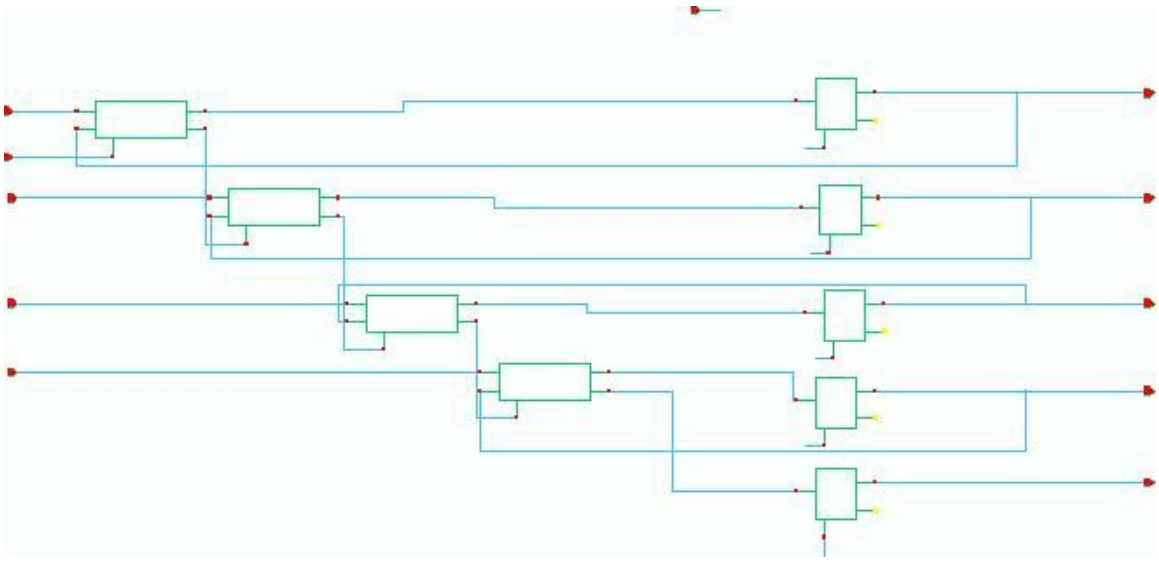

Fig 13. Schematic of 4 Bit Accumulator.

2.2.7 12 Bit Pipelined Accumulator

12 bit accumulator is one of the most important significant parts in the DDS design. I have designed a 12 bit pipelined accumulator that works at a clock frequency of 50 MHz. Since I have implemented pipelining in my design, my accumulator can work up to a clock frequency of 150 MHz. The power drawn by the accumulator is 2 mW. This will be discussed in the next section.

I have designed my 12 bit accumulator by pipelining three 4 bit accumulators. The schematic of 12 bit pipelined accumulator is shown below.

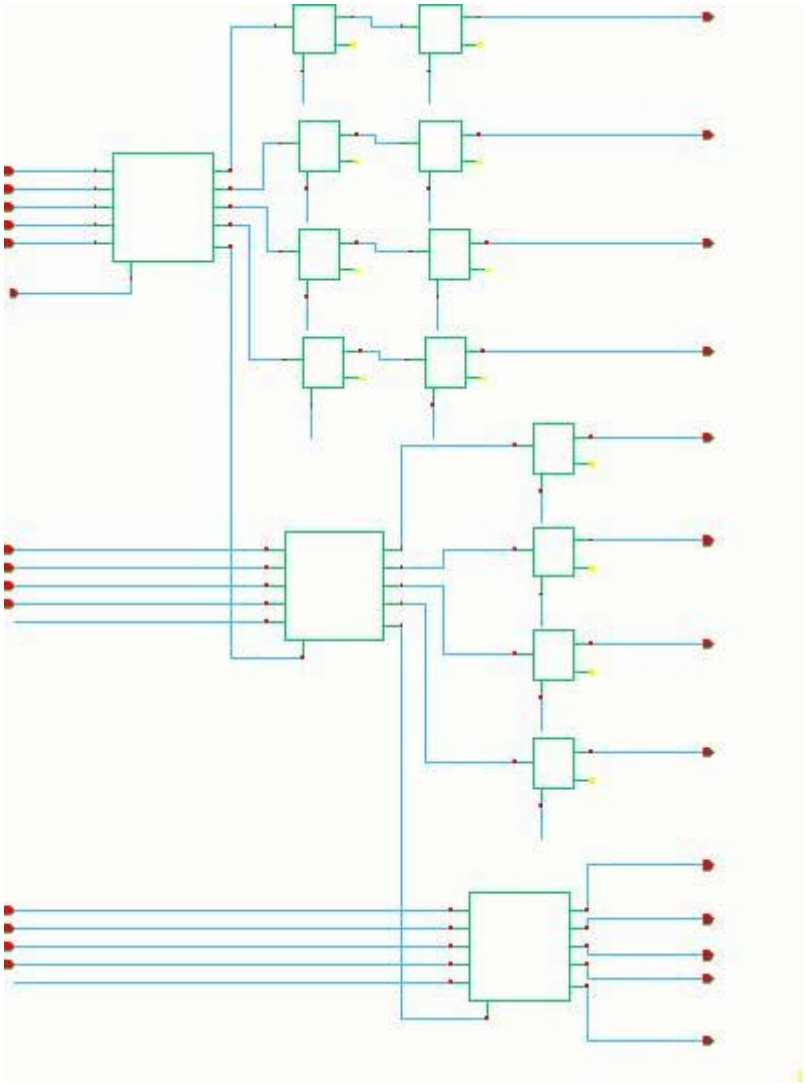

Fig 14. Schematic of 12 Bit Accumulator.

Notice that the each of the output of the topmost accumulator block is connected to 2 DFFs. The outputs of the second block are connected to 1 DFF each and the third block is not connected to any flip flop. The carry out of each 4 bit block is connected to the output of the next. I will explain why I did so.

The topmost input is the least significant bit and the bottommost is the most significant. On the first clock cycle we get the output of the first accumulator block. The carry out of the first block is connected to the carry in of the next block. On the second clock cycle, the carry out of the second block is passed into the carry in of the third. At the end of the first clock cycle we get the output at the first accumulator block. The output of the second accumulator is obtained at the end of the second clock cycle and the third block at the end of the third clock. I have used DFFs to synchronize the outputs of different accumulator blocks so that outputs of all the blocks are obtained at the end of the third clock.

Given below is a step function obtained when the 12 bit accumulator is connected to the DAC. After 1 full accumulation cycle, a new cycle begins.

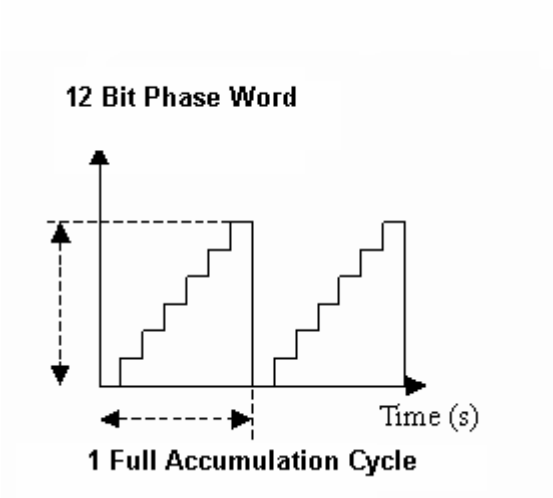

Fig 15. Accumulation Cycle.

Chapter 3
Simulation Results

3.1 Simulation Result

Simulation plays a crucial role in designing circuits. Schematic simulation was performed on both 12 bit accumulator and 4 bit accumulator to verify functionality. As the clock frequency is only 50 MHz and since the accumulator design unlike the DAC is not very much layout dependent, layout simulation does not play a crucial part in my design.

3.2 Simulation Result for 4 Bit Accumulator

Given below is the schematic for testing the 4 Bit Accumulator and corresponding waveform. The input given for testing is 0011 where the least 2 significant bits are given to be 1.The accumulation takes place in increments of four.

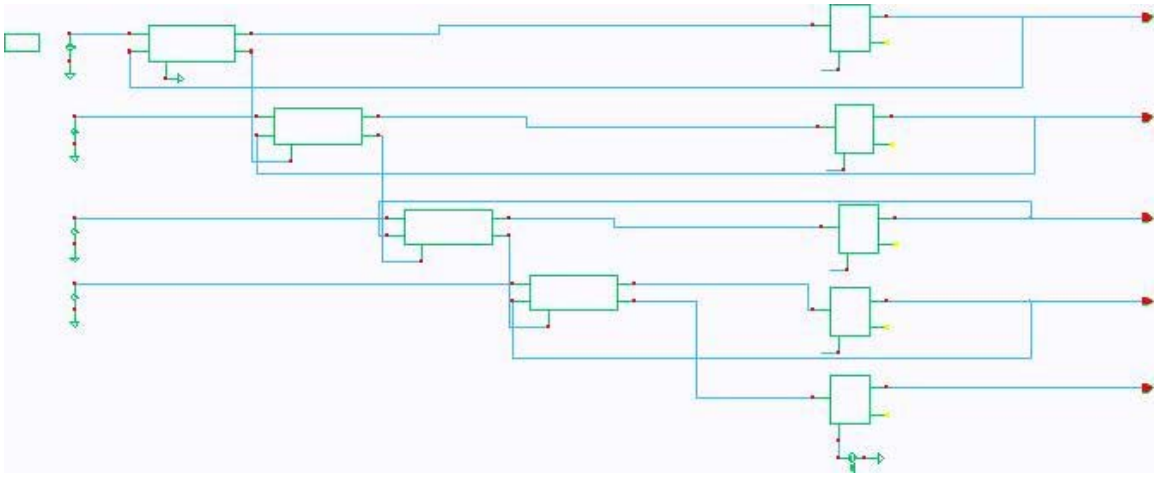

Fig 16. Testing of 4 Bit Accumulator.

Fig 17. Output waveform of 4 Bit Accumulator.

3.3 Simulation Result for 12 Bit Accumulator

The schematic for testing the 12 bit accumulator along with the output waveform is given in this section.

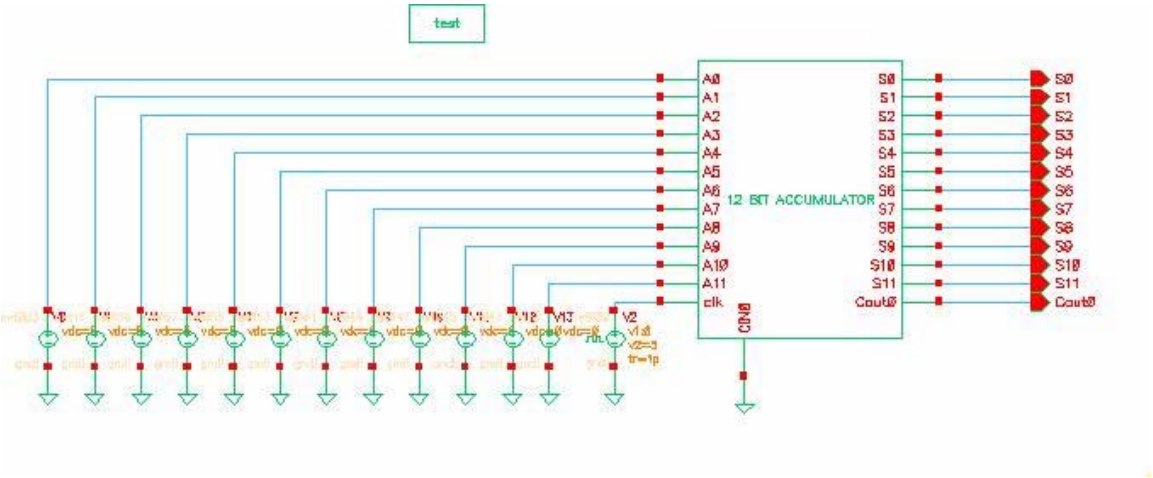

Fig 18. Testing of 12 Bit Accumulator.

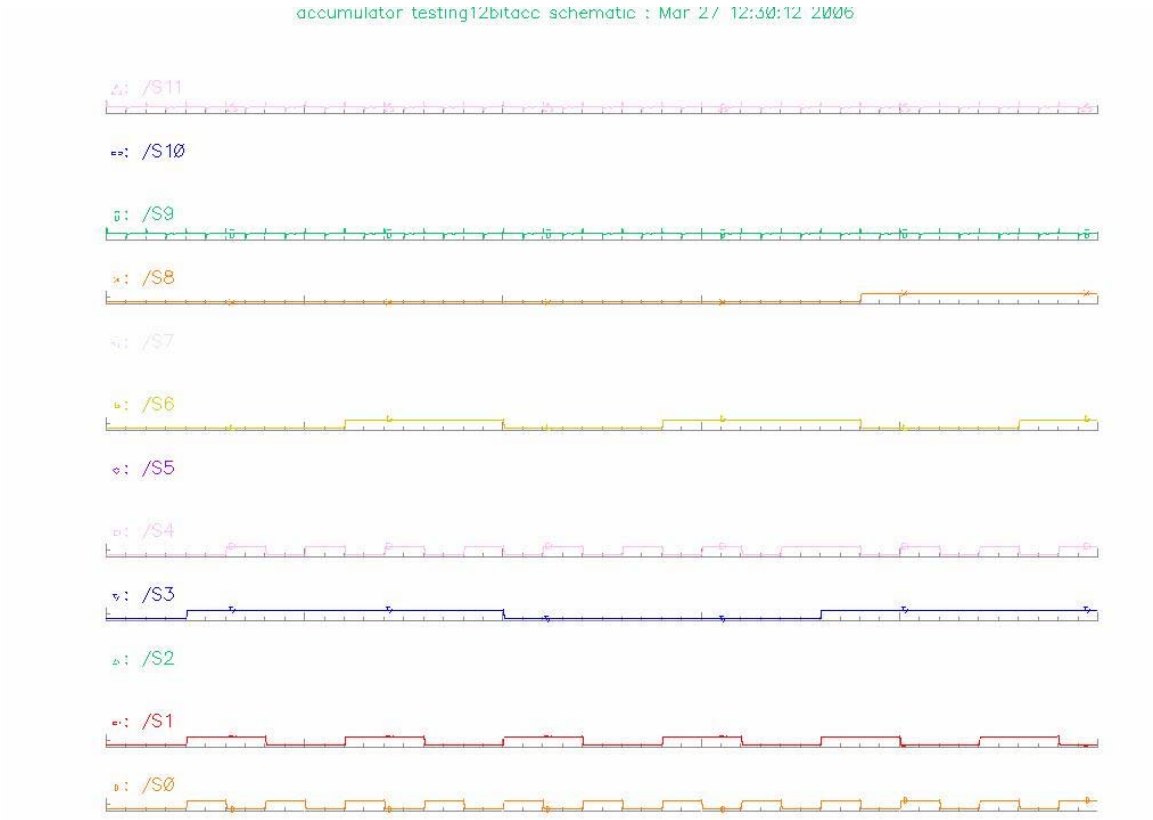

Fig 19. Output Waveform of 12 Bit Accumulator.

Chapter 4
Layout And Extracted Views

The Layout and Extracted views of the circuit elements are shown.

4.1 Inverter

Layout and Extracted views for an inverter are shown below.

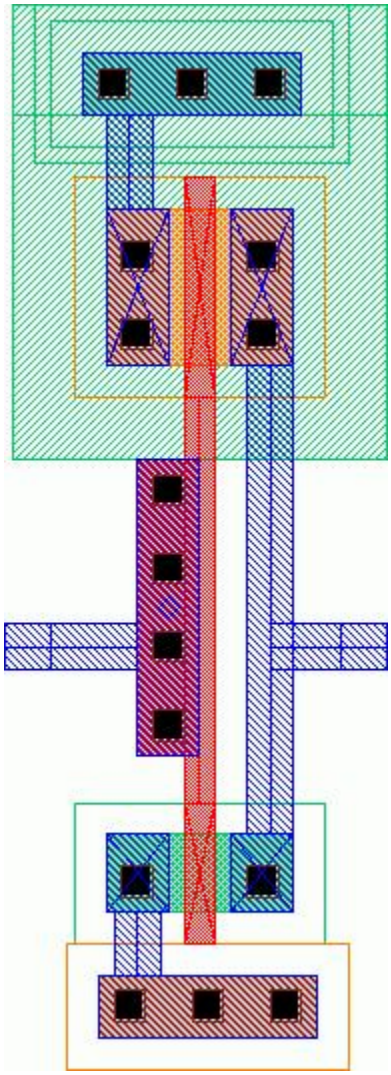

Fig 20. Layout of Inverter.

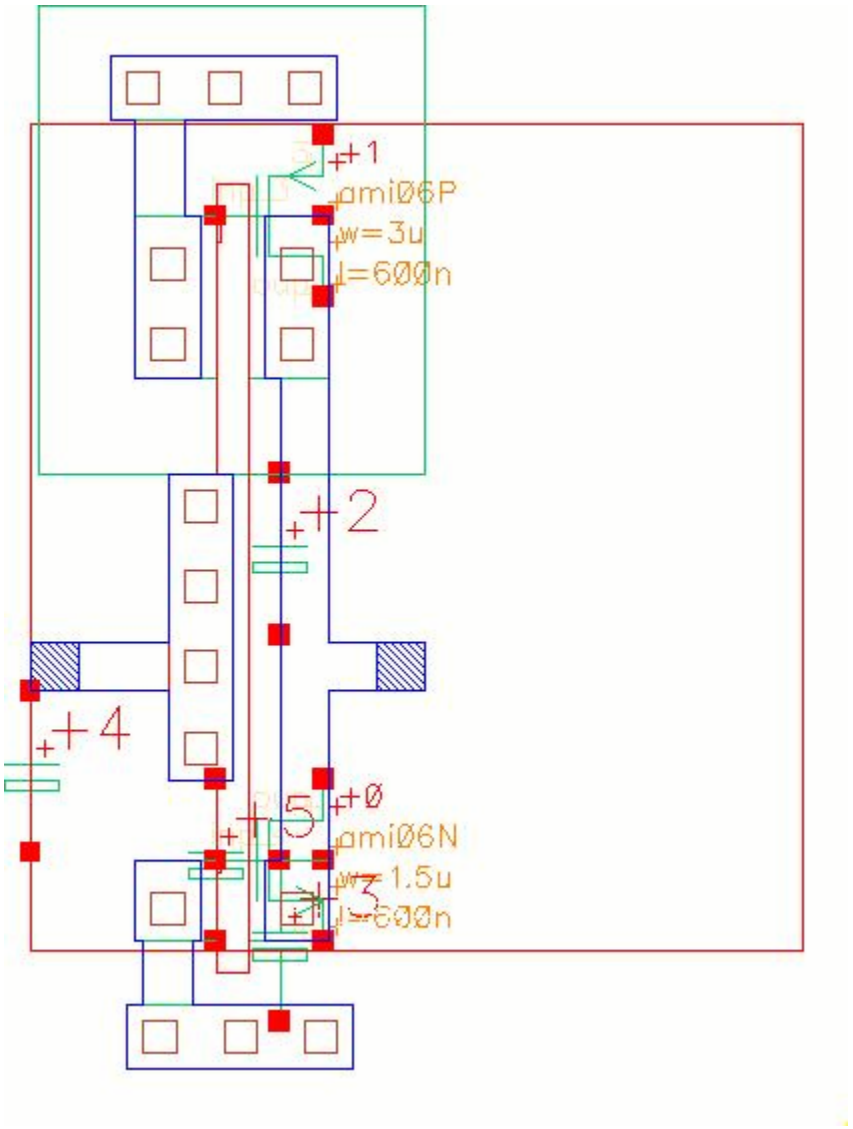

Fig 21. Extracted View Of Inverter.

4.2 2-Input NOR gate

Shown below are the Layout and Extracted views of a 2 input NOR gate.

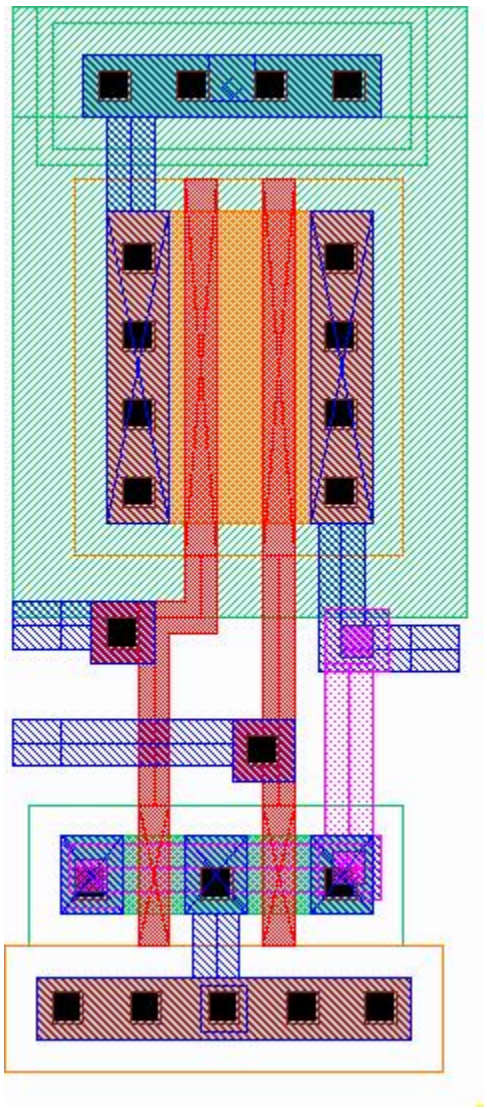

Fig 22. Layout of 2 input NOR gate

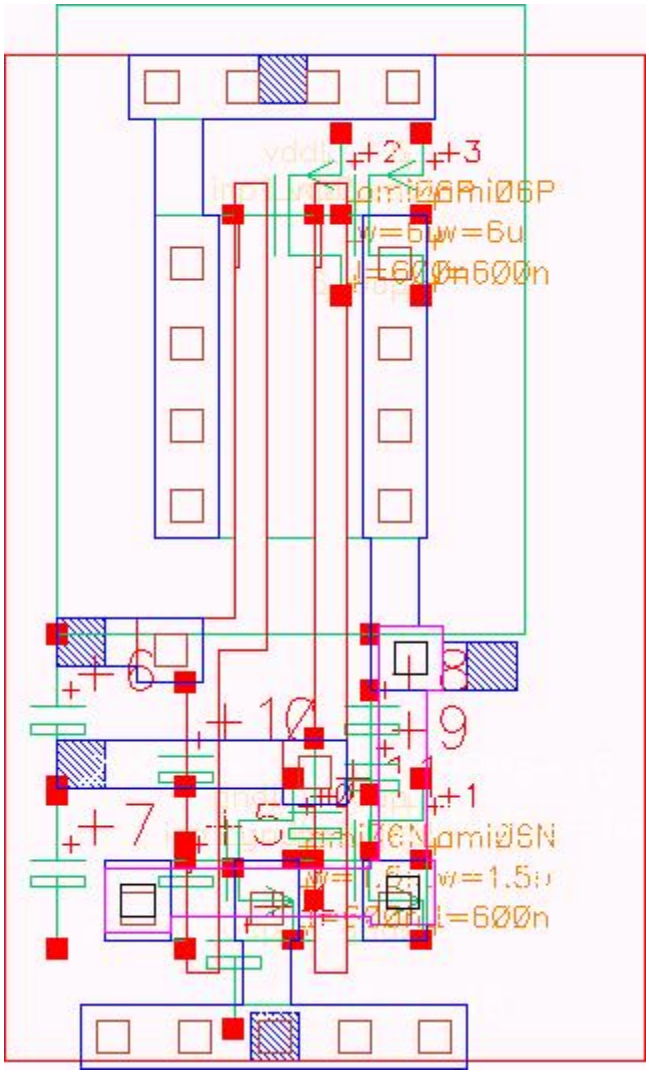

Fig 23.Extracted view of 2 input NOR gate

4.3 2-Input NAND gate

The Layout and Extracted views for a 2 input NAND gate are shown below.

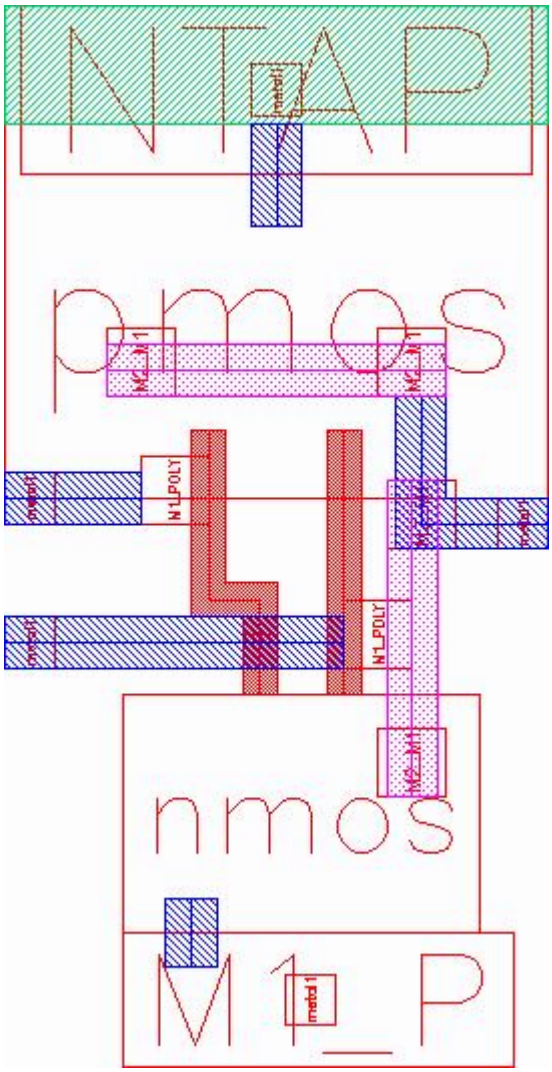

Fig 24. Layout of 2 input NAND gate

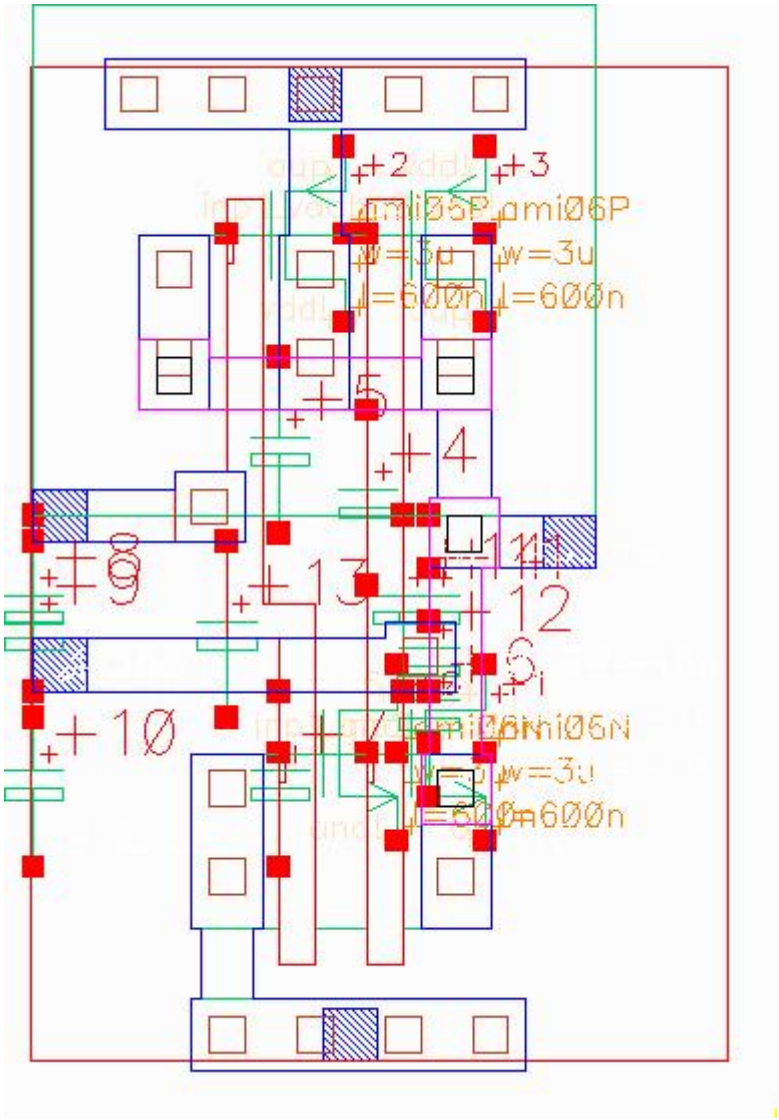

Fig 25.Extracted view of 2 input NAND gate

4.4 2-Input AND gate

The Layout and Extracted views for a 2 input AND gate are shown below.

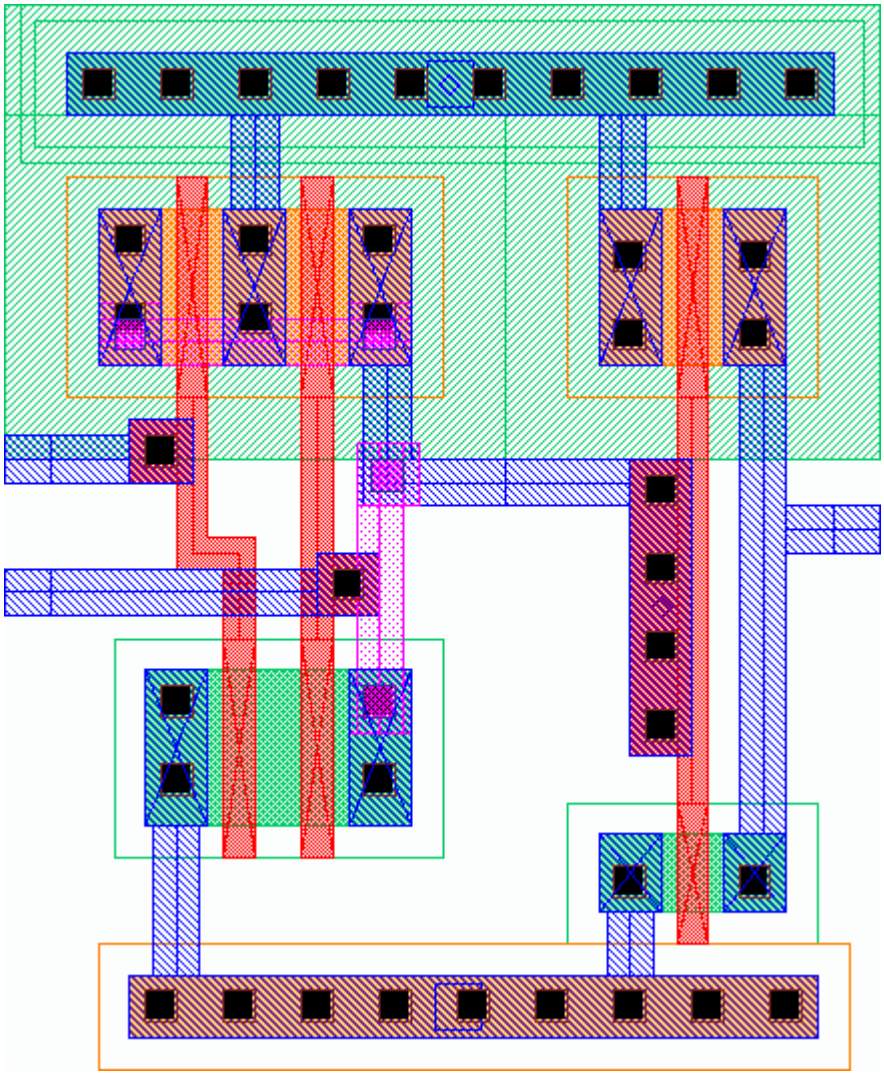

Fig 26. Layout of 2 input AND gate

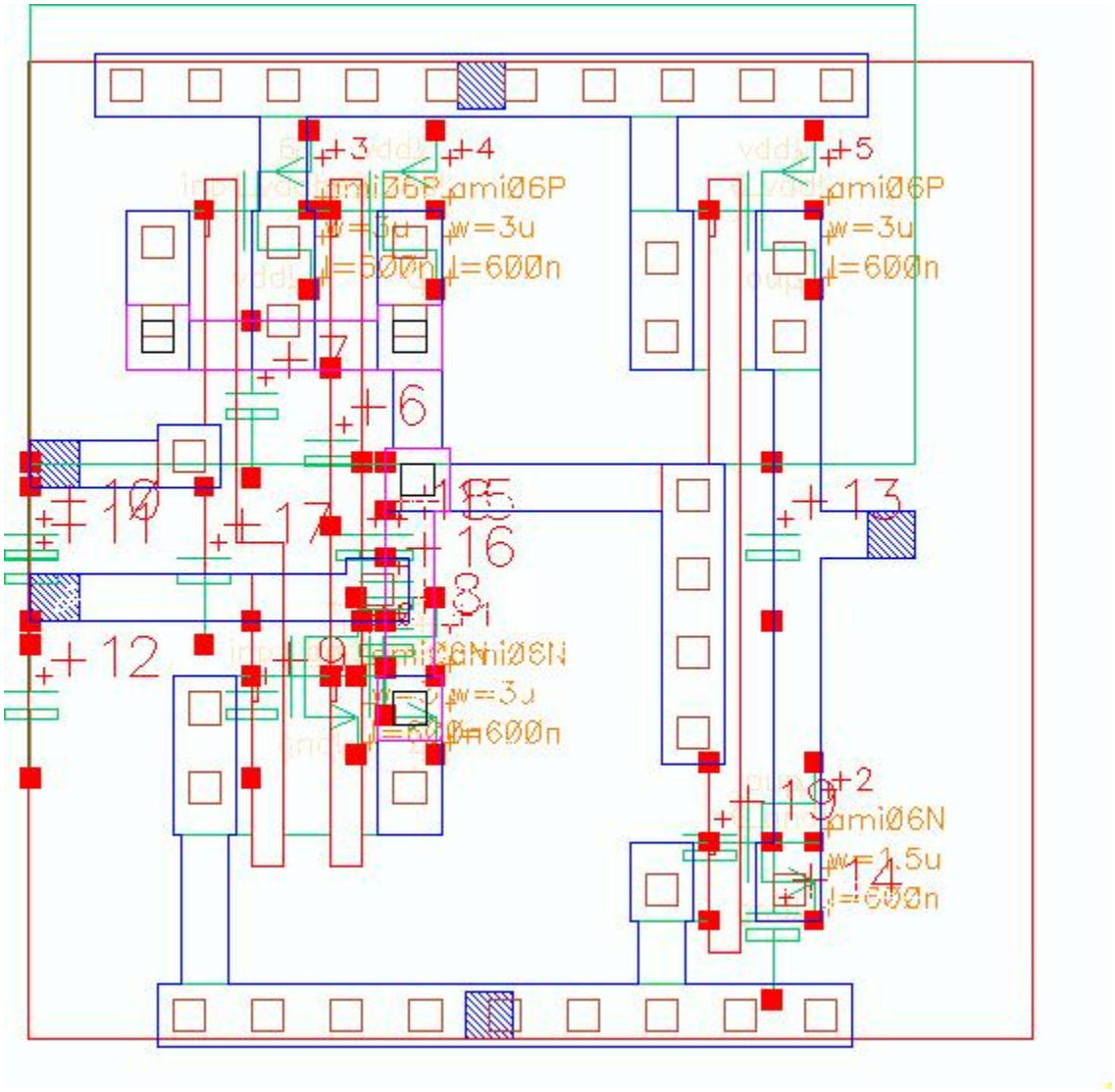

Fig 27. Extracted view of 2 input AND gate

4.5 2-Input OR gate

Shown below are the Layout and Extracted views of a 2 input NOR gate.

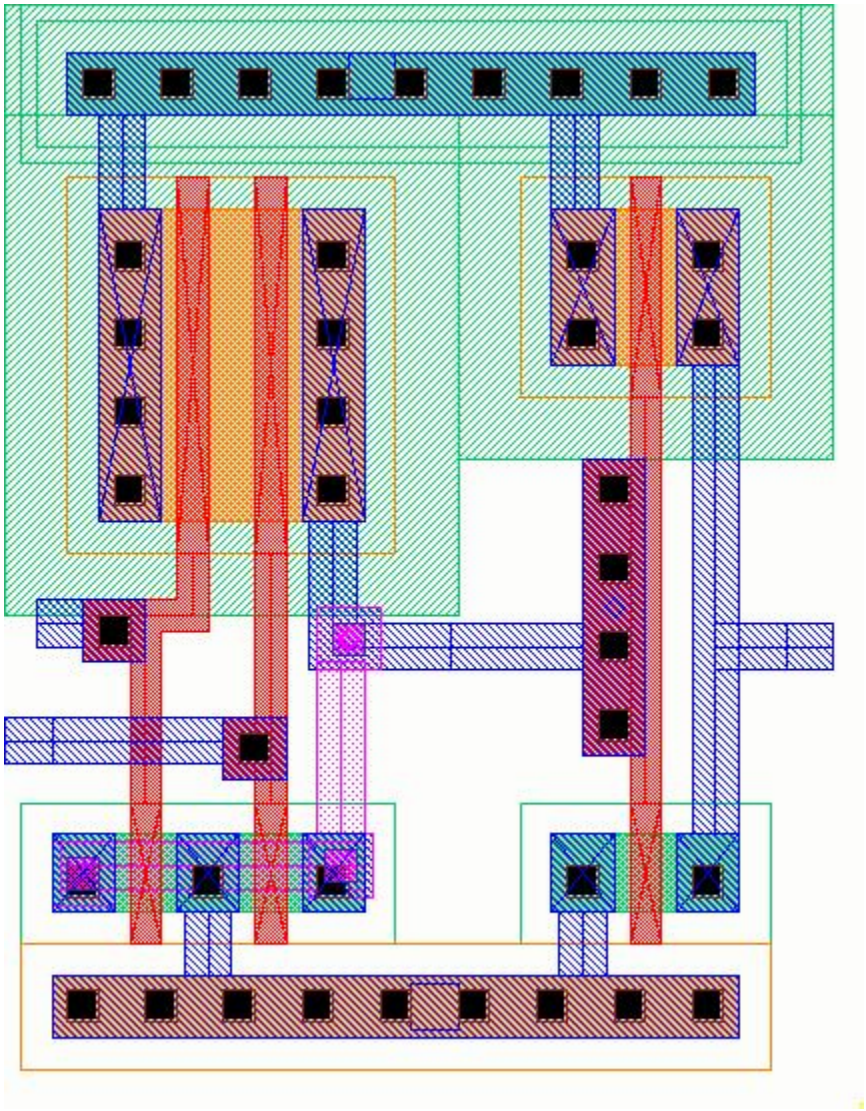

Fig 28. Layout of 2 input OR gate

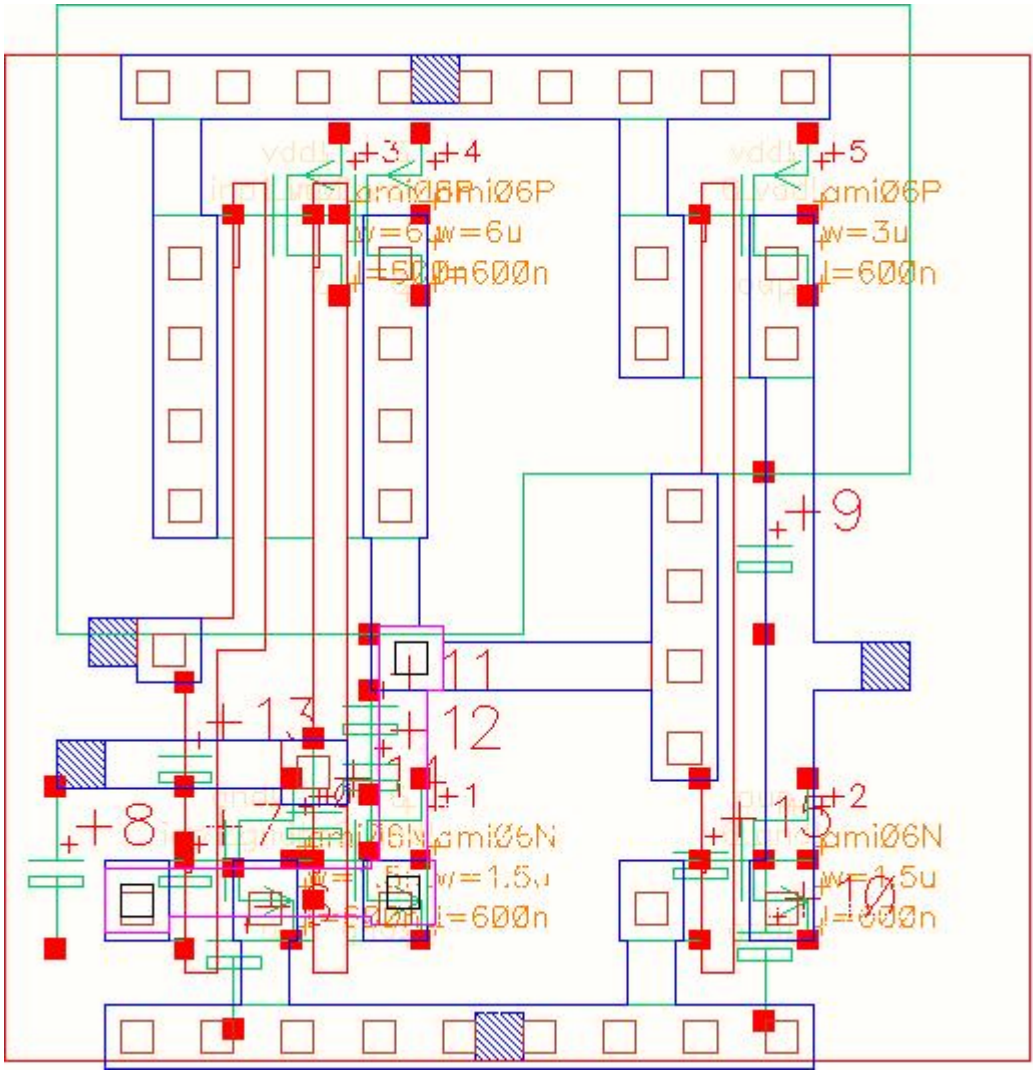

Fig 29. Extracted view of 2 input OR gate

4.6 2-Input XOR gate

The Layout and Extracted views for a 2 input XOR gate are shown below.

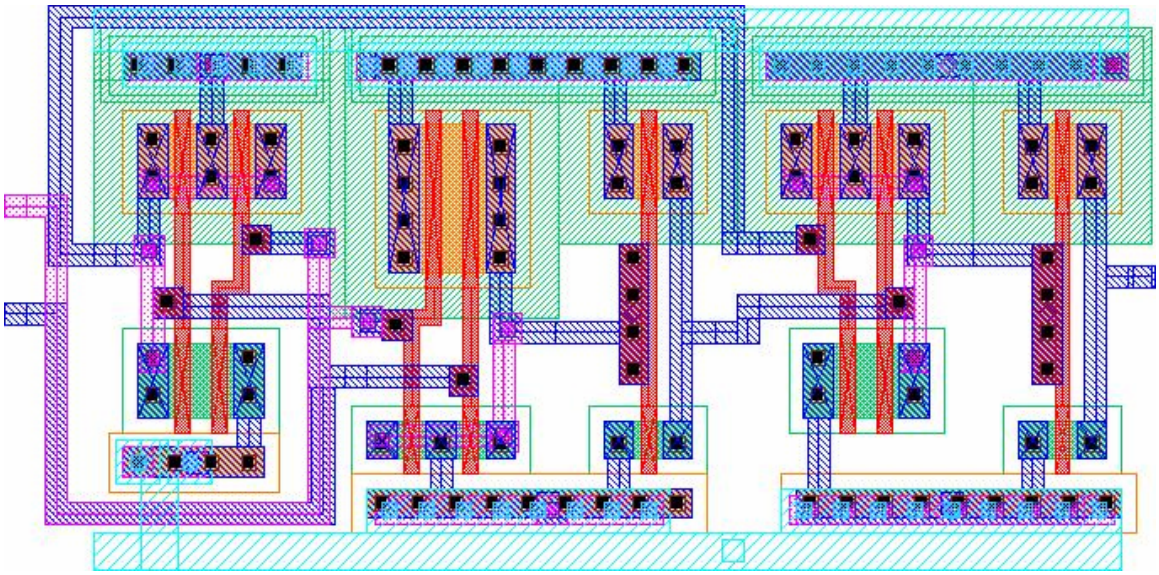

Fig 30. Layout of 2 input XOR gate

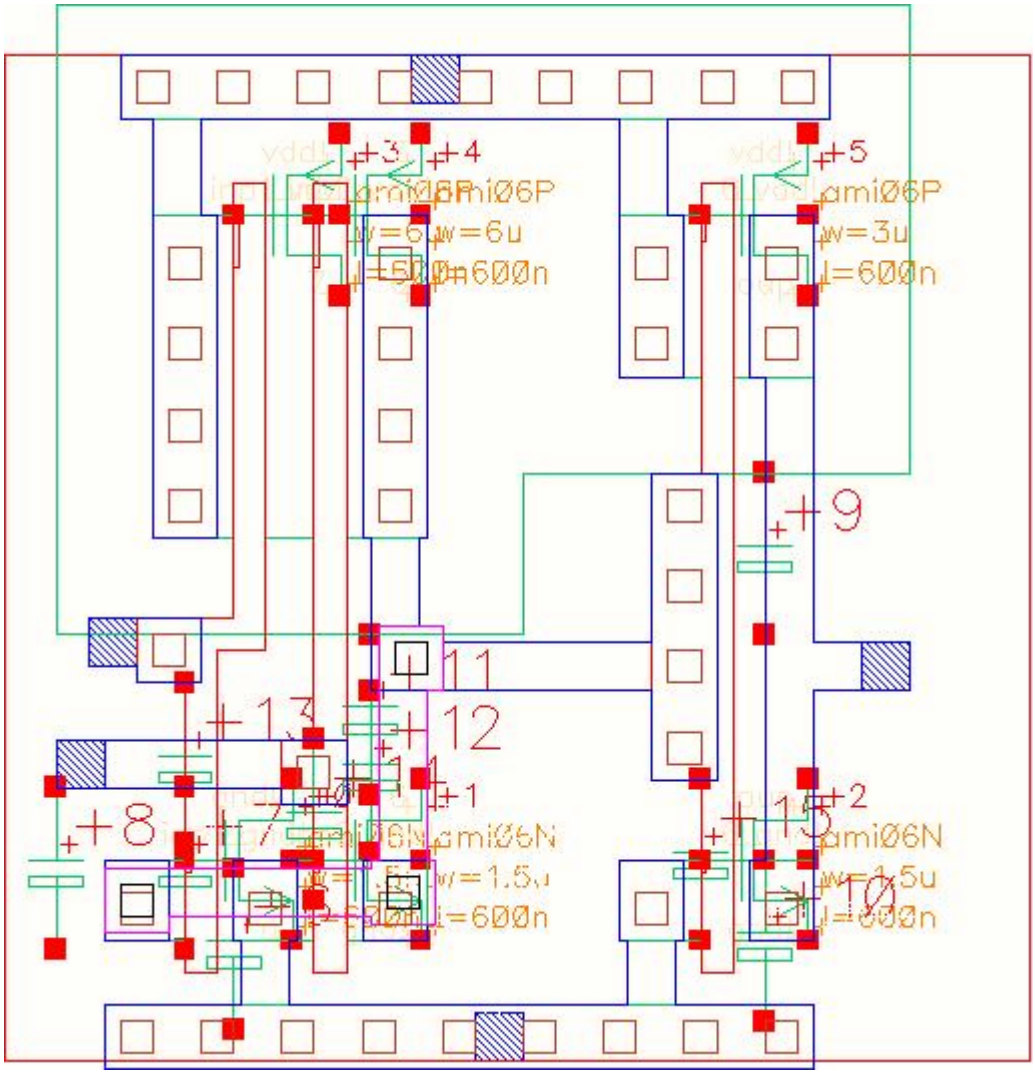

Fig 31. Extracted view of 2 input XOR gate

4.7 D Flip Flop

The Layout and Extracted views for a D Flip Flop are shown below.

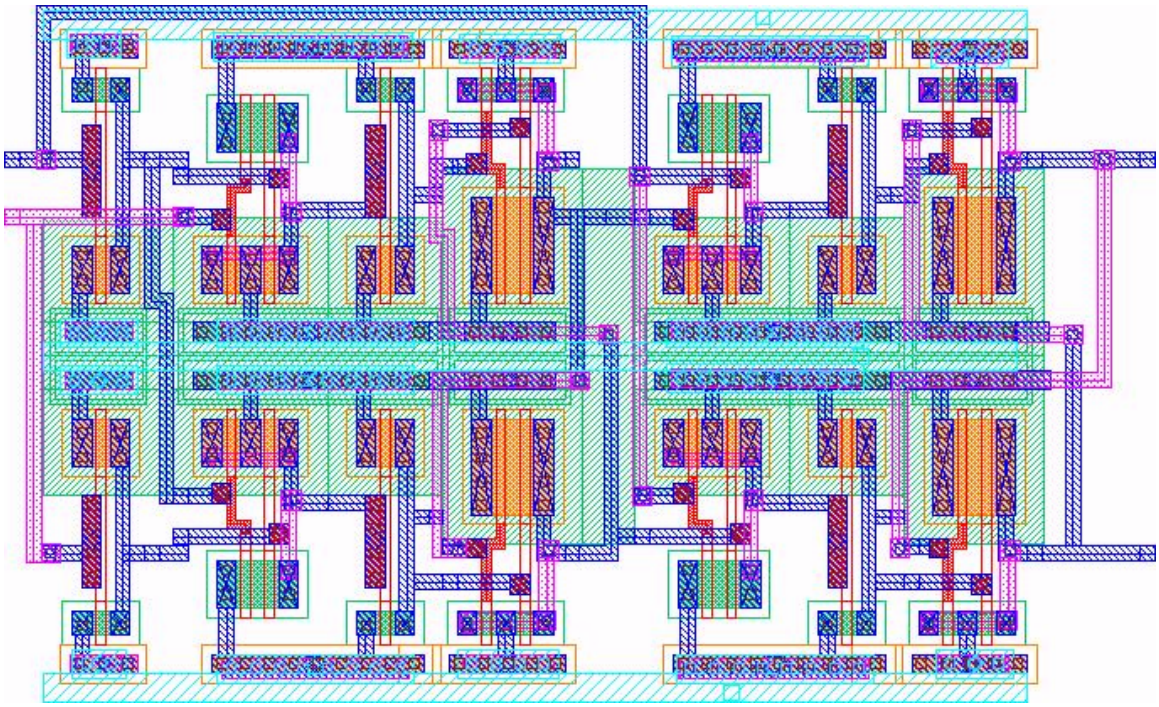

Fig 32. Layout of D flip flop

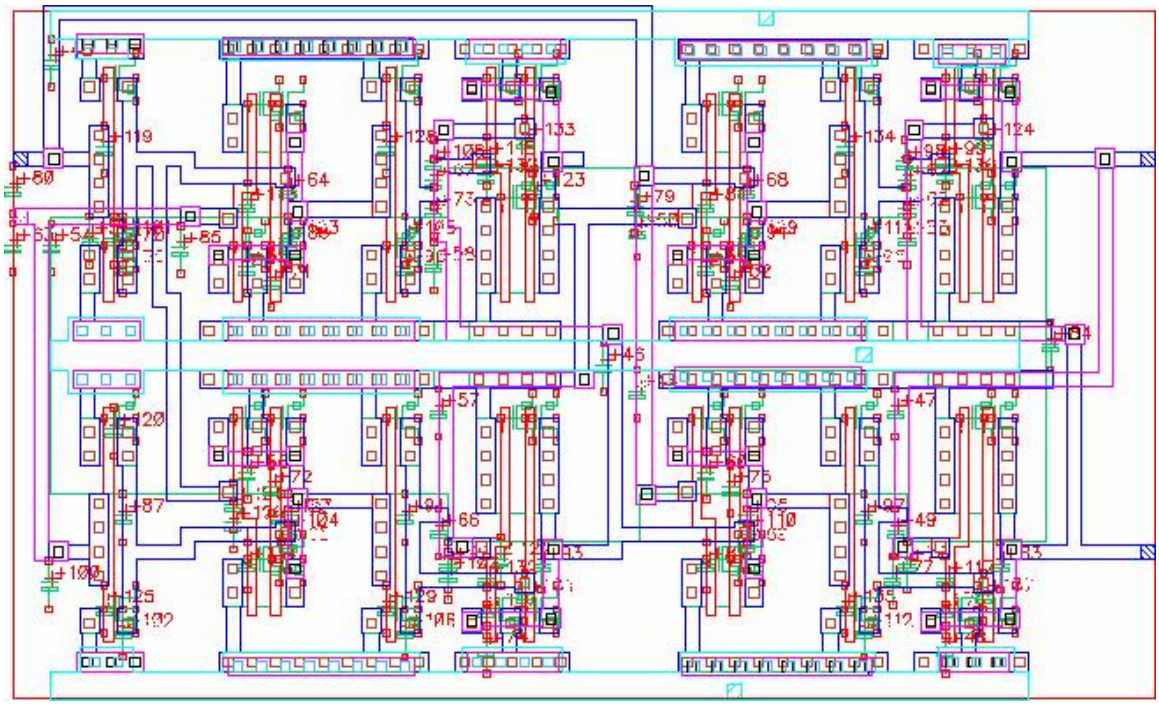

Fig 33. Extracted view of D flip flop

4.8 Full Adder

The Layout and Extracted views for a Full Adder are shown below.

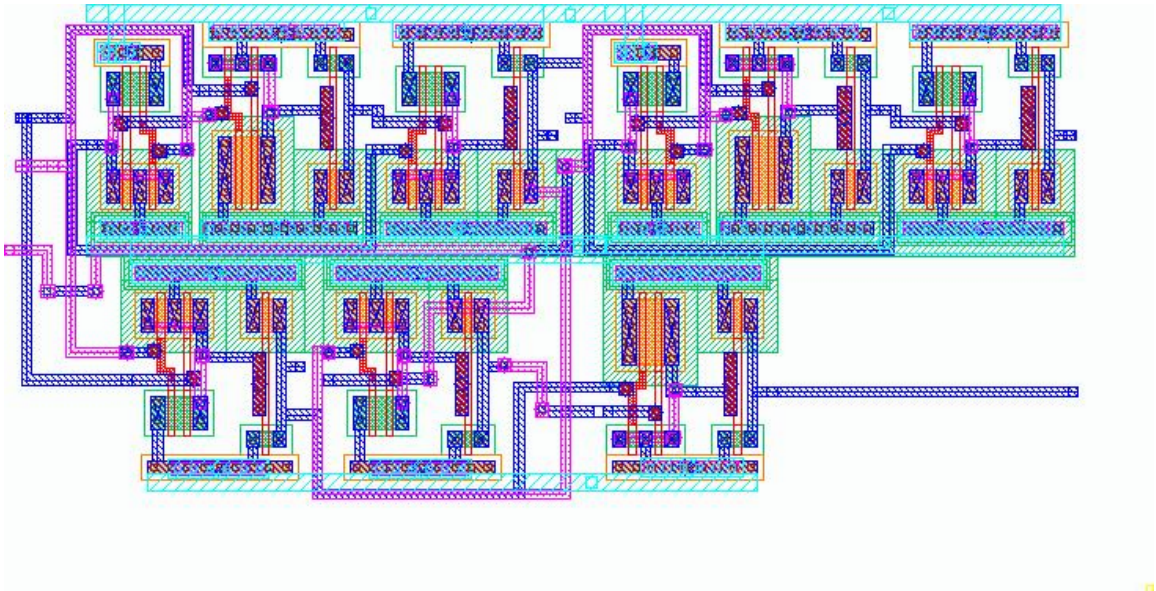

Fig 34. Layout of Full Adder

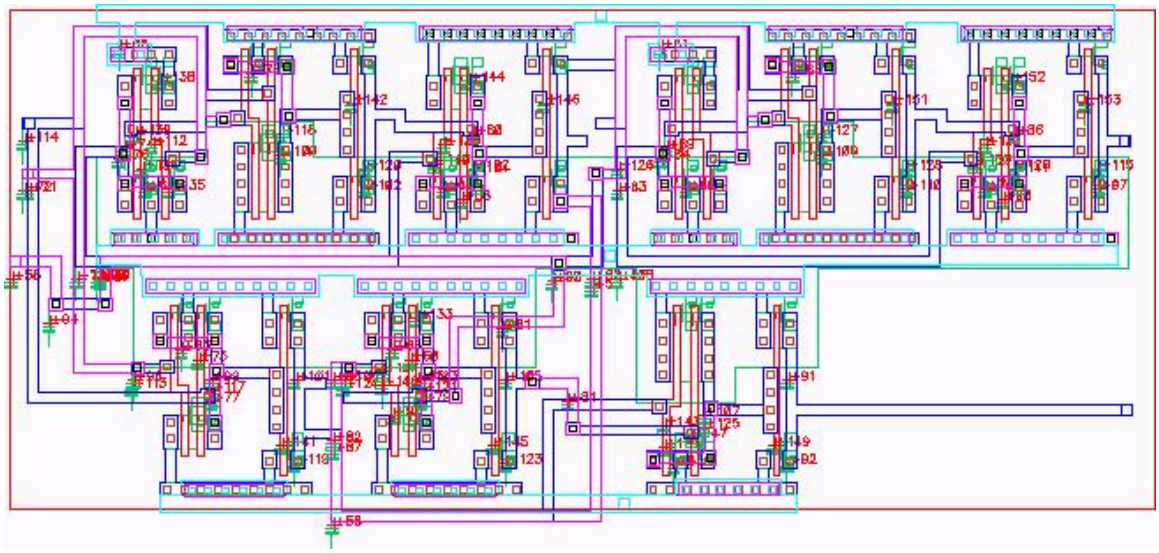

Fig 35. Extracted view of Full Adder

4.9. a 4 Bit Accumulator

The Layout and Extracted views of a 4 bit accumulator is shown.

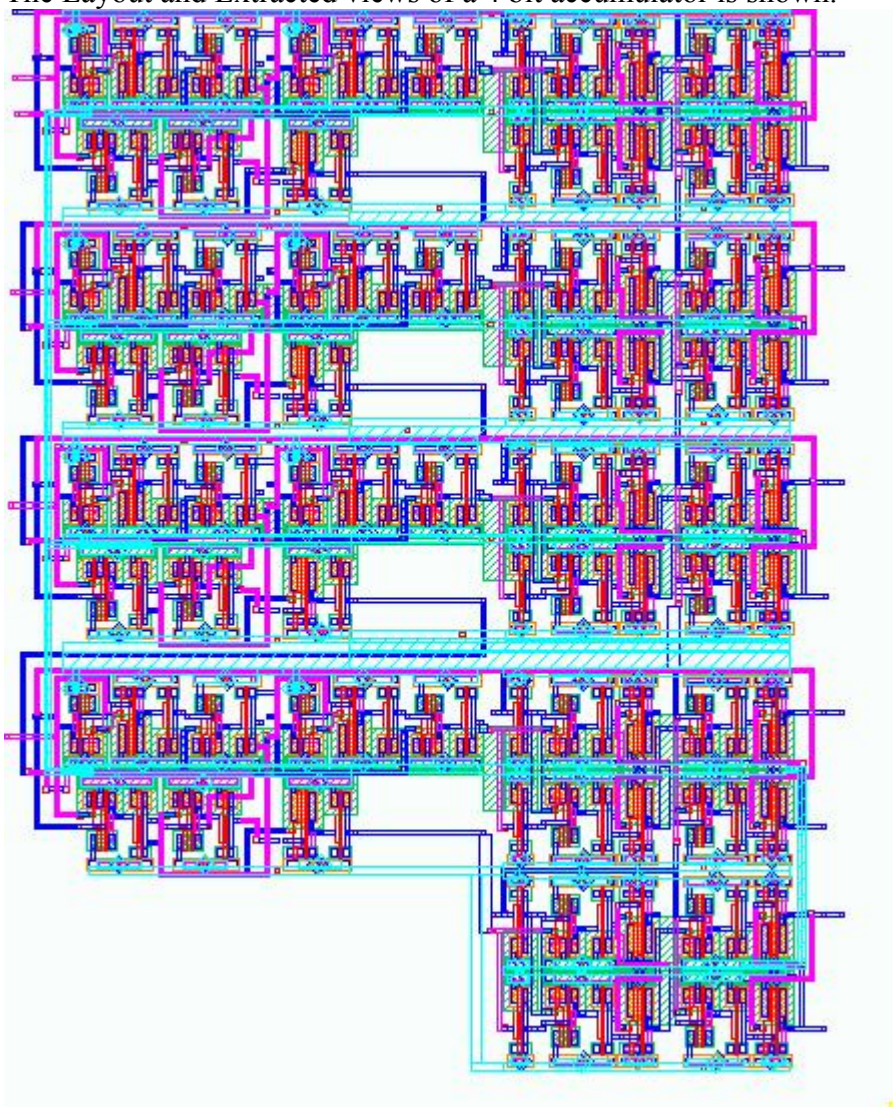

Fig 36. Layout of 4 Bit Accumulator

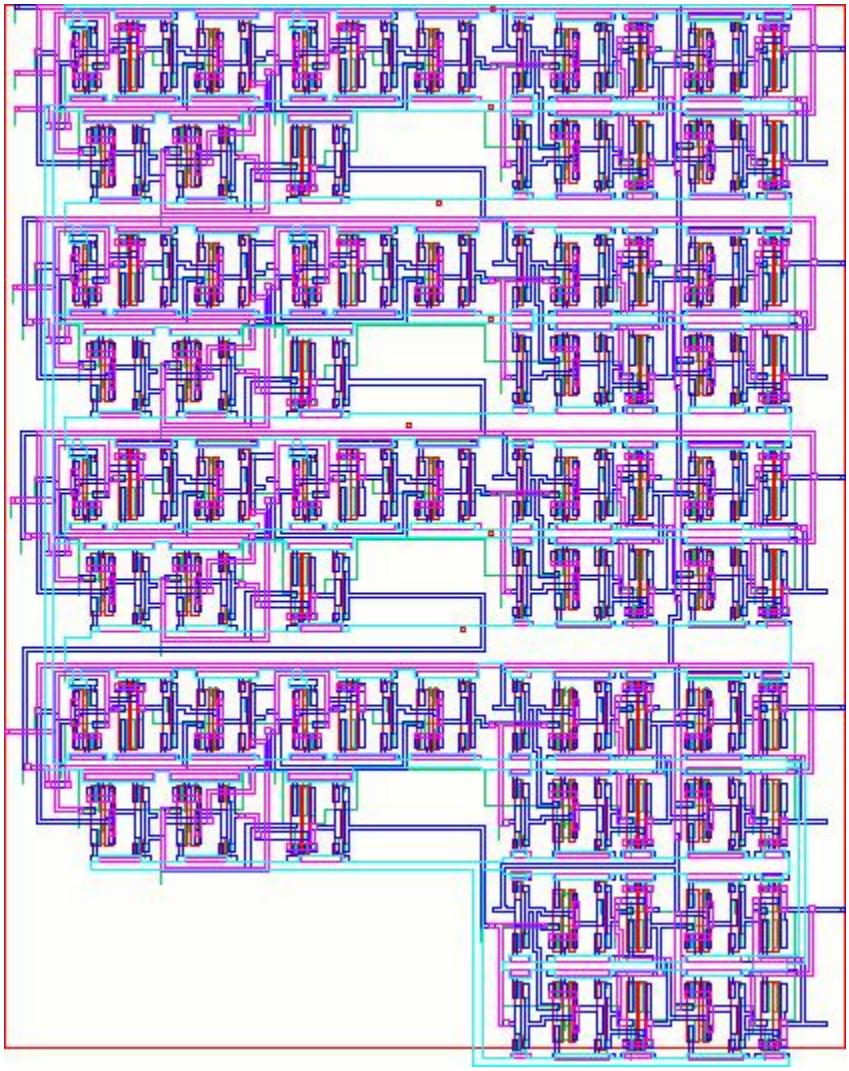

Fig 37.Extracted view of 4 Bit Accumulator

4.9. b 12 Bit Accumulator

The Layout and Extracted views of a 12 bit accumulator are shown.

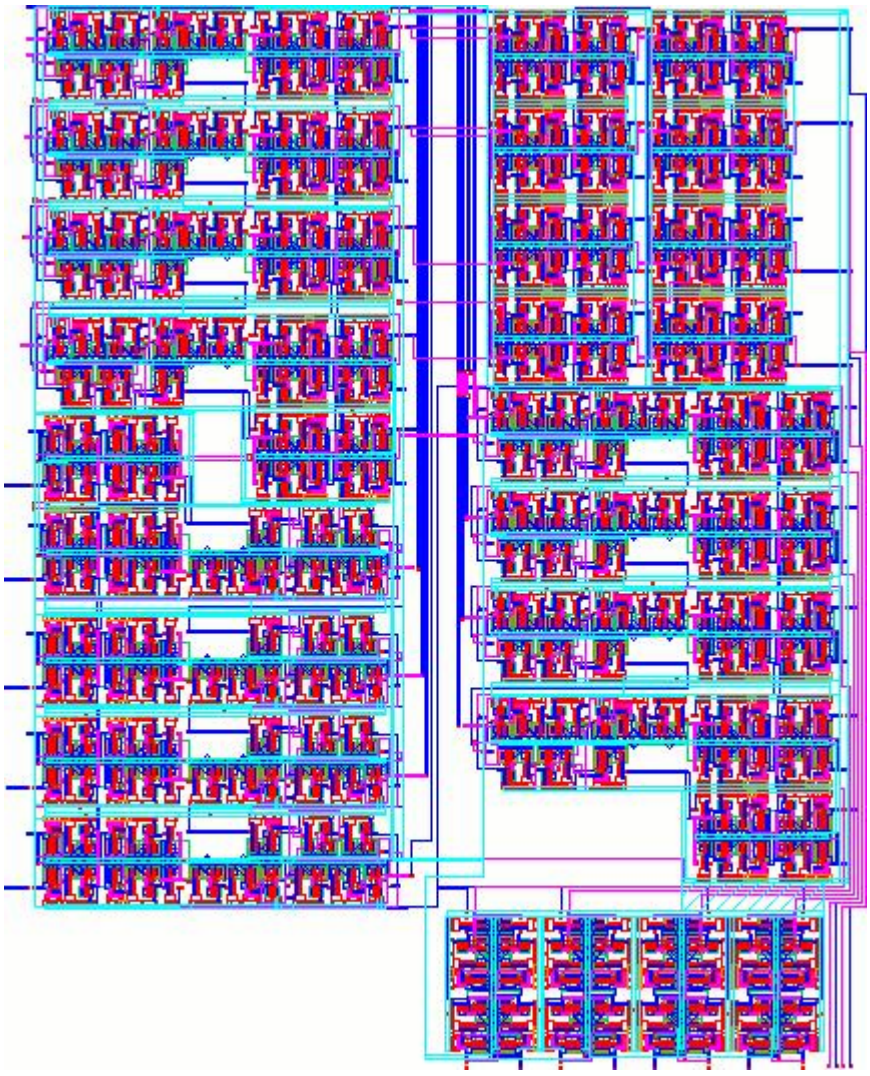

Fig 38. Layout of 12 Bit Accumulator

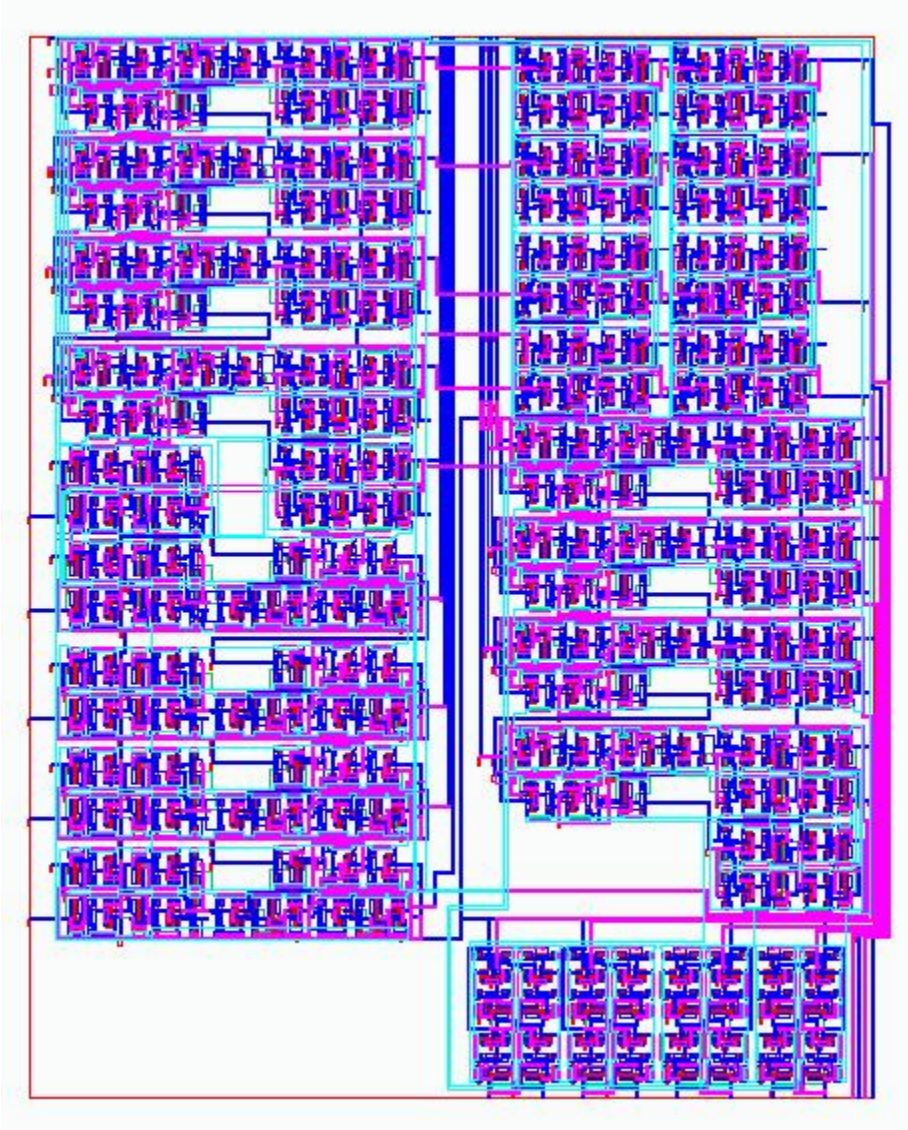

Fig 39. Extracted view of 12 Bit Accumulator

Chapter 5
Power Dissipation

In this section, I will examine the sources of power dissipation in CMOS gates and describe briefly the power dissipation taking place in my design. Power consumption in CMOS digital has been increasing at an alarming rate over the past few technology generations. It has become perhaps the most important design specification in recent year since it affects power grid design, chip temperature, packing decisions, and long term reliability. If the trend for the chip power continues, it will begin to dictate the logical/memory composition of further designs and force most of the chip to be dominated by memory, which consumes less power than logical circuits.

In CMOS the source of power can be broadly categorized into two groups:

1. Dynamic Power
2. Static Power

Dynamic power arises from the sources: power due to capacitance switching, short circuit power due to "crowbar" current flowing from Vdd to Gnd during switching, and power due to glitches in the output waveforms. Static power is due to leakage currents (sub threshold current and source/drain junction reverse-bias current) and dc standby current (e.g. pseudo NMOS circuits with low output).

Switching Power is given by

$$P_{switching} = I_{D,avg} V_{DD} = C_L \Delta V_{swing} f_{avg} V_{DD} = C_L V_{DD}^2 f_{avg}$$

Crowbar current is the current that flows directly from V_{DD} to G_{nd} during switching events. The reason why short-circuit flows is that for a certain period of time both transistors are on simultaneously; that is. $|V_{GS}| \rangle |V_T|$ for both devices. If we apply a step input, only one device would be on at any given point in time and we would not observed any short-circuit current. However, since all input have a finite slope, both devices are on when $V_{TN} < V_{in} < V_{DD} - |V_{TP}|$. Crowbar current flows in both charging and discharging conditions. The time period that short circuit current flows depends on the rise/fall time of the input:

$$\Delta t_{sc} = \Delta t_{scr} + \Delta t_{scf}$$

$$P_{sc} = I_{sc} V_{DD}$$

Since crowbar current flows during all the switching events, it is possible to rewrite the equation as follows. Taking $I_{SC,avg}$ as the average crowbar current during the switching intervals, then

$$I_{sc} = \frac{\Delta t_{sc}}{T} I_{SC,avg}$$

This can be substituted in to the previous equation to obtain

$$P_{sc} = \frac{\Delta t_{sc} I_{sc,avg}}{T} V_{DD} = \Delta t_{SC} I_{SC,avg} V_{DD} f_{clk}$$

For my accumulator design

Δt_{sc} = 156 p s

T = 20 n s

$I_{sc,avg}$ = 30 mA

V_{DD}= 5V

P_{sc} = 1.17 mW

The average power associated with my circuit for a current of 30 mA is 1.17mW.

Chapter 6
DDS Chip

6.1 Design Limitations

6.1.1 Chip Size

1.5×1.5 mm

6.1.2 IO Pins

40(package- 40 pin DIP)

6.2 Chip Layout

The layout of the chip consists of mainly 3 components and they are Accumulator, ROM and the DAC.

The 12 bit accumulator which I have designed is about 380×480 microns and the layout has been shown in chapter 4. The schematic of the DDS chip is given below.

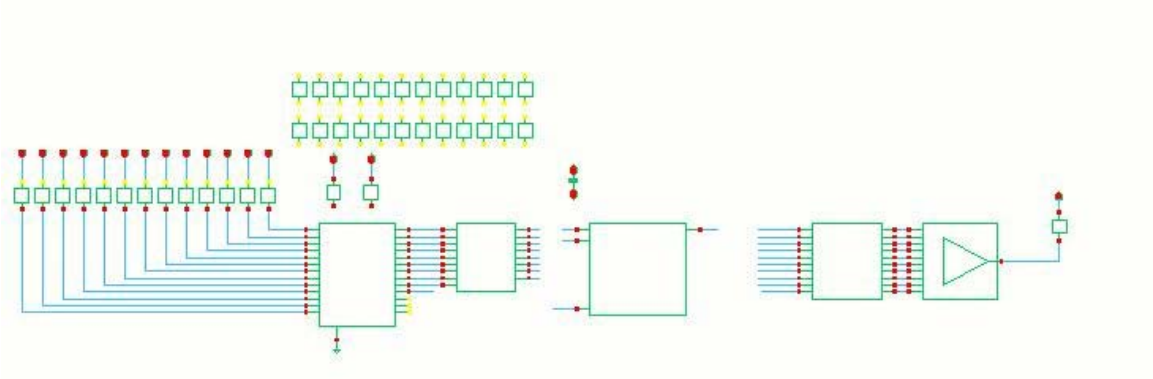

Fig 40. Schematic of the DDS Chip.

Layout of the chip is shown below. Layout of the padset (Appendix A)

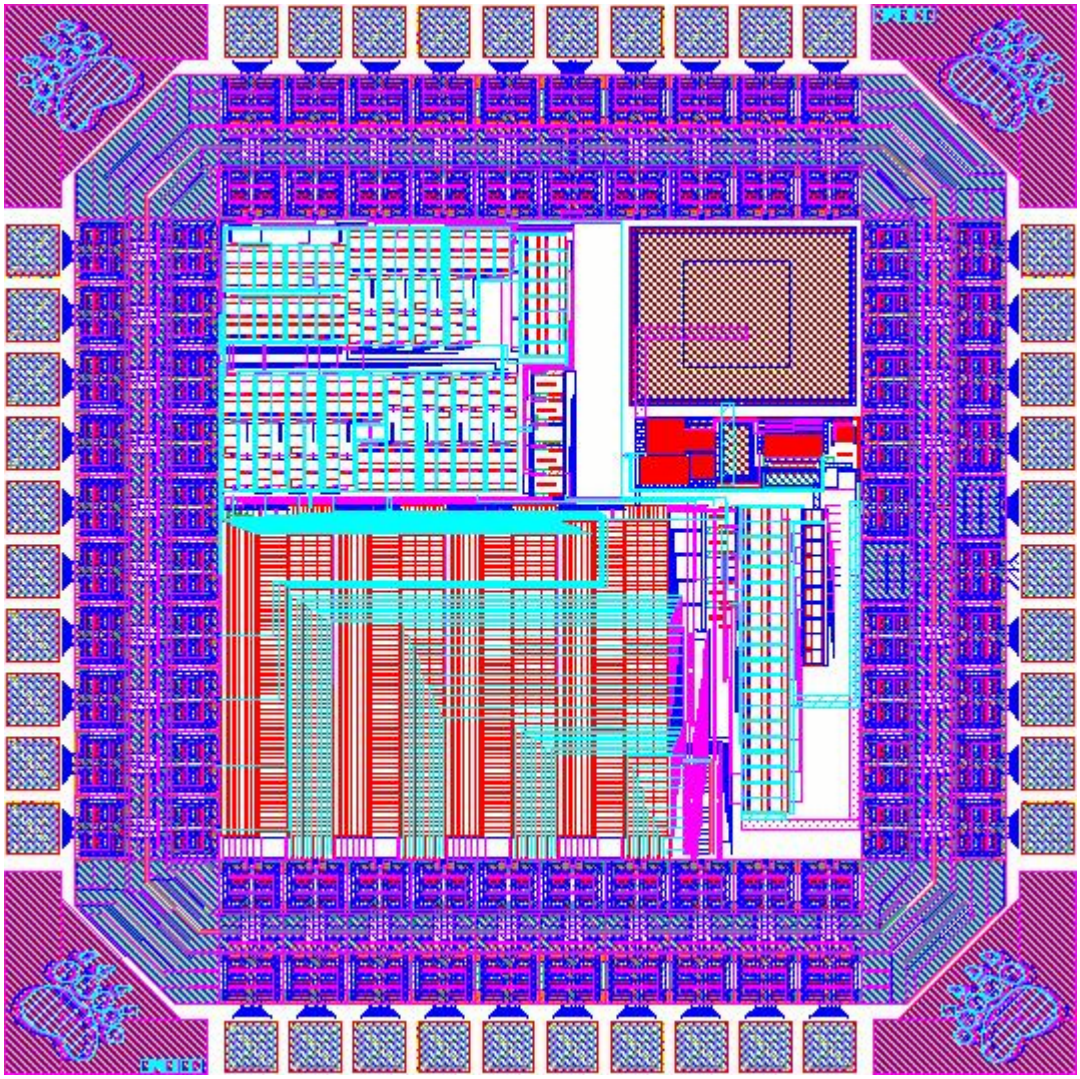

Fig 41. Layout of the DDS Chip.

Chapter 7
Verification

The chip passes LVS and DRC. Once the verification process is completed, we stream out the file (Top cell containing the schematic, layout and extracted views).LVS is then done between GDSII file and the original schematic. The LVS showed “The net-lists match”.

7.1 Output Waveform

The output waveform with parasitic extraction for the chip is a sine wave of frequency 25 MHz and having a peak-to-peak voltage of 1.7 V. The waveform is shown.

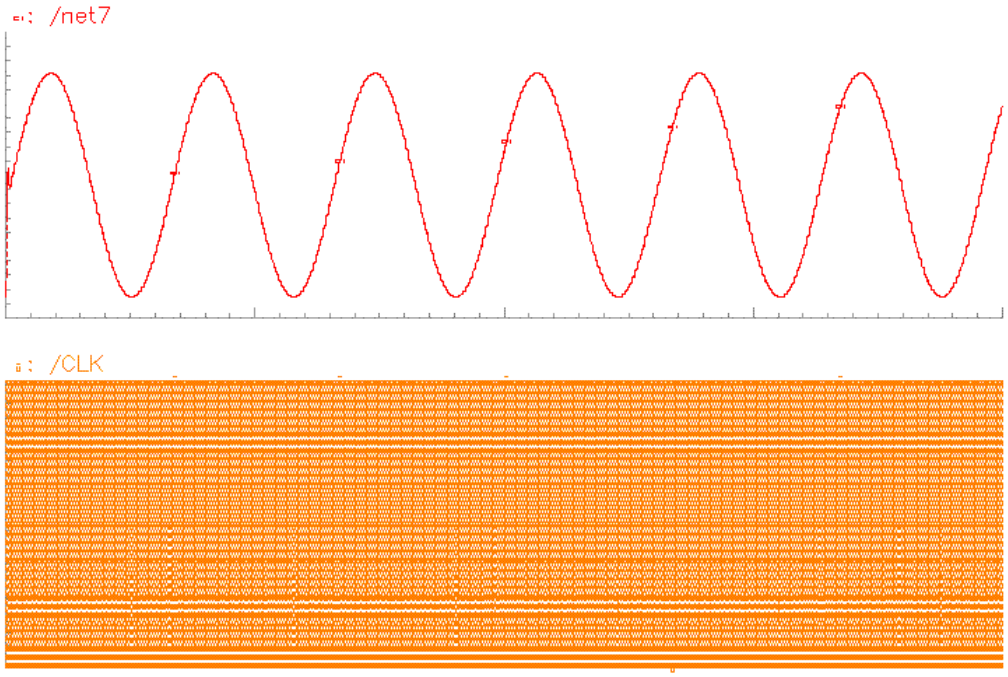

Fig 42. Output Waveform of the DDS Chip.

Chapter 8
Conclusion

A 12 Bit accumulator was designed to operate at a frequency of 50 MHz. Simulations with extracted parasitics indicates that the device functions properly. The device though designed to operate at 50 MHz can function up to 150 MHz with no loss in signal. A layout of the DDS chip was made and it passes both DRC and LVS. Output waveform was observed to be a sine wave of frequency 25 MHz and a V pp of 1.7 V. The project assigned has been completed and is currently queued for fabrication.

Chapter 9
Bibliography

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- **David A. Hodges, Horace G. Jackson, Resve A.Saleh.** *Analysis and Design of Digital Integrated Circuits, third edition, McGraw Hill*
- CHU WING-YEE, CHEE VOON-YEW, YUNG WAI-MING, *16 Bit Digital Accumulator*, Senior Design Project, Iowa State University, MAY 99
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Appendix A
Pad Specification

Pin	R (ohm)	L (nH)	C (pF)	t_{of} (ps)
1,20,21,40	0.217	8.18	5.32	209
2,19,22,39	0.177	7.92	4.39	187
3,18,23,38	0.154	7.34	3.37	157
4,17,24,37	0.110	6.48	2.34	1213
5,16,25,36	0.103	5.69	2.16	111
6,15,26,35	0.0661	4.37	1.43	79.0
7,14,27,34	0.0646	4.54	1.48	81.9
8,13,28,33	0.0498	3.69	1.05	62.3
9,12,29,32	0.0378	3.54	0.863	55.3
10,11,30,31	0.0247	3.15	0.660	45.6

Appendix B
Pad Orientation

PIN	PAD TYPE	NAME	DESCRIBTION
1	Padvdd	Vdd	Vdd pin
2	Padio		
3	Padio		
4	Padio		
5	Padio		
6	Padio		
7	Padio		
8	Padio		
9	Padio		
10	Padaref	out	Out pin
11	Padio	Clk	Clk pin
12	Padio		
13	Padio		
14	Padio	A4	4^{th} input from ACC
15	Padio	A5	5^{th} input from ACC
16	Padio	A6	6^{th} input from ACC
17	Padio	A7	7^{th} input from ACC
18	Padio	A8	8^{th} input from ACC
19	Padio	A9	9^{th} input from ACC
20	Padio	A10	10^{th} input from ACC
21	Padio	A11	11^{h} input from ACC
22	Padio	A3	3^{rd} input from ACC
23	Padio	A2	2^{nd} input from ACC
24	Padio	A1	1^{st} input from ACC
25	Padio	A0	0 input from ACC
26	Padio		
27	Padio		
28	Padio		
29	Padio		
30	Padio		
31	Padio		
32	Padio		
33	Padio		
34	Padio		
35	Padio		
36	Padio		
37	Padio		
38	Padio		

39	Padio		
40	Padgnd	Gnd	Gnd pin